

the output Q via a pull-up resistor. If these integrated resistors are not desired, the TLE42794 can be used instead of the TLE42694.

Dimensioning information on external components

The input capacitor C_I is recommended for compensation of line influences. The output capacitor C_Q is necessary for the stability of the control loop.

Circuit description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The TLE42694 also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

Type	Package	Marking
TLE42694G	PG-DSO-8	42694G
TLE42694GM	PG-DSO-14	42694GM
TLE42694E	PG-SSOP-14 exposed pad	42694E

Block diagram

1 Block diagram

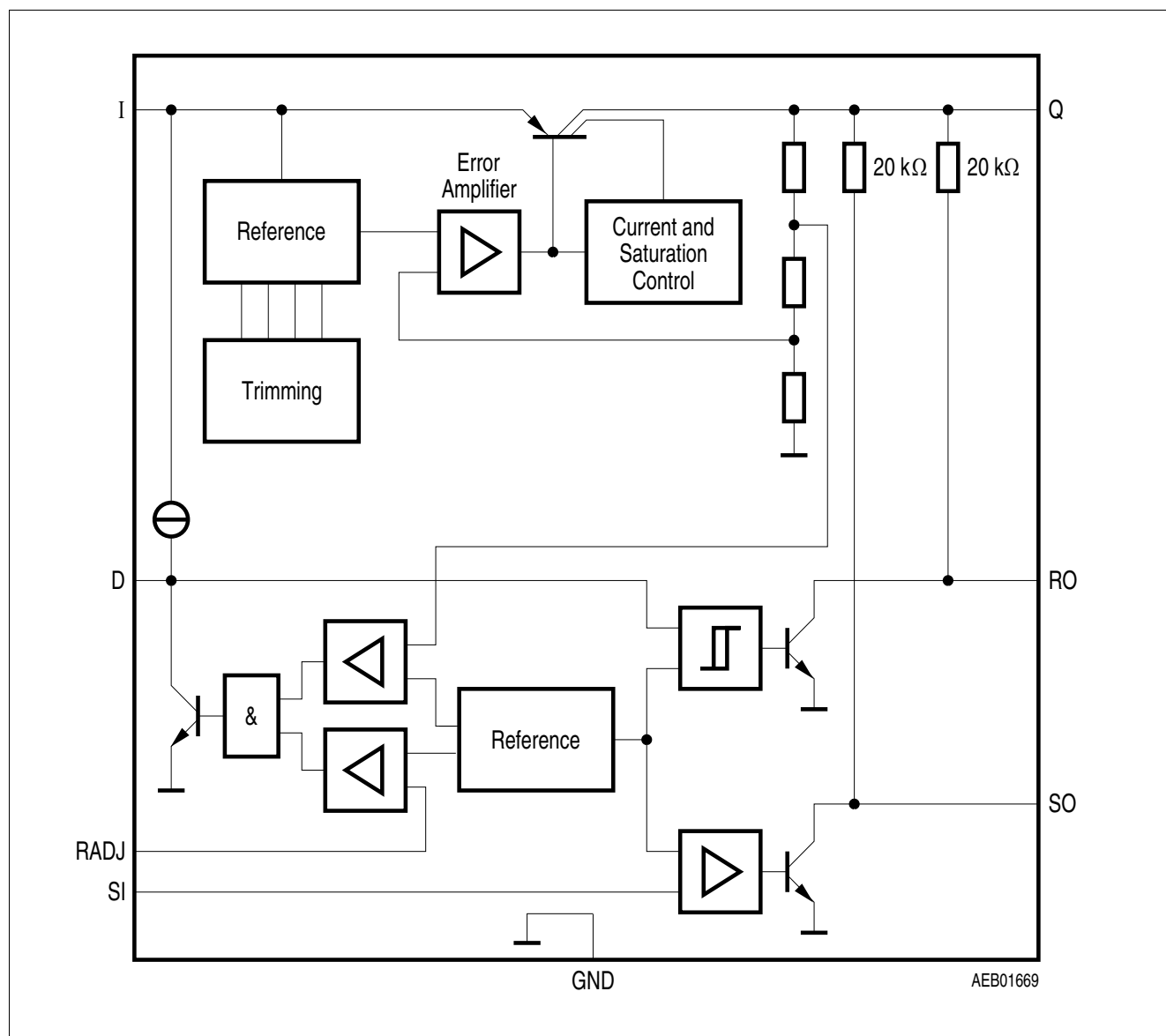


Figure 1 Block diagram

Pin configuration

2 Pin configuration

2.1 Pin assignment PG-DSO-8

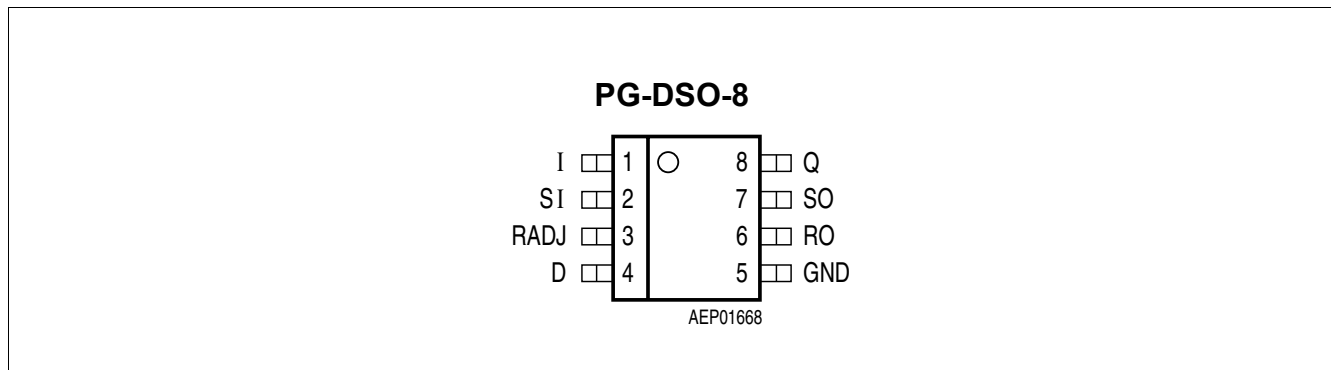


Figure 1 Pin configuration (top view)

2.2 Pin definitions and functions PG-DSO-8

Table 1 Pin definitions and functions PG-DSO-8

Pin	Symbol	Function
1	I	Input for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	SI	Sense input connect the voltage to be monitored; connect to Q if the sense comparator is not needed
3	RADJ	Reset threshold adjust connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
4	D	Reset delay timing connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
5	GND	Ground
6	RO	Reset output the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the reset function is not needed
7	SO	Sense output the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the sense comparator is not needed
8	Q	Output connect a capacitor to GND close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in “Functional range” on Page 9

Pin configuration

2.3 Pin assignment PG-DSO-14

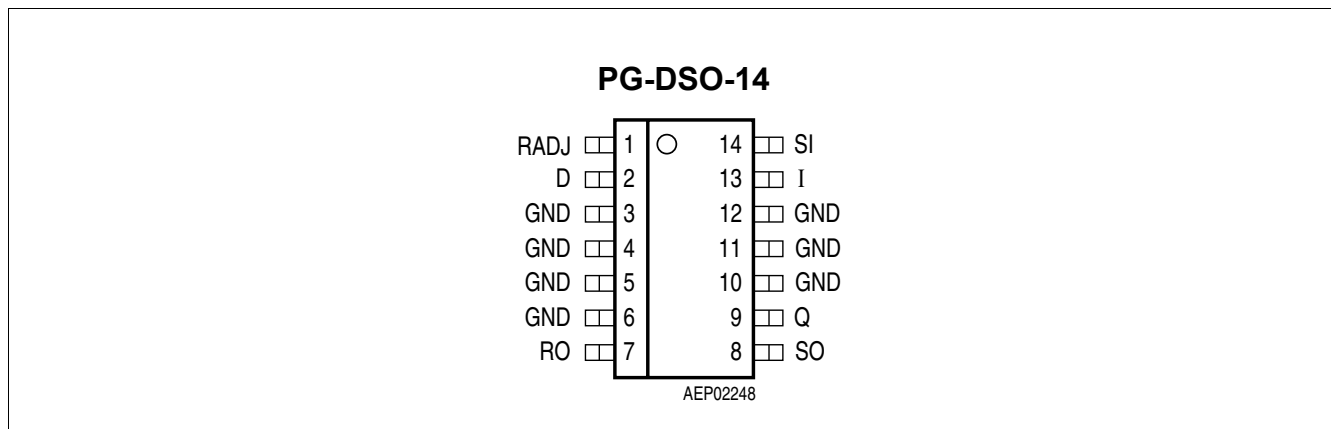


Figure 2 Pin configuration (top view)

2.4 Pin definitions and functions PG-DSO-14

Table 2 Pin definitions and functions PG-DSO-14

Pin	Symbol	Function
1	RADJ	Reset threshold adjust connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2	D	Reset delay timing connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
3, 4, 5, 6, 10, 11, 12	GND	Ground Connect all pins to GND and to the heatsink area for improved cooling
7	RO	Reset output the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	Sense Output the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the sense comparator is not needed
9	Q	Output block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table “Functional range” on Page 9
13	I	Input for compensating line influences, a capacitor to GND close to the IC terminals is recommended
14	SI	Sense input connect the voltage to be monitored; connect to Q if the sense comparator is not needed

Pin configuration

2.5 Pin assignment PG-SSOP-14 exposed pad

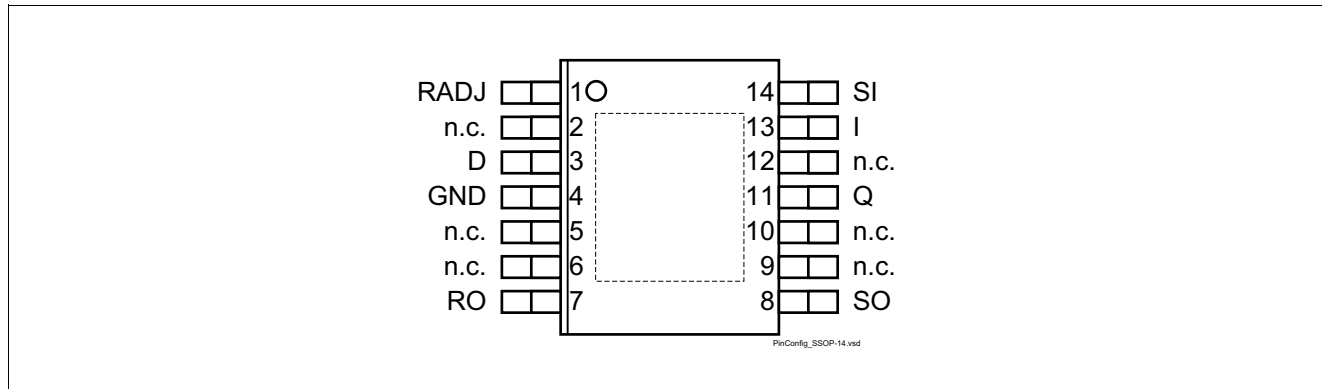


Figure 3 Pin configuration (top view)

2.6 Pin definitions and functions PG-SSOP-14 exposed pad

Table 3 Pin definitions and functions PG-SSOP-14 exposed pad

Pin	Symbol	Function
1	RADI	Reset threshold adjust connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2, 5, 6	n.c.	Not connected
3	D	Reset delay timing connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
4	GND	Ground Connect to GND
7	RO	Reset output the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	Sense output the open collector output is connected to the 5 V output via an integrated 20 kΩ pull-up resistor; leave open if the sense comparator is not needed
9, 10, 12	n.c.	Not connected
11	Q	Output block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table “Functional range” on Page 9
13	I	Input for compensating line influences, a capacitor to GND close to the IC terminals is recommended

Pin configuration

Table 3 Pin definitions and functions PG-SSOP-14 exposed pad (cont'd)

Pin	Symbol	Function
14	SI	Sense input connect the voltage to be monitored; connect to Q if the sense comparator is not needed
Pad	-	Exposed pad connect to heatsink area; connect to GND

3 General product characteristics

3.1 Absolute maximum ratings

Table 4 Absolute maximum ratings¹⁾

-40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input, sense input							
Voltage	V_I, V_{SI}	-40	–	45	V	–	P_4.1.1
Output, reset output, sense output, reset delay							
Voltage	V_Q, V_{RO}, V_{SO}, V_D	-0.3	–	7	V	–	P_4.1.2
Reset threshold							
Voltage	V_{RADJ}	-0.3	–	7	V	–	P_4.1.3
Current	I_{RADJ}	-10	–	10	mA	–	P_4.1.4
Temperature							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.5
Storage Temperature	T_{stg}	-50	–	150	°C	–	P_4.1.6
ESD susceptibility							
Human Body Model (HBM) ²⁾	Voltage	-2	–	2	kV	–	P_4.1.7
Charged Device Model (CDM) ³⁾	Voltage	-1	–	1	kV	–	P_4.1.8

1) not subject to production test, specified by design

2) ESD HBM Test according to AEC-Q100-002 - JESD22-A114

3) ESD CDM Test according to ESDA ESD-STM5.3.1

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.

General product characteristics

3.2 Functional range

Table 5 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage	V_I	5.5	–	45	V	–	P_4.2.1
Output capacitor's requirements for stability	C_Q	10	–	–	μF	– ¹⁾	P_4.2.2
Output capacitor's requirements for stability	$ESR(C_Q)$	–	–	3	Ω	– ²⁾	P_4.2.3
Junction temperature	T_j	–40	–	150	$^{\circ}\text{C}$	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) Relevant ESR value at $f = 10 \text{ kHz}$

Note: *Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

General product characteristics

3.3 Thermal resistance

Table 6 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TLE42694G (PG-DSO-8)							
Junction to soldering point ¹⁾	R_{thJSP}	–	80	–	K/W	measured to pin 5	P_4.3.1
Junction to ambient ¹⁾	R_{thJA}	–	113	–	K/W	FR4 2s2p board ²⁾	P_4.3.2
Junction to ambient ¹⁾	R_{thJA}	–	170	–	K/W	FR4 1s0p board, footprint only ³⁾	P_4.3.3
Junction to ambient ¹⁾	R_{thJA}	–	142	–	K/W	FR4 1s0p board, 300 mm ² heatsink area on PCB ³⁾	P_4.3.4
Junction to ambient ¹⁾	R_{thJA}	–	136	–	K/W	FR4 1s0p board, 600 mm ² heatsink area on PCB ³⁾	P_4.3.5
TLE42694GM (PG-DSO-14)							
Junction to soldering point ¹⁾	R_{thJSP}	–	27	–	K/W	measured to group of pins 3, 4, 5, 10, 11, 12	P_4.3.6
Junction to ambient ¹⁾	R_{thJA}	–	63	–	K/W	FR4 2s2p board ²⁾	P_4.3.7
Junction to ambient ¹⁾	R_{thJA}	–	104	–	K/W	FR4 1s0p board, footprint only ³⁾	P_4.3.8
Junction to ambient ¹⁾	R_{thJA}	–	73	–	K/W	FR4 1s0p board, 300 mm ² heatsink area on PCB ³⁾	P_4.3.9
Junction to ambient ¹⁾	R_{thJA}	–	65	–	K/W	FR4 1s0p board, 600 mm ² heatsink area on PCB ³⁾	P_4.3.10
TLE42694E (PG-SSOP-14 exposed pad)							
Junction to soldering point ¹⁾	R_{thJSP}	–	10	–	K/W	measured to pin 5	P_4.3.11
Junction to ambient ¹⁾	R_{thJA}	–	47	–		FR4 2s2p board ²⁾	P_4.3.12
Junction to ambient ¹⁾	R_{thJA}	–	145	–	K/W	FR4 1s0p board, Footprint only ³⁾	P_4.3.13
Junction to ambient ¹⁾	R_{thJA}	–	63	–	K/W	FR4 1s0p board, 300 mm ² heatsink area on PCB ³⁾	P_4.3.14
Junction to ambient ¹⁾	R_{thJA}	–	53	–	K/W	FR4 1s0p board, 600 mm ² heatsink area on PCB ³⁾	P_4.3.15

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q , the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional range" on Page 9** have to be maintained. For details see also the typical performance graph **"Output capacitor series resistor ESR(C_Q) versus output current I_Q " on Page 14**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor C_I is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above $V_I = 22$ V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150°C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42694 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

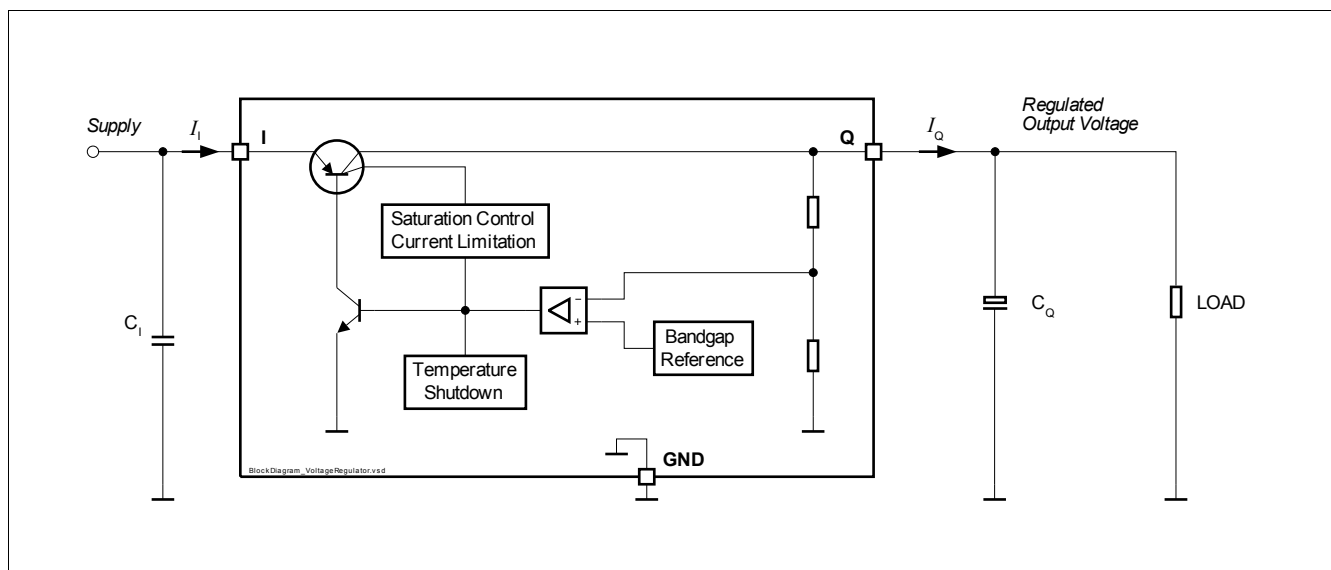


Figure 4 Voltage regulator

Block description and electrical characteristics

Table 7 Electrical characteristics voltage regulator

$V_I = 13.5 \text{ V}$, $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_Q	4.9	5.0	5.1	V	$100 \mu\text{A} < I_Q < 100 \text{ mA}$ $6 \text{ V} < V_I < 18 \text{ V}$	P_5.1.1
Output current limitation	$I_{Q,\text{max}}$	150	200	500	mA	$V_Q = 4.8 \text{ V}$	P_5.1.2
Load regulation steady-state	$\Delta V_{Q,\text{load}}$	-30	-15	–	mV	$I_Q = 5 \text{ mA to } 100 \text{ mA}$ $V_I = 6 \text{ V}$	P_5.1.3
Line regulation steady-state	$\Delta V_{Q,\text{line}}$	–	10	40	mV	$V_I = 6 \text{ V to } 32 \text{ V}$ $I_Q = 5 \text{ mA}$	P_5.1.4
Dropout voltage ¹⁾ $V_{\text{dr}} = V_I - V_Q$	V_{dr}	–	250	500	mV	$I_Q = 100 \text{ mA}$	P_5.1.5
Overtemperature shutdown threshold	$T_{j,\text{sd}}$	151	–	200	°C	T_j increasing ²⁾	P_5.1.6
Overtemperature shutdown threshold hysteresis	$T_{j,\text{sdh}}$	–	15	–	°C	T_j decreasing ²⁾	P_5.1.7
Power supply ripple rejection	$PSRR$	–	70	–	dB	$f_{\text{ripple}} = 100 \text{ Hz}$ $V_{\text{ripple}} = 0.5 V_{\text{pp}}$	P_5.1.8

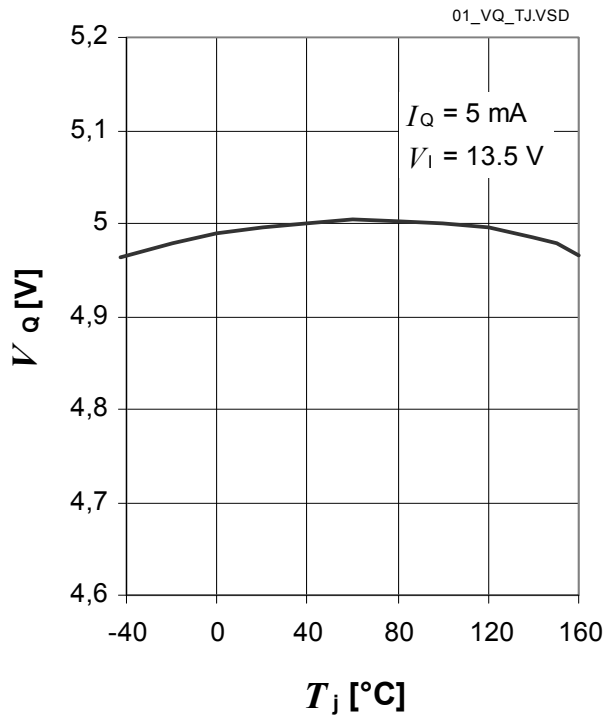
1) Measured when the output voltage V_Q has dropped 100mV from the nominal value obtained at $V_I = 13.5 \text{ V}$

2) Not subject to production test, specified by design

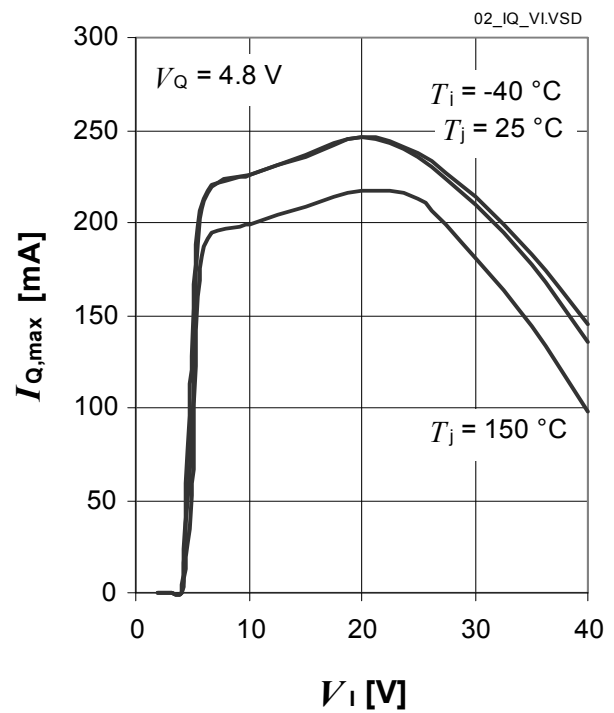
Block description and electrical characteristics

Typical Performance Characteristics Voltage Regulator

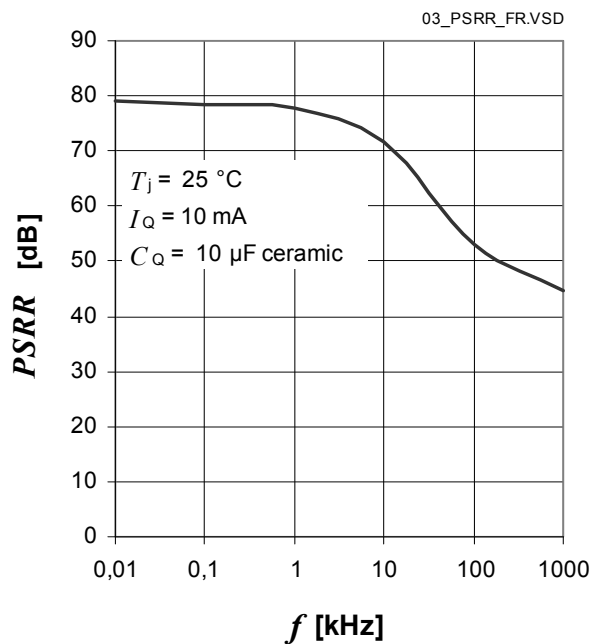
**Output voltage V_Q versus
junction temperature T_j**



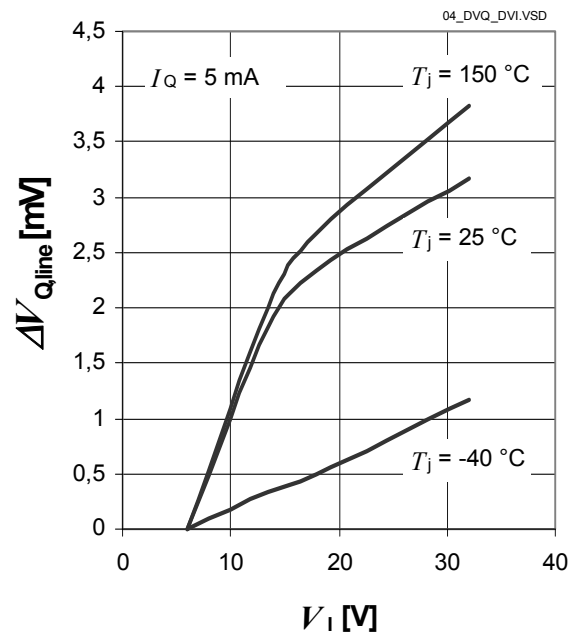
**Output current I_Q versus
input voltage V_I**



**Power supply ripple rejection $PSRR$ versus
ripple frequency f_r**

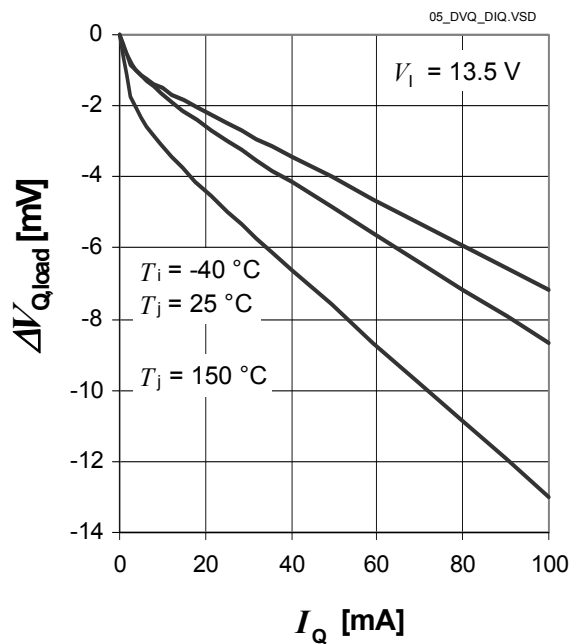


**Line regulation $\Delta V_{Q,line}$ versus
input voltage change ΔV_I**

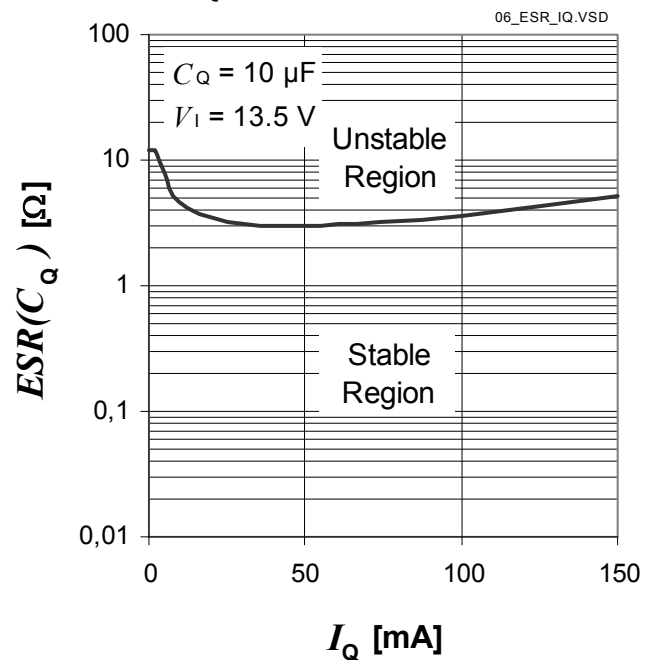


Block description and electrical characteristics

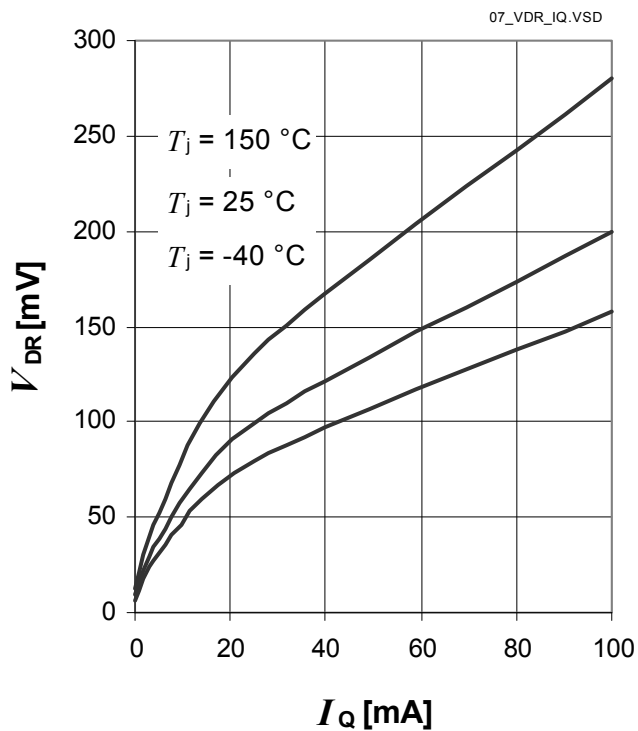
Load regulation $\Delta V_{Q,load}$ versus output current change ΔI_Q



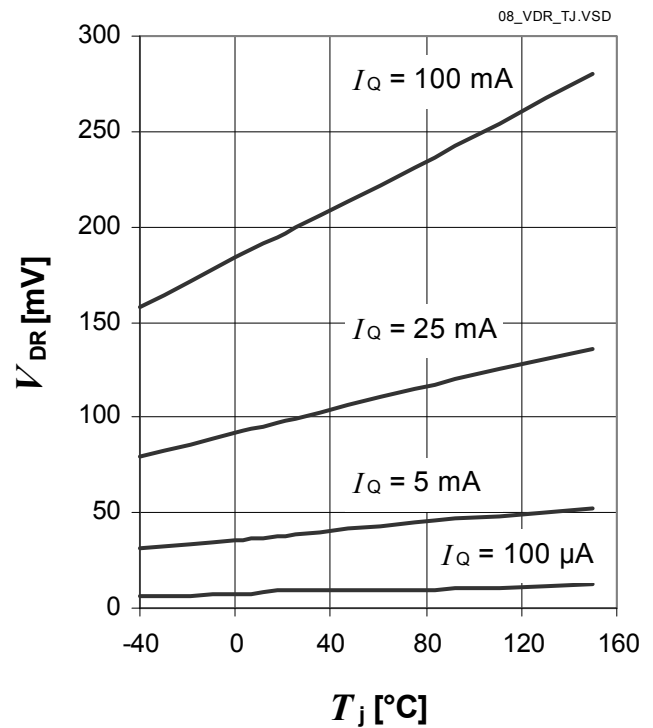
Output capacitor series resistor $ESR(C_Q)$ versus output current I_Q



Dropout voltage V_{dr} versus output current I_Q



Dropout voltage V_{dr} versus junction temperature T_j



Block description and electrical characteristics

4.2 Current consumption

Table 8 Electrical characteristics current consumption

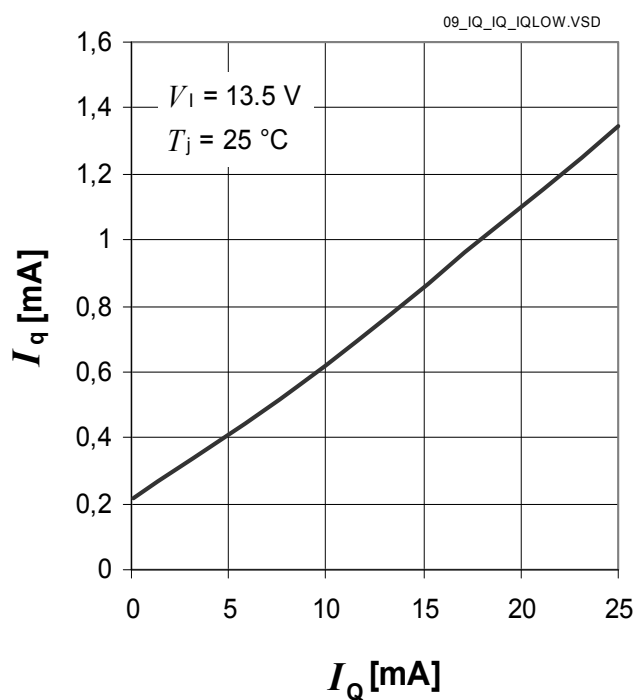
$V_I = 13.5 \text{ V}$, $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I - I_Q$	I_q	–	210	280	μA	$I_Q = 100 \mu\text{A}$ $T_j = 25^\circ\text{C}$	P_5.2.1
Current consumption $I_q = I_I - I_Q$	I_q	–	240	300	μA	$I_Q = 100 \mu\text{A}$ $T_j \leq 85^\circ\text{C}$	P_5.2.2
Current consumption $I_q = I_I - I_Q$	I_q	–	0.7	1	mA	$I_Q = 10 \text{ mA}$	P_5.2.3
Current consumption $I_q = I_I - I_Q$	I_q	–	3.5	8	mA	$I_Q = 50 \text{ mA}$	P_5.2.4

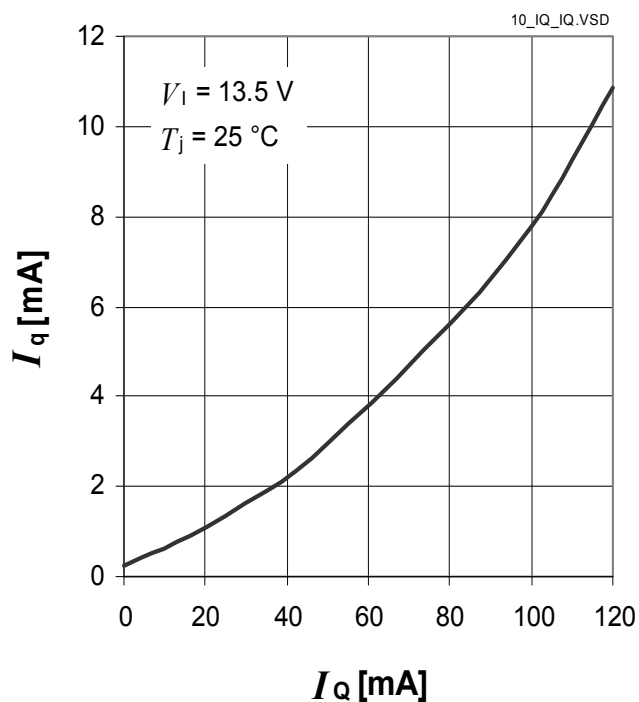
Block description and electrical characteristics

Typical performance characteristics current consumption

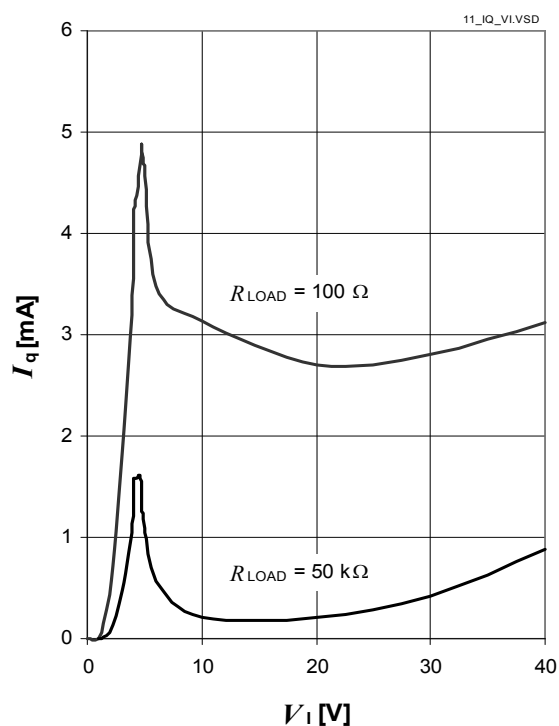
Current consumption I_q versus output current I_Q (I_Q low)



Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



Block description and electrical characteristics

4.3 Reset function

The reset function provides several features:

Output undervoltage reset:

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-on reset delay time:

The power-on reset delay time t_{rd} allows a microcontroller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold V_{RT} until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D charged by the delay capacitor charge current $I_{D,ch}$ starting from $V_D = 0$ V.

If the application needs a power-on reset delay time t_{rd} different from the value given in **Power-on reset delay time**, the delay capacitor's value can be derived from the specified values in **Power-on reset delay time** and the desired power-on delay time:

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 100\text{nF} \quad (4.1)$$

with

- C_D : capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd} : power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor's tolerance into consideration.

Reset reaction time:

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction time t_{rr} considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D (see typical performance graph for details). Hence, the total reset reaction time becomes:

$$t_{rr} = t_{rd,int} + t_{rr,d} \quad (4.2)$$

with

- t_{rr} : reset reaction time
- $t_{rr,int}$: internal reset reaction time
- $t_{rr,d}$: reset discharge

Optional reset output pull-up resistor $R_{RO,ext}$:

The Reset Output RO is an open collector output with an integrated pull-up resistor. To improve the EMC behavior of the component, an external pull-up resistor to the output V_Q can be added. In **Table 9 “Electrical characteristics reset function” on Page 19** a minimum value for the external resistor $R_{RO,ext}$ is given.

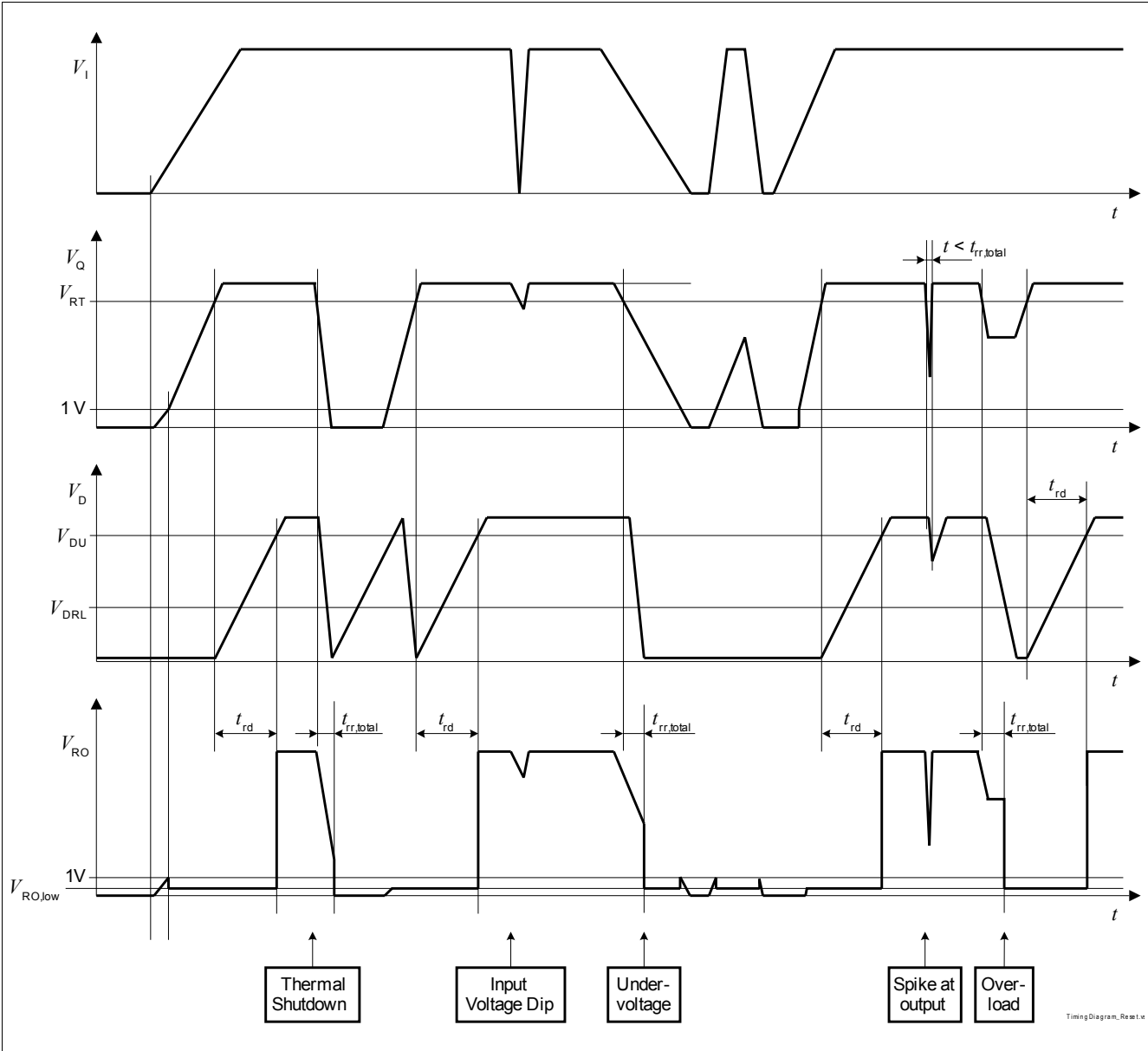


Figure 6 Timing diagram reset

Table 9 Electrical characteristics reset function

$V_I = 13.5\text{ V}$, $-40\text{ °C} \leq T_j \leq 150\text{ °C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset							
Default output undervoltage Reset switching thresholds	V_{RT}	4.5	4.65	4.8	V	V_Q decreasing	P_5.3.1
Output undervoltage reset threshold adjustment							
Reset adjust Switching threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	$3.5\text{ V} \leq V_Q < 5\text{ V}$	P_5.3.2

Block description and electrical characteristics

Table 9 Electrical characteristics reset function (cont'd)

$V_I = 13.5 \text{ V}$, $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset adjustment range ¹⁾	$V_{RT,range}$	3.50	–	4.65	V	–	P_5.3.3
Reset output RO							
Reset output low voltage	$V_{RO,low}$	–	0.1	0.4	V	$1 \text{ V} \leq V_Q \leq V_{RT}$ no external $R_{RO,ext}$	P_5.3.4
Reset output internal pull-up resistor to V_Q	R_{RO}	10	20	40	k Ω	–	P_5.3.5
Optional reset output external pull-up resistor to V_Q	$R_{RO,ext}$	20	–	–	k Ω	$1 \text{ V} \leq V_Q \leq V_{RT}$; $V_{RO} \leq 0.4 \text{ V}$	P_5.3.6
Reset delay timing							
Delay pin output voltage	V_D	–	–	5	V	–	P_5.3.7
Power-on reset delay time	t_{rd}	17	28	39	ms	$C_D = 100 \text{ nF}$	P_5.3.8
Upper delay switching threshold	V_{DU}	–	1.8	–	V	–	P_5.3.9
Lower delay switching threshold	V_{DL}	–	0.45	–	V	–	P_5.3.10
Delay capacitor charge current	$I_{D,ch}$	–	6.5	–	μA	$V_D = 1 \text{ V}$	P_5.3.11
Delay capacitor reset discharge current	$I_{D,dch}$	–	70	–	mA	$V_D = 1 \text{ V}$	P_5.3.12
Delay capacitor discharge time	$t_{rr,d}$	–	1.9	3	μs	Calculated value: $t_{rr,d} = C_D \cdot (V_{DU} - V_{DL}) / I_{D,dch}$ $C_D = 100 \text{ nF}$	P_5.3.13
Internal reset reaction time	$t_{rr,int}$	–	3	7	μs	$C_D = 0 \text{ nF}$ ²⁾	P_5.3.14
Reset reaction time	$t_{rr,total}$	–	4.9	10	μs	Calculated value: $t_{rr,total} = t_{rr,int} + t_{rr,d}$ $C_D = 100 \text{ nF}$	P_5.3.15

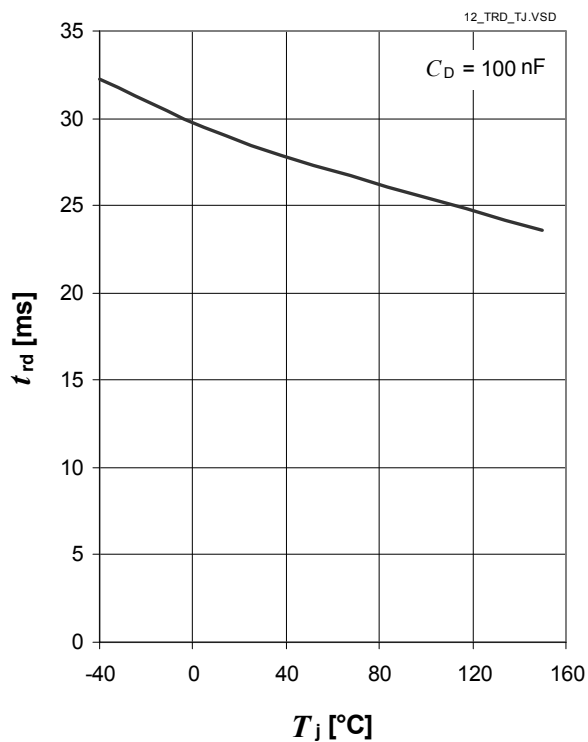
1) V_{RT} is scaled linearly, in case the reset switching threshold is modified

2) Parameter not subject to production test; specified by design

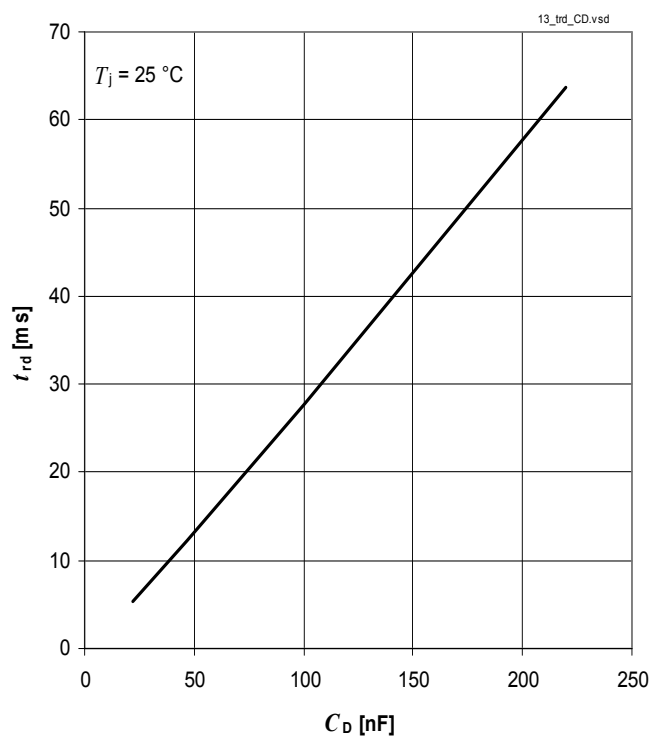
Block description and electrical characteristics

Typical performance characteristics reset function

**Power-on reset delay time t_{rd}
 versus junction temperature T_j**



**Power-on reset delay time t_{rd}
 versus capacitance C_D**



Block description and electrical characteristics

4.4 Early warning function

The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low.

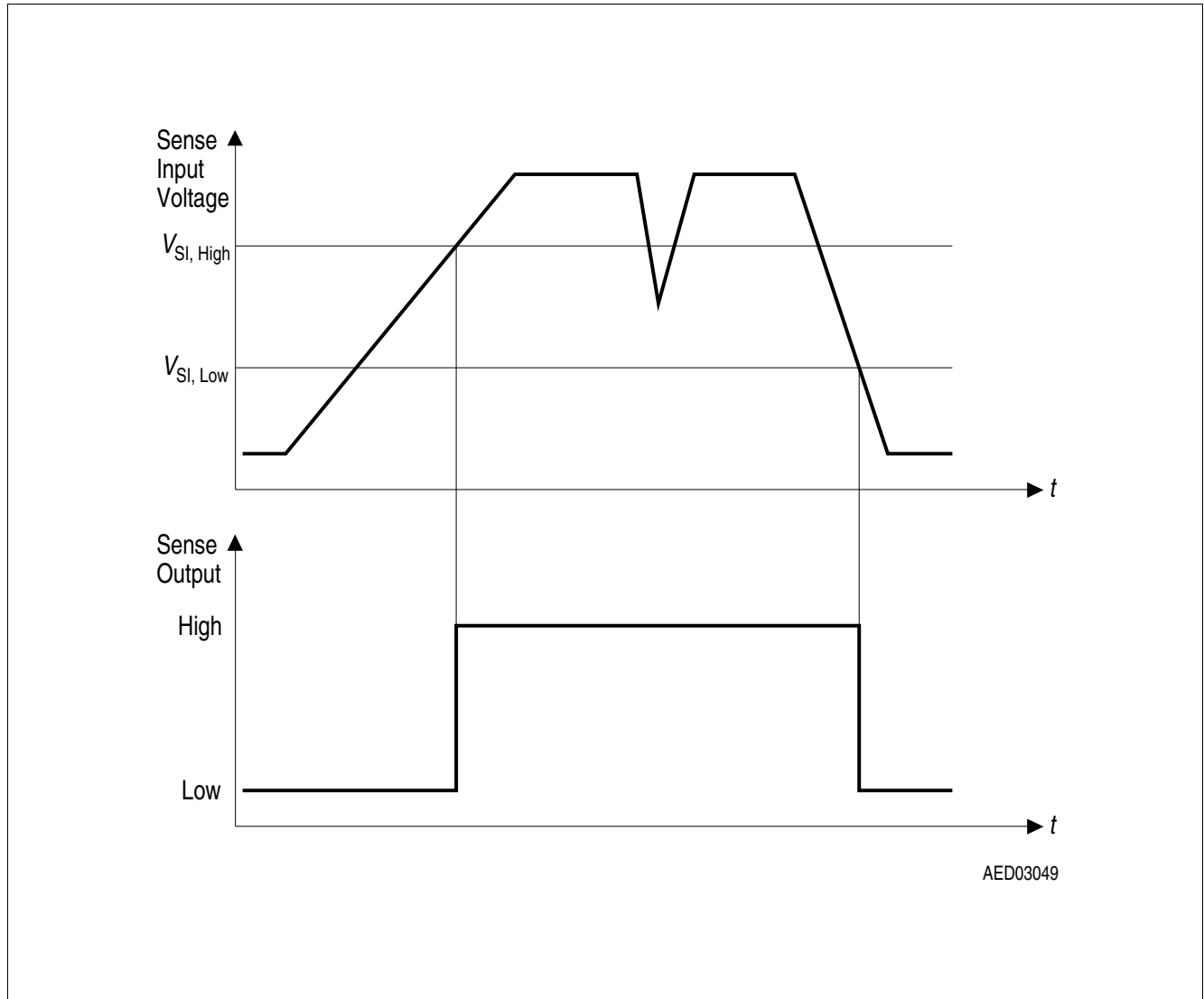


Figure 7 Sense timing diagram

Table 10 Electrical characteristics early warning function

$V_I = 13.5\text{ V}$, $-40\text{ °C} \leq T_j \leq 150\text{ °C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sense comparator input							
Sense threshold high	$V_{SI,high}$	1.24	1.31	1.38	V	–	P_5.4.1
Sense threshold low	$V_{SI,low}$	1.16	1.22	1.28	V	–	P_5.4.2
Sense switching hysteresis	$V_{SI,hy}$	20	90	160	mV	–	P_5.4.3
Sense input current	I_{SI}	-1	-0.1	1	μA	–	P_5.4.4

Block description and electrical characteristics

Table 10 Electrical characteristics early warning function (cont'd)

$V_I = 13.5 \text{ V}$, $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sense comparator output							
Sense output low voltage	$V_{SO,low}$	–	0.1	0.4	V	$V_{SI} < V_{SI,low}$ $V_I > 5.5\text{ V}$ no external $R_{SO,ext}$	P_5.4.5
Sense output internal pull-up resistor to V_Q	$R_{SO,int}$	10	20	40	kΩ	–	P_5.4.7
Optional sense output external pull-up resistor to V_Q	$R_{SO,ext}$	20	–	–	kΩ	$V_I > 5.5\text{ V}$ $V_{SO} \leq 0.4\text{ V}$	P_5.4.8

Application information

5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

5.1 Application diagram

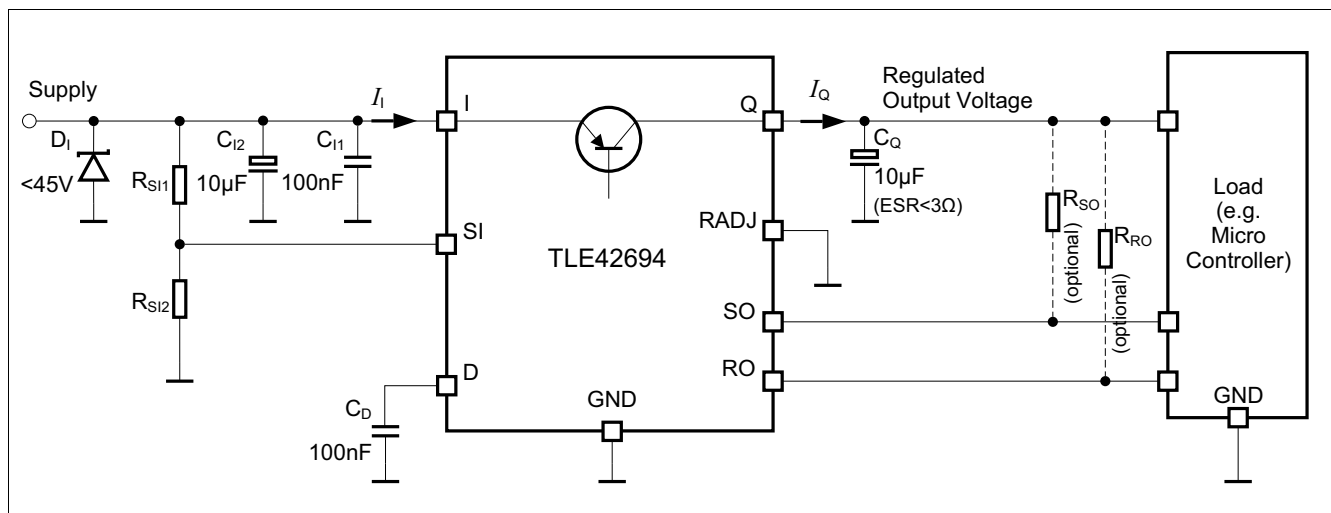


Figure 8 Application diagram with selecting default reset thresholds

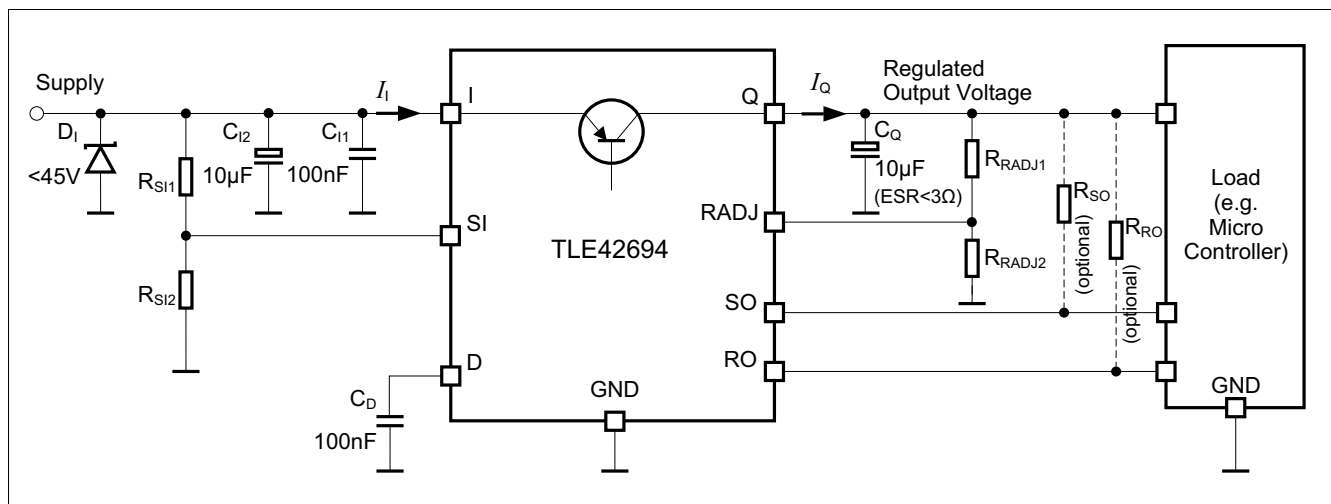


Figure 9 Application diagram with reset thresholds adjustment

Application information

5.2 Selection of external components

5.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 μ F to 470 μ F is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional range” on Page 9**. The graph **“Output capacitor series resistor ESR(C_Q) versus output current I_Q ” on Page 14** shows the stable operation range of the device.

TLE42694 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

Application information

5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- P_D : continuous power dissipation
- V_I : input voltage
- V_Q : output voltage
- I_Q : output current
- I_q : quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA, \max} = \frac{T_{j, \max} - T_a}{P_D} \quad (5.2)$$

with

- $T_{j, \max}$: maximum allowed junction temperature
- T_a : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **“Thermal resistance” on Page 10**.

Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 5 \text{ V}$$

$$I_Q = 50 \text{ mA}$$

$$T_a = 105 \text{ °C}$$

Calculation of $R_{thJA, \max}$:

$$\begin{aligned} P_D &= (V_I - V_Q) \cdot I_Q + V_I \cdot I_q \\ &= (13.5 \text{ V} - 5 \text{ V}) \cdot 50 \text{ mA} + 13.5 \text{ V} \cdot 8 \text{ mA} \\ &= 0.425 \text{ W} + 0.108 \text{ W} \\ &= 0.533 \text{ W} \\ R_{thJA, \max} &= (T_{j, \max} - T_a) / P_D \\ &= (150 \text{ °C} - 105 \text{ °C}) / 0.533 \text{ W} \\ &= 84.4 \text{ K/W} \end{aligned}$$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 84.4 K/W. By considering TLE42694E (PG-SSOP-14 EP package) and according to **“Thermal resistance” on Page 10**, at least 300 mm² heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

Application information

5.4 Reverse polarity protection

TLE42694 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 8** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shutdown circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

6 Package information

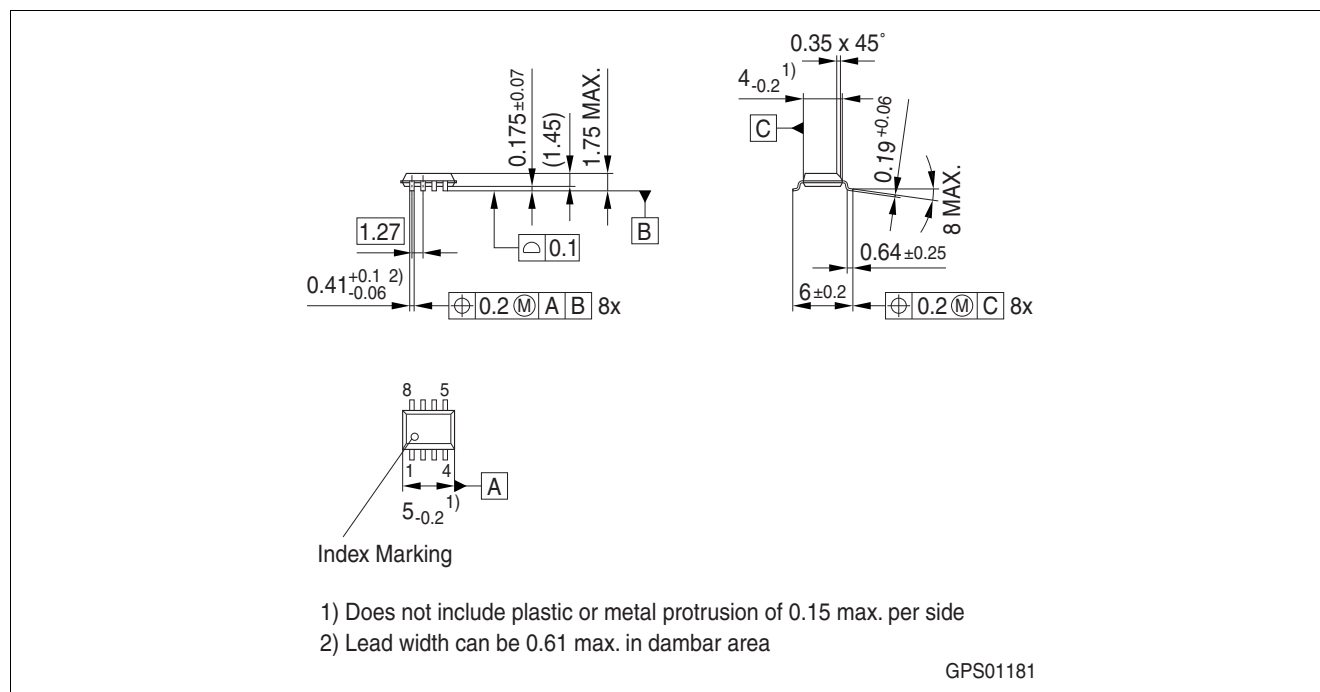


Figure 10 PG-DSO-8¹⁾

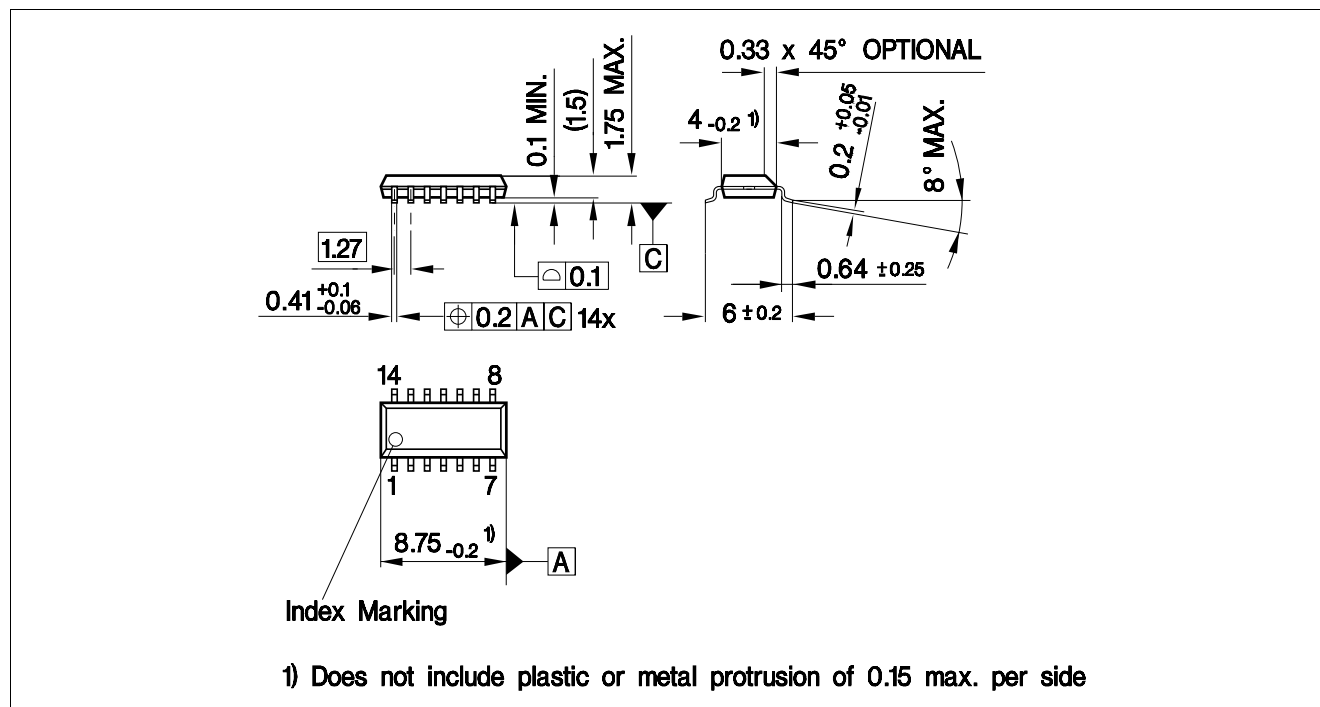
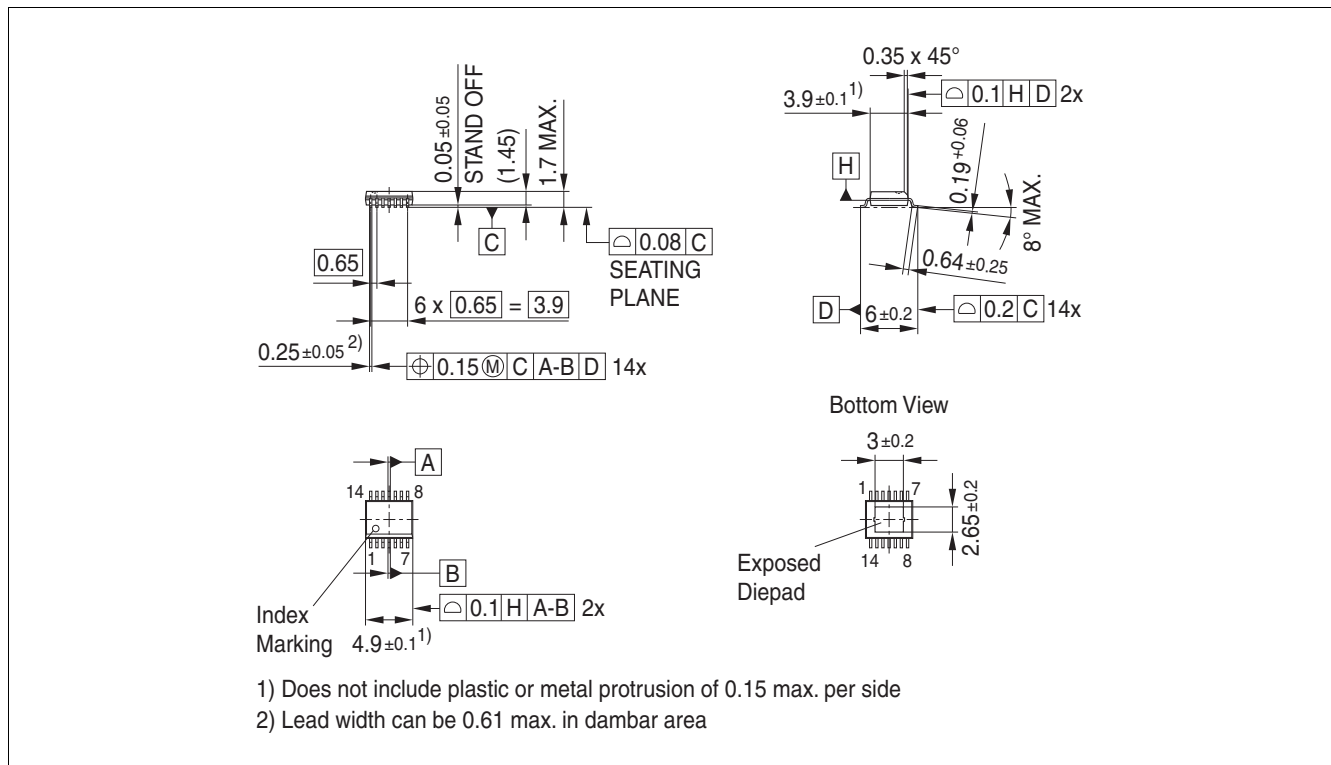


Figure 11 PG-DSO-14¹⁾

1) Dimensions in mm



Revision History

7 Revision History

Revision	Date	Changes
1.41	2019-04-30	Editorial change on page 5 and 6
1.4	2018-11-20	Updated Layout Updated package drawing "PG-DSO-14" Editorial changes
1.3	2014-07-03	"Application information" on Page 24 added PG-SSOP-14 EP package outline updated
1.2	2010-11-26	Updated PG-SSOP-14 Exposed Pad connection
1.1	2008-10-07	package version TLE42694E in PG-SSOP-14 exposed pad and all related information added In "Overview" on Page 2 package graphic for PG-SSOP-14 exposed pad and product name "TLE42694E" added In Chapter 2 "Pin assignment PG-SSOP-14 exposed pad" on Page 6 and "Pin definitions and functions PG-SSOP-14 exposed pad" on Page 6 added In "Thermal resistance" on Page 10 values for TLE42694E added In "Package Outlines" on Page 30 outlines for TLE42694E added
1.0	2008-08-25	initial version data sheet

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Edition 2019-04-30

Published by

**Infineon Technologies AG
81726 Munich, Germany**

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**Document reference
Z8F52698690**

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