Contents TDA7718N

Contents

1	Bloc	k circui	t diagram	. 6
2	Pin d	connect	tion and pin description	7
	2.1	Pin co	nnection	7
	2.2	Pin de	scription	7
3	Elec	trical sp	pecifications	9
	3.1	Therm	al data	9
	3.2	Absolu	ute maximum ratings	9
	3.3	Electri	cal characteristics	9
4	Desc	cription	of the audioprocessor	. 13
	4.1	Input s	stages	. 13
		4.1.1	Quasi-differential stereo input (QD1)	. 13
		4.1.2	Single-ended stereo input (SE1, SE2, SE3)	. 13
		4.1.3	Full-differential stereo input or single-ended input (FD1/QD2/SE4+SE5) 13
	4.2	Loudn	ess	. 15
		4.2.1	Loudness attenuation	. 15
		4.2.2	Peak frequency	. 15
		4.2.3	High frequency boost	. 16
		4.2.4	Flat mode	. 16
	4.3	SoftMu	ute	. 17
	4.4	SoftSt	ep volume	. 17
	4.5	Bass		. 18
		4.5.1	Bass attenuation	. 18
		4.5.2	Bass center frequency	. 18
		4.5.3	Quality factors	. 19
		4.5.4	DC mode	. 19
	4.6	Middle		. 20
		4.6.1	Middle attenuation	. 20
		4.6.2	Middle center frequency	. 20
		4.6.3	Quality factors	. 21
	4.7	Treble		. 21



7	Revis	ion his	tory	39
6	Packa	age info	ormation	38
	5.3	Data by	te specification	29
		5.2.3	Reset condition	27
		5.2.2	Transmission mode	27
		5.2.1	Receive mode	27
	5.2	I ² C bus	electrical characteristics	26
	5.1	Interfac	e protocol	26
5	I ² C bu	us spec	eification	26
	4.11	Audiop	rocessor testing	25
	4.10	DC offs	set detector	23
	4.9	Softste	p control	23
	4.8	Subwoo	ofer filter	22
		4.7.2	Center frequency	22
		4.7.1	Treble attenuation	21

List of tables TDA7718N

List of tables

Table 1.	Device summary	1
Table 2.	Pin description	7
Table 3.	Thermal data	9
Table 4.	Absolute maximum ratings	9
Table 5.	Electrical characteristics	9
Table 6.	I ² C bus electrical characteristics	. 26
Table 7.	Subaddress (receive mode)	. 28
Table 8.	Main selector (0)	. 29
Table 9.	Soft mute / others (4)	. 30
Table 10.	SoftStep I (5)	. 31
Table 11.	SoftStep II / DC detector (6)	. 32
Table 12.	Loudness (7)	. 33
Table 13.	Volume / output gain (8)	. 33
Table 14.	Treble filter (9)	. 34
Table 15.	Middle filter (10)	. 34
Table 16.	Bass filter (11)	. 35
Table 17.	Subwoofer / middle / bass (12)	. 35
Table 18.	Speaker attenuation (FL/FR/RL/RR/SWL/SWR) (13-18)	. 36
Table 19.	Testing audio processor 1 (19)	. 36
Table 20.	Testing audio processor 2 (20)	. 37
Table 21.	Testing audio processor 3 (21)	. 37
Table 22.	Document revision history	. 39



TDA7718N List of figures

List of figures

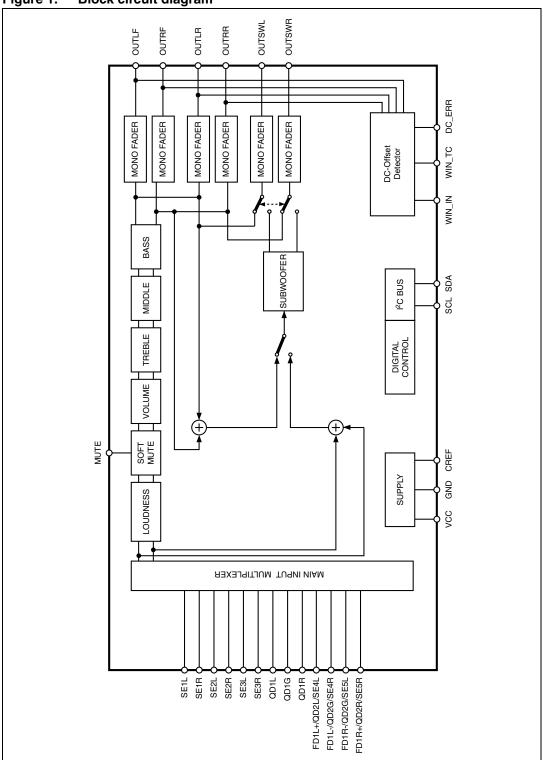
Figure 1.	Block circuit diagram	6
Figure 2.	Pin connection (top view)	
Figure 3.	FD / QD / SE block diagram	. 14
Figure 4.	Loudness attenuation @ fP = 400 Hz	. 15
Figure 5.	Loudness center frequencies @ attn. = 15 dB	. 15
Figure 6.	Loudness attenuation, f _c = 2.4 kHz	. 16
Figure 7.	SoftMute timing	. 17
Figure 8.	Bass control @ fC = 80 Hz, Q = 1	. 18
Figure 9.	Bass center frequencies @ gain = 14 dB, Q = 1	. 18
Figure 10.	Bass quality factors @ gain = 14 dB, f _C = 80 Hz	. 19
Figure 11.	Bass normal and DC mode @ gain = 14 dB, f _C = 80 Hz	
Figure 12.	Middle control @ fC = 1 kHz, Q = 1	. 20
Figure 13.	Middle center frequencies @ gain = 14 dB, Q = 1	
Figure 14.	Middle quality factors @ gain = 14 dB, f _C = 1 kHz	. 21
Figure 15.	Treble control @ fC = 17.5 kHz	
Figure 16.	Treble center frequencies @ gain = 14 dB	. 22
Figure 17.	Subwoofer cut frequencies	. 22
Figure 18.	DC offset detection circuit (simplified)	. 24
Figure 19.	Test circuit	
Figure 20.	I ² C bus interface protocol	
Figure 21.	I ² C bus data	
Figure 22.	TSSOP28 mechanical data and package dimensions	. 38



Block circuit diagram TDA7718N

1 Block circuit diagram



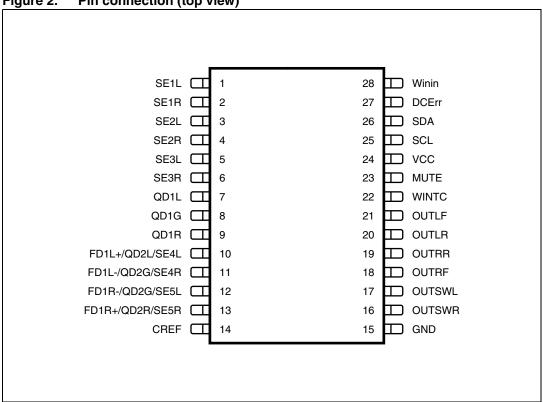


577

2 Pin connection and pin description

2.1 Pin connection





2.2 Pin description

Table 2. Pin description

No.	Pin name	Description	1/0
1	SE1L	Single-end input left	I
2	SE1R	Single-end input right	I
3	SE2L	Single-end input left	I
4	SE2R	Single-end input right	I
5	SE3L	Single-end input left	I
6	SE3R	Single-end input right	- 1
7	QD1L	quasi-differential stereo inputs left	I
8	QD1G	quasi-differential stereo inputs common	I
9	QD1R	quasi-differential stereo inputs right	I
10	FD1L+/QD2L/SE4L	Full differential + input left or quasi-differential left or single-end input left	I

477

Doc ID 16502 Rev 2

7/40

Table 2. Pin description (continued)

No.	Pin name	Description	I/O
11	FD1L-/QD2G/SE4R	Full differential - input left or quasi-differential ground or single-end input right	I
12	FD1R-/QD2G/SE5L	Full differential - input right or quasi-differential ground or single-end input left	I
13	FD1R+/QD2R/SE5R	Full differential + input right or quasi-differential right or single-end input right	I
14	CREF	Reference capacitor	0
15	GND	Ground	S
16	OUTSWR	Subwoofer right output	0
17	OUTSWL	Subwoofer left output	0
18	OUTRF	Front right output	0
19	OUTRR	Rear right output	0
20	OUTLR	Rear left output	0
21	OUTLF	Front left output	0
22	WinTC	DC offset detector filter output	0
23	MUTE	External mute pin	I
24	VCC	Supply	S
25	SCL	I ² C bus clock	I
26	SDA	I ² C bus data	I/O
27	DC_ERR	DC offset detector output	0
28	WIN_IN	DC offset detector input	I

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
R _{th-j amb}	Thermal resistance junction-to-ambient	114	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _S	Operating supply voltage	10.5	V
V _{in_max}	Maximum voltage for signal input pins	7	V
T _{amb}	Operating ambient temperature	-40 to 85	°C
T _{stg}	Storage temperature range	-55 to 150	°C

3.3 Electrical characteristics

 V_S = 8.5 V; T_{amb} = 25 °C; R_L = 10 k Ω ; all gains = 0 dB; f = 1 kHz; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Supply						
V _s	Supply voltage	-	7.5	8.5	10	V
Is	Supply current	-	23	29	35	mA
Input sele	ector					
R _{in}	Input resistance	All single ended inputs	70	100	130	kΩ
V _{CL}	Clipping level	Input gain = 0 dB	2	-	-	V_{RMS}
S _{IN}	Input separation	-	-	95	-	dB
Differenti	ial stereo inputs					
R _{in}	Input resistance	Differential	70	100	-	kΩ
CMRR	Common mode rejection ratio for	V _{CM} = 1 V _{RMS} @ 1 kHz	44	60	-	dB
OWINH	main source	V _{CM =} 1 V _{RMS} @ 10 kHz	44	60	-	dB
e _{No}	Output noise @ speaker outputs	20 Hz - 20 kHz, A-weighted; all stages 0 dB	-	12	22	μV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit		
Loudness control								
A _{MAX}	Max attenuation	-	14	15	16	dB		
A _{STEP}	Step resolution	-	0.5	1	1.5	dB		
		f _{P1}	-	400	-	Hz		
f _{Peak}	Peak frequency	f _{P2}	-	800	-	Hz		
		f _{P3}	-	14 15 16 0.5 1 1.5 - 400 - - 800 - - 2400 - 22 23 24 - -31 -30 0.5 1 1.5 0.75 0 +0.75 - - 2 -3 0.1 3 -5 0.5 5 80 100 - 0.35 0.48 0.65 0.7 0.96 1.3 5.6 7.6 9.6 12.3 15.3 18.3 - - 1 2.5 - - 3 3.3 3.6 - 60 - - 80 - - 100 - - 200 - - 1.25 - - 1.5 - - 1.5 - - 2	Hz			
Volume c	ontrol							
G _{MAX}	Max gain	-	22	23	24	dB		
A _{MAX}	Max attenuation	-	-	-31	-30	dB		
A _{STEP}	Step resolution	-	0.5	1	1.5	dB		
E _A	Attenuation set error	-	-0.75	0	+0.75	dB		
E _T	Tracking error	-	-	-	2	dB		
W	DC atoms	Adjacent attenuation steps	-3	0.1	3	mV		
V_{DC}	DC steps	From 0 dB to G _{MIN}	-5	0.5	5	mV		
Soft mute	•							
A _{MUTE}	Mute attenuation	-	80	100	-	dB		
	Delay time	T1	0.35	0.48	0.65	ms		
		T2	0.7	0.96	1.3	ms		
		Т3	5.6	7.6	9.6	ms		
		T4	12.3	15.3	18.3	ms		
V _{TH Low}	Low threshold for SM pin	-	-	-	1	٧		
V _{TH High}	High threshold for SM pin	-	2.5	-	-	٧		
R _{PU}	Internal pull-up resistor	-	32	45	58	kΩ		
V _{PU}	Internal pull-up voltage	-	3	3.3	3.6	٧		
Bass con	trol							
		f _{C1}	-	60	-	Hz		
- -	0	f _{C2}	-	80	-	Hz		
Fc	Center frequency	f _{C3}	-	100	16 1.5 24 -30 1.5 +0.75 2 3 5 - 0.65 1.3 9.6 18.3 1 - 58 3.6	Hz		
		f _{C4}	-	200	-	Hz		
		Q ₁	-	1	-	-		
0	Quality factor	Q_2	-	1.25	-	•		
Q _{BASS}	Quality factor	Q_3	-	1.5	-	•		
		Q ₄	-	2	-	-		
C _{RANGE}	Control range	-	±14	±15	±16	dB		
A _{STEP}	Step resolution	-	0.5	1	1.5	dB		
DC	Bass-DC-gain	DC = off	-1	0	+1	dB		
DC _{GAIN}	Dass-DO-yaiii	$DC = on, gain = \pm 15 dB$	±4.3	±4.7	16 1.5 24 -30 1.5 +0.75 2 3 5 - 0.65 1.3 9.6 18.3 1 - 58 3.6	dB		

10/40 Doc ID 16502 Rev 2

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Middle co	ontrol	•	•			
C _{RANGE}	Control range	-	±14	±15	±16	dB
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
		f _{C1}	-	500	-	Hz
	Contax fraguency	f _{C2}	- 500 1 1.5 2.5 0.75 1 1.25 - ±14 ±15 ±16 0.5 1 1.5 - 10 12.5 15 17.5 - 14 15 16 - 79 -74 0.5 1 1.5	-	kHz	
f _c	Center frequency	f _{C3}	-	1.5	-	kHz
		f _{C4}	-	±14 ±15 ±16 0.5 1 1.5 - 500 - - 1 - - 1.5 - - 2.5 - - 0.75 - - 1 - - 1.25 - ±14 ±15 ±16 0.5 1 1.5 - 10 - - 12.5 - - 15 - - 17.5 - 14 15 16 79 -74	kHz	
		Q ₁	-	0.75	-	-
Q _{MIDDLE}	Quality factor	Q_2	-	1	-	-
	Clipping level Step resolution	Q_3	-	1.25	-	-
Treble co	ntrol					
C _{RANGE}	Clipping level	-	±14	±15	±16	dB
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
		f _{C1}	-	10	-	kHz
Speaker at	Center frequency	f _{C2}	-	12.5	-	kHz
		f _{C3}	-	15	-	kHz
		f _{C4}	-	17.5	-	kHz
Speaker a	attenuators					
G _{MAX}	Max gain	-	14	15	16	dB
A _{MAX}	Max attenuation	-	-	-79	-74	dB
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
A _{MUTE}	Mute attenuation	-	80	90	-	dB
E _E	Attenuation set error	-	-	-	2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-	0.1	5	mV
Audio ou	tputs					
V	Clipping level	d = 0.3 %; byte8_D6=1	2	-	-	V _{RMS}
V CL	Clipping level	d = 1 %; byte8_D6=0	2.2	-	-	V _{RMS}
R _{OUT}	Output impedance	-	-	30	100	Ω
R _L	Output load resistance	-	2	-	-	kΩ
CL	Output load capacitor	-	-	-	10	nF
V_{DC}	DC voltage level	-	3.8	4.0	4.2	V
Subwoof	er lowpass					
		f _{LP1}	-	55	-	Hz
f	Lownson corner frequency	f _{LP2}	-	85	-	Hz
Treble con Crange Astep fc Speaker at Gmax Amax Astep Amute Ee Voc Audio outp Vcl Rout Rl Cl Vdc Subwoofer	Lowpass corner frequency	f _{LP3}	-	120	-	Hz
		f _{LP4}	-	160	-	Hz



Doc ID 16502 Rev 2

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
DC offset	detection circuit		•			
		V1	±10	±25	±40	mV
W	Zoro comp window cizo	V2	±30	±50	±70	mV
v _{th}	Zero comp. window size	V3	±50	±75	±100	mV
V _{th} Z t _{sp} M I _{CHDCErr} E I _{DISDCErr} E V _{OutH} E General e _{NO} C S/N S D E		V4	±70	±100	±130	mV
		-	2	11	30	μs
t _{sp}	Max rejected spike length	-	5	22	50	μs
		-	10	33	70	μs
		-	15	44	90	μs
I _{CHDCErr}	DCErr charge current	-	2	5	8	μΑ
I _{DISDCErr}	DCErr discharge current	-	4	5	9	mA
V_{OutH}	DCErr high voltage	-	3	3.3	3.6	V
V _{OutH}	DCErr low voltage	-	-	100	300	mV
General		<u>.</u>				
•	Output poins	BW=20 Hz to 20 kHz A- Weighted, all gain = 0 dB	-	12	22	μV
eNO	Output noise	BW=20 Hz - 20 kHz A- Weighted, Output muted	-	7	12	μV
S/N	Signal to noise ratio	all gain = 0 dB, A-weighted; $V_0 = 2 V_{RMS}$	98	104	-	dB
D	Distortion	V _{IN} =1 V _{RMS} ; all stages 0 dB	-	0.01	0.1	%
S _C	Channel separation left/right	-	-	90	-	dB

4 Description of the audioprocessor

4.1 Input stages

One quasi-differential stereo input, one full-differential stereo input and maximum five single-ended inputs are available.

4.1.1 Quasi-differential stereo input (QD1)

The QD input is implemented as a buffered quasi-differential stereo stage with 100 k Ω input-impedance at each input. There is -3 dB attenuation at QD input stage.

4.1.2 Single-ended stereo input (SE1, SE2, SE3)

The input-impedance at each input is 100 k Ω and the attenuation is fixed to -3 dB for incoming signals.

4.1.3 Full-differential stereo input or single-ended input (FD1/QD2/SE4+SE5)

This device provides a full-differential stereo input stage (FD1) or 2^{nd} quasi-differential stereo input stage. The full differential is a buffered full-differential stereo stage with $100~\text{k}\Omega$ input-impedance at each input. When using as QD2 application, it needs to connect the two QD2G pins together from external and the input impedance at QDG becomes $50~\text{k}\Omega$. This stage can be also configured as 2 single-ended stereo input stages (SE4 and SE5). The configuration is done with the input selector control bits and the selection of FD1 and QD2 is controlled by a separate bit. There is -3 dB attenuation at the input stage. *Figure 3* shows the block diagram of this input stage.

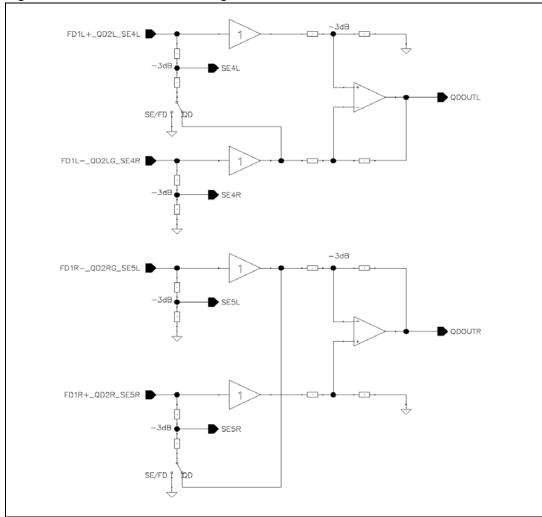


Figure 3. FD / QD / SE block diagram

57

4.2 Loudness

There are four parameters programmable in the loudness stage.

4.2.1 Loudness attenuation

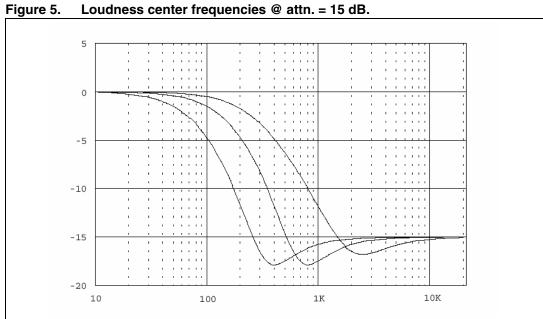
Figure 4 shows the attenuation as a function of frequency at $f_P = 400$ Hz.

5 0 -5 -10 -15 -20 10K 10 100 1K

Figure 4. Loudness attenuation @ fp = 400 Hz.

4.2.2 **Peak frequency**

Figure 5 shows the four possible peak-frequencies at 400, 800 and 2400 Hz.



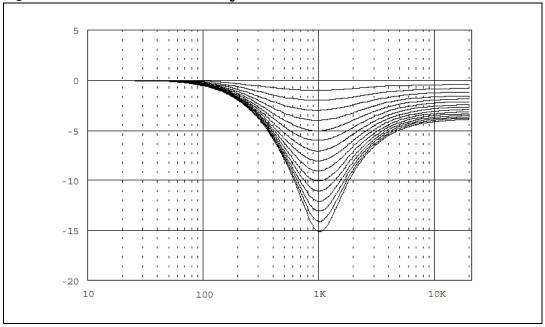
Doc ID 16502 Rev 2

15/40

4.2.3 High frequency boost

Figure 6 shows the different Loudness shapes in low and high frequency boost.

Figure 6. Loudness attenuation, $f_c = 2.4 \text{ kHz}$



4.2.4 Flat mode

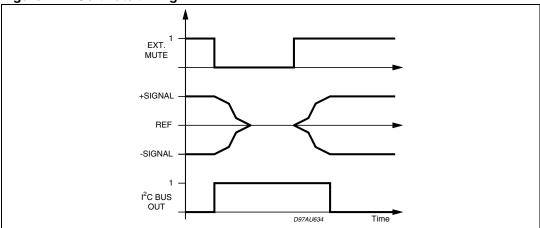
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

4.3 SoftMute

The digitally controlled SoftMute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the SoftMute pin or by the I^2C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 7*).

For timing purposes the bit 0 of the I²C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 7. SoftMute timing



Note:

Please notice that a started mute-action is always terminated and could not be interrupted by a change of the mute –signal.

4.4 SoftStep volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC-offset before the volume-stage or the sudden change of the envelope of the audio signal. With the SoftStep-feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable as 5 ms or 10 ms. The SoftStep control is described in detail in *Chapter 4.9*.

4.5 **Bass**

There are four parameters programmable in the bass stage:

4.5.1 **Bass attenuation**

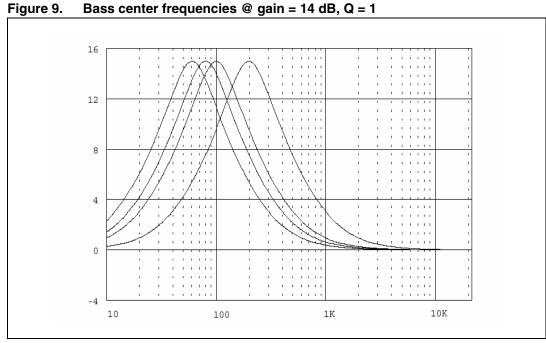
Figure 8 shows the attenuation as a function of frequency at a center frequency of 80 Hz.

Bass control @ f_C = 80 Hz, Q = 1 15.0 10.0 5.0 dΒ 0.0 -5.0-10.0 -15.010.0K Hz

Figure 8.

4.5.2 **Bass center frequency**

Figure 9 shows the four possible center frequencies 60, 80, 100 and 200 Hz.



4.5.3 **Quality factors**

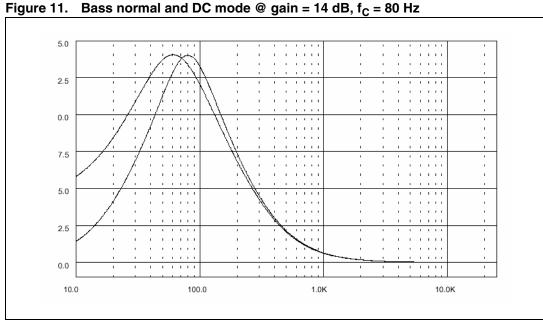
Figure 10 shows the four possible quality factors 1, 1.25, 1.5 and 2.

15.0 12.5 10.0 7.5 5.0 2.5 0.0 100.0 1.0K 10.0K 10.0

Figure 10. Bass quality factors @ gain = 14 dB, f_C = 80 Hz

4.5.4 DC mode

In this mode the DC-gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.



1. The center frequency, Q and DC-mode can be set fully independently.

577

4.6 Middle

There are three parameters programmable in the middle stage:

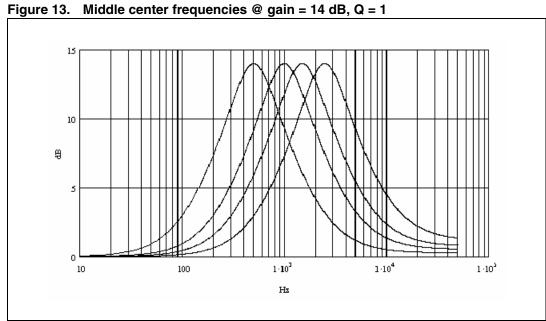
4.6.1 Middle attenuation

Figure 12 shows the attenuation as a function of frequency at a center frequency of 1 kHz.

Figure 12. Middle control @ $f_C = 1$ kHz, Q = 1 15.0 10.0 5.0 0.0 -5.0 -10.0 -15.0 10.0 100.0 1.0K 10.0K

4.6.2 Middle center frequency

Figure 13 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.



20/40 Doc ID 16502 Rev 2

4.6.3 **Quality factors**

Figure 14 shows the three possible quality factors 0.75, 1 and 1.25.

15 10 æ 1.10^3 10 100 1.104 1.104

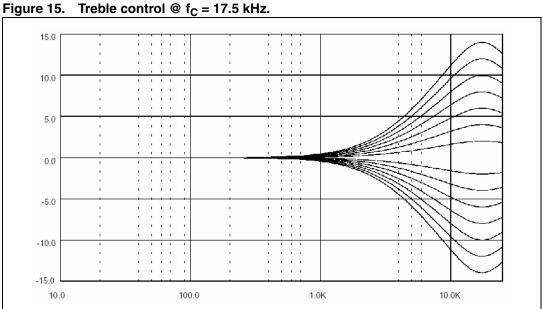
Figure 14. Middle quality factors @ gain = 14 dB, $f_C = 1$ kHz

4.7 **Treble**

There are two parameters programmable in the treble stage:

4.7.1 **Treble attenuation**

Figure 15 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.



4.7.2 Center frequency

Figure 16 shows the four possible center frequencies 10 k, 12.5 k, 15 k and 17.5 kHz.

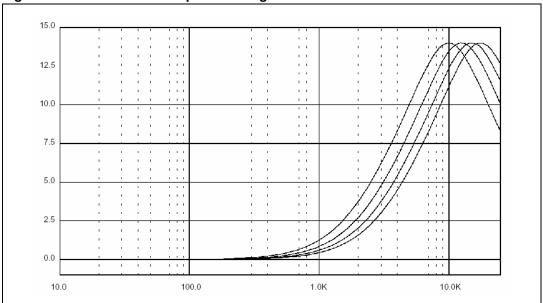


Figure 16. Treble center frequencies @ gain = 14 dB

4.8 Subwoofer filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (55 Hz / 85 Hz / 120 Hz / 160 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from bass filter output or output of input mux.

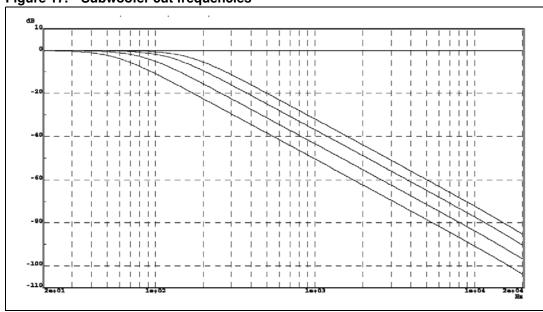


Figure 17. Subwoofer cut frequencies

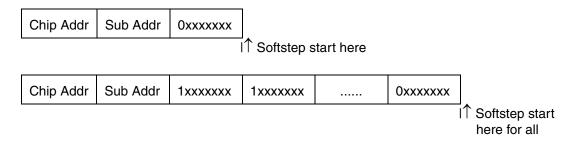
22/40 Doc ID 16502 Rev 2

4.9 Softstep control

In this device, the softstep function is available for volume, speaker, loudness, treble, middle and bass block. With softstep function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting gain setting of the block.

For each block, the softstep function is controlled by softstep on/off control bit in the control table. The softstep transient time selection (5 ms or 10 ms) is common for all blocks and it is controlled by softstep time control bit. The softstep operation of all blocks has a common centralized control. In this case, a new softstep operation can not be started before the completion previous softstep.

There are two different modes to activate the softstep operation. The softstep operation can be started right after I²C data sending, or the softstep can be activated in parallel after data sending of several different blocks. The two modes are controlled by the 'act bit' (it is normally bit7 of the byte.) of each byte. When act bit is '0', which means action, the softstep is activated right after the date byte is sent. When the act bit is '1', which means wait, the block goes to wait for softstep status. In this case, the block will wait for some other block to activate the operation. The softstep operation of all blocks in wait status will be done together with the block which activate the softstep. With this mode, all specific blocks can do the softstep in parallel. This avoids waiting when the softstep is operated one by one.



4.10 DC offset detector

Using the DC offset detection circuit (*Figure 18*) an offset voltage difference between the audio power amplifier and the APR's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the APR. The WinIn-input has an internal pull-up resistor connected to 5.5 V. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC-pin are implemented, with external capacitors introducing the same delay τ = 7.5 k Ω * C_{ext} as the AC-coupling between the APR and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

For electrical characteristics see *Chapter 3 on page 9*.

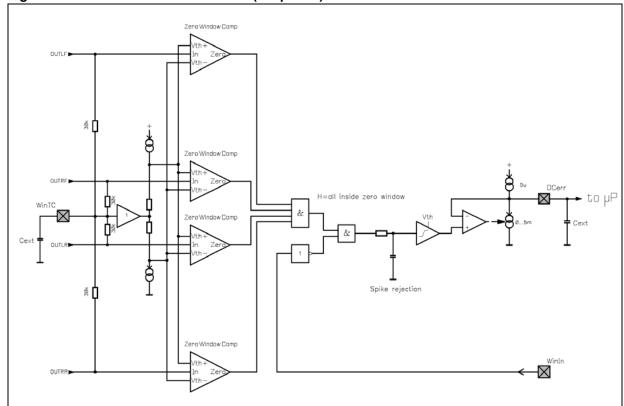
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

- a) Front and rear outputs are inside zero crossing windows.
- b) The Input voltage VWinIn is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

Doc ID 16502 Rev 2 23/40

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication.

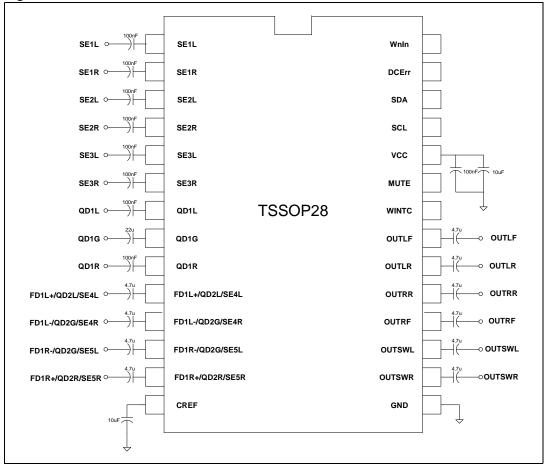
Figure 18. DC offset detection circuit (simplified)



4.11 Audioprocessor testing

In the test mode, which can be activated by setting bit D7 of the I^2C subaddress byte and bit D0 of the testing audioprocessor byte, several internal signals are available at the SE1L pin. In this mode, the input resistance of 100 k Ω is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.





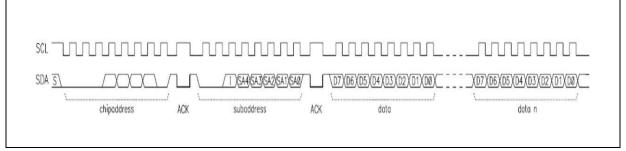
5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400 kbit/s
- 3.3 V logic compatible

Figure 20. I²C bus interface protocol



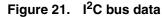
- 1. S = Start
- 2. ACK = Acknowledge

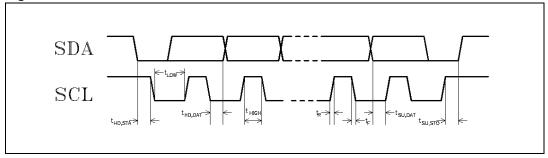
5.2 I²C bus electrical characteristics

Table 6. I²C bus electrical characteristics

Symbol	Parameter	Min	Max	Unit
f _{SCL}	SCL clock frequency	-	400	kHz
VIH	High level input voltage	2.4	-	V
VIL	Low level input voltage	-	0.8	V
t _{HD,STA}	Hold time for START	0.6	-	μs
t _{SU,STO}	Setup time for STOP	0.6	-	μs
t _{LOW}	Low period for SCL clock	1.3	-	μs
t _{HIGH}	High period for SCL clock	0.6	-	μs
t _F	Fall time for SCL/SDA	-	300	ns
t _R	Rise time for SCL/SDA	-	300	ns
t _{HD,DAT}	Data hold time	0	-	ns
t _{SU,DAT}	Data setup time	100	-	ns

26/40 Doc ID 16502 Rev 2





5.2.1 Receive mode

9	- 1	Λ	\cap	\cap	1	Λ	\cap	R/W	ACK	TS	Y	ΔΙ	Δ1	Δα	Δ2	Δ1	$\Delta \cap$	ACK	$D\Delta T\Delta$	ACK	P
9	٠,	U	U	U		U	0	1 1/ V V	AOIN	10		/\i	$^{-}$	70	72		70	AOIN	חחם	AOI	

S = Start

 $R/W = "0" -> Receive Mode (Chip can be programmed by <math>\mu P$)

"1" -> Transmission Mode (Data could be received by μP)

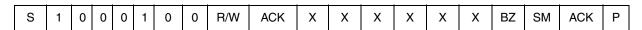
ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

5.2.2 Transmission mode



SM = Soft mute activated for main channel

BZ = Softstep Busy ('0' = Busy)

X = Not used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

5.2.3 Reset condition

A Power-On-Reset is invoked if the supply voltage is below than 3.5 V. After that the registers are initialized to the default data written in following tables.

Table 7. Subaddress (receive mode)

MSB							LSB	
12	l1	10	A 4	А3	A2	A 1	Α0	Function
								Testing mode
0 1	-	-	-	-	-	-	-	Off On
-	х	-	-	-	-	-	-	Not used
-	-	0	-	-	-	-	-	Auto increment mode Off On
-	-	-	0	0	0	0	0	Main selector
-	-	ı	0	0	0	0	1	Not used
-	-	-	0	0	0	1	0	Not used
-	-	-	0	0	0	1	1	Not used
-	-	-	0	0	1	0	0	Soft mute / others
-	-	-	0	0	1	0	1	Soft step I
-	-	-	0	0	1	1	0	Soft step II / DC-detector
-	-	-	0	0	1	1	1	Loudness
-	-	-	0	1	0	0	0	Volume / output gain
-	-	-	0	1	0	0	1	Treble
-	-	-	0	1	0	1	0	Middle
-	-	-	0	1	0	1	1	Bass
-	-	-	0	1	1	0	0	Subwoofer / middle / bass
-	-	-	0	1	1	0	1	Speaker attenuator left front
-	-	-	0	1	1	1	0	Speaker attenuator right front
-	-	-	0	1	1	1	1	Speaker attenuator left rear
-	-	-	1	0	0	0	0	Speaker attenuator right rear
-	-	-	1	0	0	0	1	Subwoofer attenuator left
-	-	-	1	0	0	1	0	Subwoofer attenuator right
-	-	-	1	0	0	1	1	Testing audio processor 1
-	-	-	1	0	1	0	0	Testing audio processor 2
-	-	-	1	0	1	0	1	Testing audio processor 3

5.3 Data byte specification

Table 8. Main selector (0)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Main source selector
					0	0	0	SE1
					0	0	1	SE3
					0	1	0	QD1
-	-	-	-	-	0	1	1	QD2 / FD1
					1	0	0	SE2
					1	0	1	SE4
					1	1	0	SE5
					1	1	1	Mute
								FD / QD2 selection
-	-	-	-	0	-	-	-	FD
				1				QD2
								Main source input gain select
-	-	-	0	-	-	-	-	0 dB
			1					3 dB
								Subwoofer flat
-	-	0	-	-	-	-	-	Off
		1						<u>On</u>
Х	х	-	-	-	-	-	-	Not used

Not used (1-3)

Table 9. Soft mute / others (4)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
-	-	-	-	-	-	-	0	Soft mute On Off
-	-	-	-	-	-	0	-	Pin influence for mute Pin and IIC IIC
-	-	-	-	0 0 1 1	0 1 0	-	-	Soft mute time 0.48 ms 0.96 ms 7.68 ms 15.36 ms
-	-	-	0	-	-	-	-	Subwoofer input source Input mux Bass output
-	-	0 1	-	-	-	-	-	Subwoofer enable (OUTSWL & OUTSWR) On Off
-	0 1	-	-	-	-	-	-	Fast charge On Off
0	-	-	-	-	-	-	-	Anti-alias filter On Off (bypass)

Table 10. SoftStep I (5)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
-	-	-	-	-	-	-	0 1	Loudness soft step On Off
-	-	-	-	-	-	0	-	Volume soft step On Off
-	-	-	-	-	0 1	-	-	Treble soft step On Off
-	-	-	-	0	-	-	-	Middle soft step On Off
-	-	-	0	-	-	-	-	Bass soft step On Off
-	-	0	-	-	-	-	-	Speaker LF soft step On Off
-	0	-	-	-	-	-	-	Speaker RF soft step On Off
0	-	-	-	-	-	-	-	Speaker LR soft step On Off

Table 11. SoftStep II / DC detector (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
-	-	-	-	-	-	-	0 1	Speaker RR soft step On Off
-	-	-	-	-	-	0	-	Subwoofer left soft step On Off
-	-	-	-	-	0	-	-	Subwoofer right soft step On Off
-	-	-	-	0	-	-	-	Soft step time 5 ms 10 ms
-	-	0 0 1 1	0 1 0	-	-	-	-	Zero-comparator window size ±100 mV ±75 mV ±50 mV ±25 mV
0 0 1 1	0 1 0	-	-	-	-	-	-	Spike rejection time constant 11 µs 22 µs 33 µs 44 µs

I²C bus specification

Table 12. Loudness (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Attenuation
				0	0	0	0	0 dB
				0	0	0	1	-1 dB
_	-	-	-	:	:	:	:	:
				1	1	1	0	<u>-14 dB</u>
				1	1	1	1	-15 dB
								Center frequency
		0	0					Flat
-	-	0	1	-	-	-	-	400 Hz
		1	0					800 Hz
		1	1					2400 Hz
								High boost
-	0	-	-	-	-	-	-	On
	1							<u>Off</u>
								Soft step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 13. Volume / output gain (8)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Gain/attenuation
		0	0	0	0	0	0	+0 dB
		0	0	0	0	0	1	+1 dB
		:	:	:	:	:	:	:
		0	0	1	1	1	1	+15 dB
		0	1	0	0	0	0	+16 dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	+23 dB
_	-	0	1	1	0	0	0	Not used
		:	:	:	:	:	:	:
		0	1	1	1	1	1	Not used
		1	0	0	0	0	0	-0 dB
		:	:	:	:	:	:	:
		1	0	1	1	1	1	-15 dB
		:	:	:	:	:	:	:
		1	1	1	1	1	1	-31 dB
								Output gain
-	0	-	-	-	-	-	-	1 dB
	1							<u>0 dB</u>
								Soft step action
0	-	-	-	-	-	-	-	Act
1								<u>Wait</u>

Doc ID 16502 Rev 2 33/40

Table 14. Treble filter (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	<u>+1 dB</u>
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Treble center frequency
	0	0						10.0 kHz
-	0	1	-	-	-	-	-	12.5 kHz
	1	0						15.0 kHz
	1	1						<u>17.5 kHz</u>
								Soft step action
0	-	-	-	-	-	-	-	Act
1								<u>Wait</u>

Table 15. Middle filter (10)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	<u>+1 dB</u>
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Middle Q factor
	0	0						0.75
-	0	1	-	-	-	-	-	1
	1	0						<u>1.25</u>
	1	1						Reserved
								Soft step action
0	-	-	-	-	-	-	-	Act
1								Wait

34/40 Doc ID 16502 Rev 2

Table 16. Bass filter (11)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Gain/attenuation
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			:	:	:	:	:	:
			0	1	1	1	0	-1 dB
-	-	-	0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	<u>+1 dB</u>
			:	:	:	:	:	:
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Bass Q factor
	0	0						1.0
-	0	1	-	-	-	-	-	1.25
	1	0						1.5
	1	1						2.0
								Soft step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 17. Subwoofer / middle / bass (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Subwoofer cut-off frequency
						0	0	55 Hz
-	-	-	-	-	-	0	1	85 Hz
						1	0	<u>120 Hz</u>
						1	1	160 Hz
								Subwoofer output phase
-	-	-	-	-	0	-	-	180 deg
					1			<u>0 deg</u>
								Middle center frequency
			0	0				500 Hz
-	-	-	0	1	-	-	-	1000 Hz
			1	0				1500 Hz
			1	1				2500 Hz
								Bass center frequency
	0	0						60 Hz
-	0	1	-	-	-	-	-	80 Hz
	1	0						100 Hz
	1	1						200 Hz
								Bass DC mode
0	-	-	-	-	-	-	-	On
1								<u>Off</u>

577

Table 18. Speaker attenuation (FL/FR/RL/RR/SWL/SWR) (13-18)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Gain/attenuation
	0	0	0	0	0	0	0	0 dB
	0	0	0	0	0	0	1	1 dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15 dB
-	0	0	1	0	0	0	0	-0 dB
	0	0	1	0	0	0	1	-1 dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-78 dB
	1	0	1	1	1	1	1	-79 dB
	1	1	х	х	х	х	х	<u>mute</u>
								Soft step action
0	-	-	-	-	-	-	-	Act
1								Wait

Table 19. Testing audio processor 1 (19)

MSB							LSB	- Function
D7	D6	D5	D4	D3	D2	D1	D0	- Function
								Audio processor testing mode
-	-	-	-	-	-	-	0	<u>Off</u>
							1	On
								Test multiplexer at SE1L (1)
			0	0	0	0		SSCLK
			0	0	0	1		REQ
			0	0	1	0		SMCLK
			0	0	1	1		DCDet Vth High
			0	1	0	0		DCDet Vth Low
_	_	_	0	1	0	1	_	IntZeroErr
			0	1	1	0		Ref5V5
			0	1	1	1		VGB1.95
			1	0	0	0		Clock200k
			1	0	0	1		SDCLK
			1	0	1	0		VrefDCO
								Clock fast mode (2)
-	-	0	-	-	-	-	-	On
		1						<u>Off</u>
								Clock source ⁽²⁾
-	0	-	-	-	-	-	-	External
	1							Internal (200 kHz)
								Attenuator gain clock control (2)
0	-	-	-	-	-	-	-	On
1								<u>Off</u>

^{1.} The control bit needs both I²C test mode on & sub-address test mode on.

47/

^{2.} The control bit does not depend on test mode.

Table 20. Testing audio processor 2 (20)

MSB			<u> </u>				LSB	Franction
D7	D6	D5	D4	D3	D2	D1	D0	- Function
								Test architecture (1)
-	-	-	-	-	-	-	0	Normal
							1	Split
								Oscillator clock (2)
-	-	-	-	-	-	0	-	400 kHz
						1		800 kHz
								Softstep curve (2)
-	-	-	-	-	0	-	-	S-Curve
					1			Linear curve
								Manual set busy signal (1)
			0	0				Auto
-	-	-	0	1	-	-	-	Auto
			1	0				0
			1	1				1
								Request for clk generator (1)
			0	0				Allow
-	-	-	0	1	-	-	-	Allow
			1	0				Stopped
			1	1				Stopped
								No DCO spike rejection ⁽¹⁾
-	-	0	-	-	-	-	-	On
		1						Off
Х	Х	-	-	-	-	-	-	Not used

^{1.} The control bit needs sub-address test mode on.

Table 21. Testing audio processor 3 (21)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Function
								Enable clock for FL/FR/RL/RR/SWL/SWR
-	-	-	-	-	-	-	0	On
							1	<u>Off</u>
								Enable clock for volume
-	-	-	-	-	-	0	-	On
						1		<u>Off</u>
								Enable clock for treble and bass
-	-	-	-	-	0	-	-	On
					1			<u>Off</u>
								Enable clock for loudness and middle
-	-	-	-	0	-	-	-	On
				1				Off
Х	х	Х	х	-	-	-	-	Not used

^{2.} The control bit does not depend on test mode.

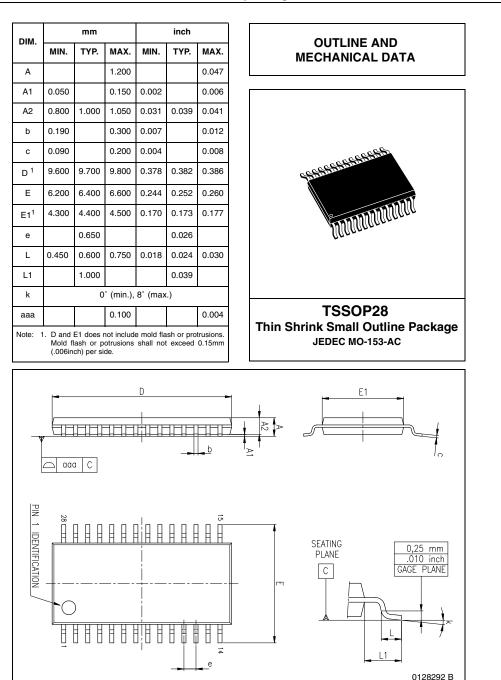
Package information TDA7718N

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>.

 $\mathsf{ECOPACK}^{(\! B\!)}$ is an ST trademark.

Figure 22. TSSOP28 mechanical data and package dimensions



38/40 Doc ID 16502 Rev 2

TDA7718N Revision history

7 Revision history

Table 22. Document revision history

Date	Revision	Changes
21-Oct-2009	1	Initial release.
16-Sept-2013	2	Updated Disclaimer

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Downloaded from **Arrow.com**.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries. Information in this document supersedes and replaces all information previously supplied. The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

40/40 Doc ID 16502 Rev 2

