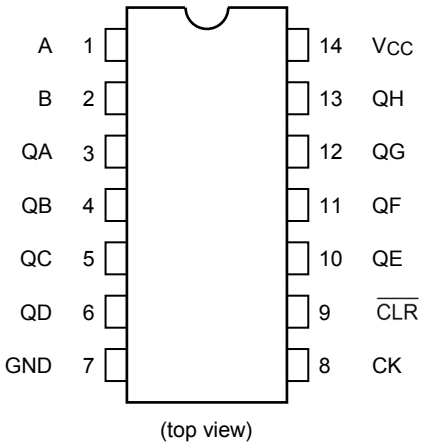
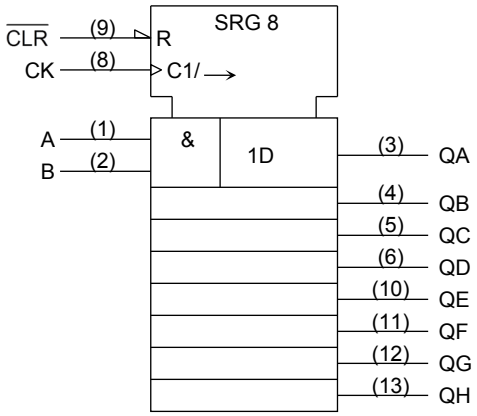
Pin Assignment



IEC Logic Symbol



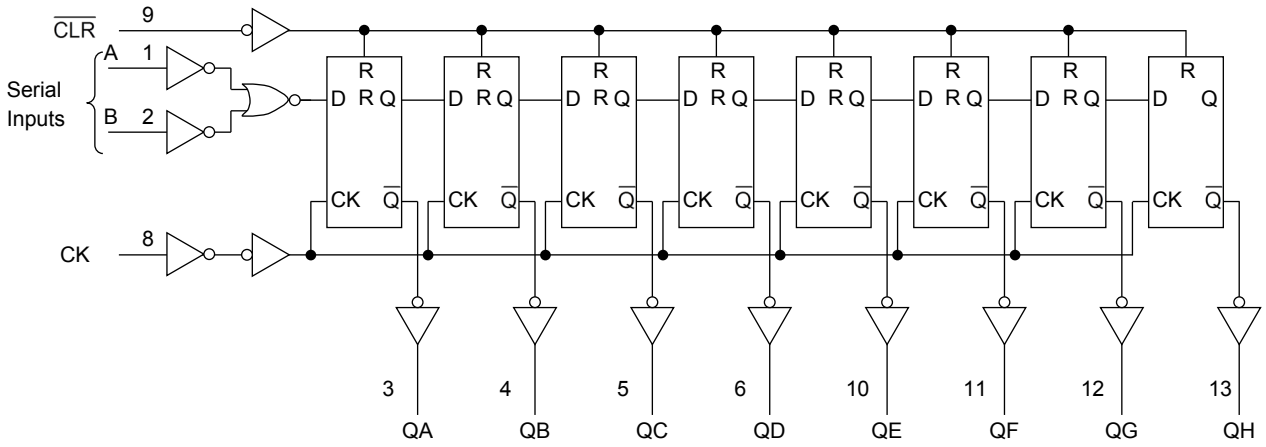
Truth Table

Inputs				Outputs			
$\overline{CLR}$	CK	Serial IN		QA	QB	⋯	QH
		A	B				
L	X	X	X	L	L	⋯	L
H	↓	X	X	No Change			
H	↑	L	X	L	QA_n	⋯	QG_n
H	↑	X	L	L	QA_n	⋯	QG_n
H	↑	H	H	H	QA_n	⋯	QG_n

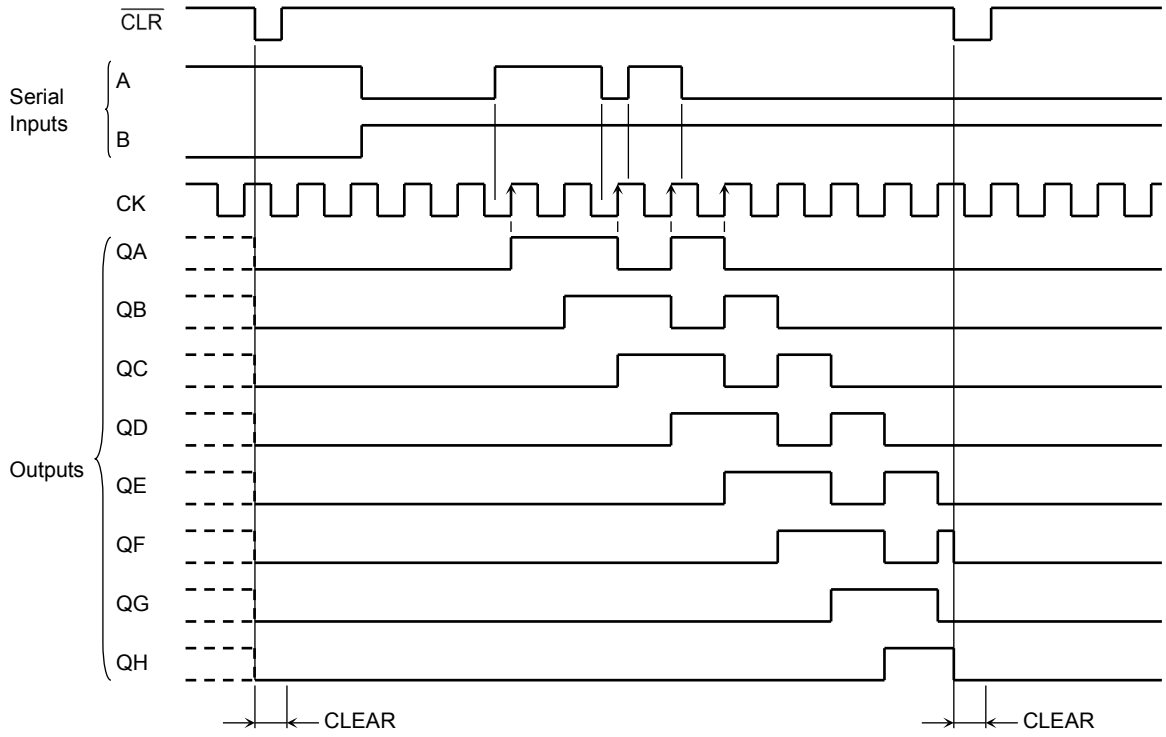
X: Don't care

QA_n to QG_n: The level of QA to QG, respectively, before the most recent positive edge of the clock.

System Diagram



Timing Chart



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C				Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max		Min	Max	
High-level input voltage	V_{IH}	—	2.0	1.50	—	—		1.50	—	V
			3.0 to 5.5	V_{CC} × 0.7	—	—		V_{CC} × 0.7	—	
Low-level input voltage	V_{IL}	—	2.0	—	—	0.50		—	0.50	V
			3.0 to 5.5	—	—	V_{CC} × 0.3		—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_{w\,(L)}$ $t_{w\,(H)}$	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum pulse width ($\overline{CLR}$)	$t_{w\,(L)}$	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum set-up time	t_s	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 4.5	6.0 4.5	ns
Minimum hold time	t_h	—	3.3 ± 0.3 5.0 ± 0.5	— —	0.0 1.0	0.0 1.0	ns
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	3.3 ± 0.3 5.0 ± 0.5	— —	2.5 2.5	2.5 2.5	ns

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	8.4	12.8	1.0	15.0	ns
				50	—	10.9	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.8	9.0	1.0	10.5	
				50	—	7.3	11.0	1.0	12.5	
Propagation delay time ($\overline{CLR}$-Q)	t_{pHL}	—	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	ns
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.2	8.6	1.0	10.0	
				50	—	6.7	10.6	1.0	12.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	80	125	—	65	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	125	175	—	105	—	
				50	85	115	—	75	—	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)			—	76	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

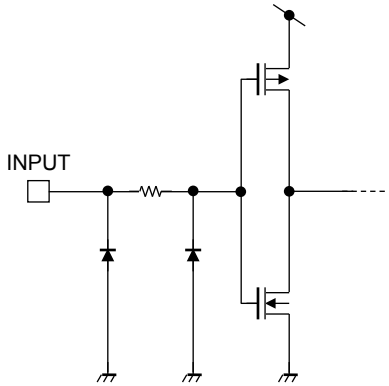
Average operating current can be obtained by the equation:

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V_{CC} (V)	Typ.	Max	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.5	−0.8	V
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

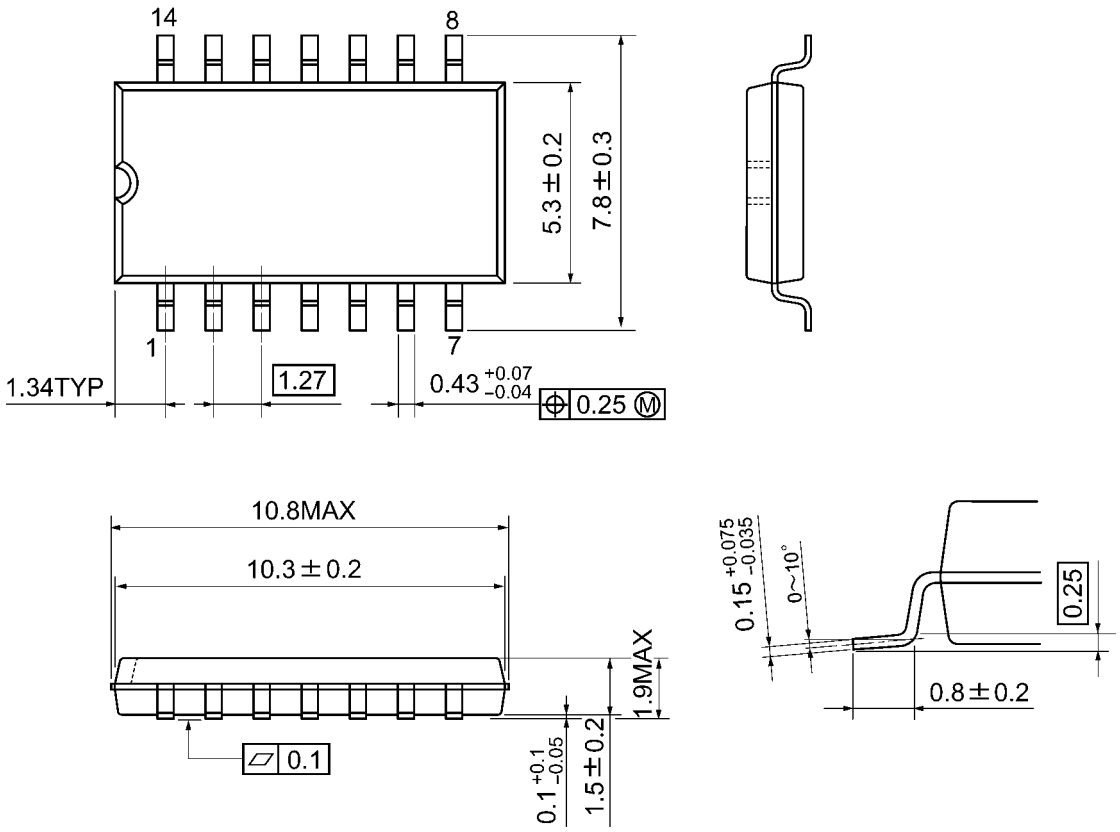
Input Equivalent Circuit



Package Dimensions

SOP14-P-300-1.27A

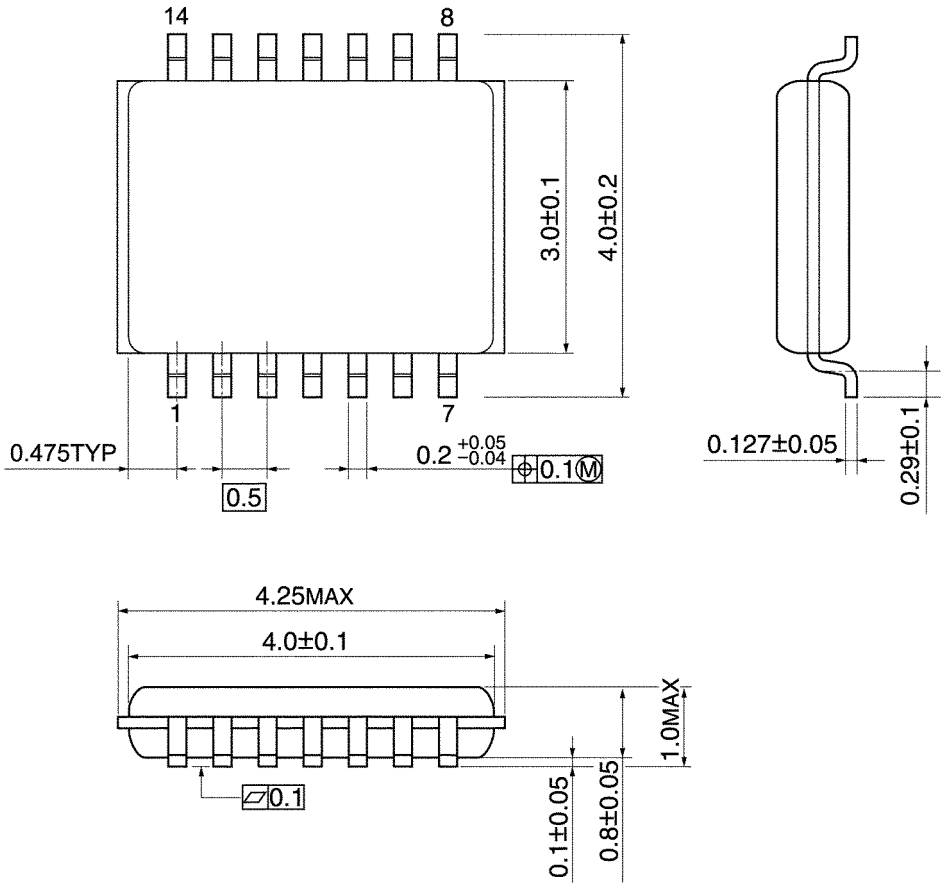
Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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