CONTENTS

1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified T_A = 25 °C

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Notes
Drain Peak Current(1)	I_{DPEAK}	Single pulse	1 – 3	5.0	A	STR-W6051S
				7.0		STR-W6052S
				7.5		STR-W6072S
				9.5		STR-W6053S
Maximum Switching Current(2)	I_{DMAX}	Single pulse Ta= –20 to 125°C	1 – 3	5.0	A	STR-W6051S
				7.0		STR-W6052S
				7.5		STR-W6072S
				9.5		STR-W6053S
Avalanche Energy(3)(4)	E_{AS}	I_{LPEAK}=2.0A	1 – 3	47	mJ	STR-W6051S
		I_{LPEAK}=2.3A		60		STR-W6072S
		I_{LPEAK}=2.3A		62		STR-W6052S
		I_{LPEAK}=2.7A		86		STR-W6053S
S/OCP Pin Voltage	V_{OCP}		3 – 5	− 2 to 6	V	
VCC Pin Voltage	V_{CC}		4 – 5	32	V	
FB/OLP Pin Voltage	V_{FB}		6 – 5	− 0.3 to 14	V	
FB/OLP Pin Sink Current	I_{FB}		6 – 5	1.0	mA	
BR Pin Voltage	V_{BR}		7 – 5	− 0.3 to 7	V	
BR Pin Sink Current	I_{BR}		7 – 5	1.0	mA	
MOSFET Power Dissipation(5)	P_{D1}	With infinite heatsink	1 – 3	22.3	W	STR-W6051S
				23.6		STR-W6052S
				25.8		STR-W6072S
				26.5		STR-W6053S
		Without heatsink	1 – 3	1.3	W	
Control Part Power Dissipation	P_{D2}	V_{CC}×I_{CC}	4 – 5	0.13	W	
Internal Frame Temperature in Operation	T_F		−	− 20 to 115	°C	
Operating Ambient Temperature	T_{OP}		−	− 20 to 115	°C	
Storage Temperature	T_{stg}		−	− 40 to 125	°C	
Junction Temperature	T_{ch}		−	150	°C	

(1) Refer to 3.3 MOSFET Safe Operating Area Curves.
(2) The maximum switching current is the drain current determined by the drive voltage of the IC and threshold voltage (V_{th}) of the MOSFET.
(3) Refer to Figure 3-2 Avalanche Energy Derating Coefficient Curve.
(4) Single pulse, V_{DD} = 99 V, L = 20 mH
(5) Refer to 3.2 Ta-P_{D1}curves.

2. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A = 25 °C, V_{CC} = 18 V

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Notes
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		4 – 5	13.8	15.3	16.8	V	
Operation Stop Voltage[1]	$V_{CC(OFF)}$		4 – 5	7.3	8.1	8.9	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	4 – 5	−	−	2.5	mA	
Startup Circuit Operation Voltage	$V_{ST(ON)}$		4 – 5	−	40	−	V	
Startup Current	$I_{STARTUP}$	V_{CC} = 13.5 V	4 – 5	− 3.9	− 2.5	− 1.1	mA	
Startup Current Biasing Threshold Voltage	$V_{CC(BIAS)}$	I_{CC} = − 100 µA	4 – 5	8.5	9.5	10.5	V	
Normal Operation								
Average Switching Frequency	$f_{OSC(AVG)}$		1 – 5	60	67	74	kHz	
Switching Frequency Modulation Deviation	Δf		1 – 5	−	5	−	kHz	
Maximum ON Duty	D_{MAX}		1 – 5	63	71	79	%	
Protection Function								
Leading Edge Blanking Time	t_{BW}		−	−	390	−	ns	
OCP Compensation Coefficient	DPC		−	−	18	−	mV/µs	
OCP Compensation ON Duty	D_{DPC}		−	−	36	−	%	
OCP Threshold Voltage at Zero ON Duty	$V_{OCP(L)}$		3 – 5	0.70	0.78	0.86	V	
OCP Threshold Voltage at 36% ON Duty	$V_{OCP(H)}$	V_{CC} = 32 V	3 – 5	0.79	0.88	0.97	V	
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	6 – 5	− 340	− 230	− 150	µA	
Minimum Feedback Current	$I_{FB(MIN)}$		6 – 5	− 30	− 15	− 7	µA	
FB/OLP pin Oscillation Stop Threshold Voltage	$V_{FB(STB)}$		6 – 5	0.85	0.95	1.05	V	
OLP Threshold Voltage	$V_{FB(OLP)}$		6 – 5	7.3	8.1	8.9	V	
OLP Operation Current	$I_{CC(OLP)}$	V_{CC} = 12 V	4 – 5	−	300	−	µA	
OLP Delay Time	t_{OLP}		6 – 5	54	68	82	ms	
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		6 – 5	11	12.8	14	V	
Brown-In Threshold Voltage	$V_{BR(IN)}$	V_{CC} = 32 V	7 – 5	5.2	5.6	6	V	
Brown-Out Threshold Voltage	$V_{BR(OUT)}$	V_{CC} = 32 V	7 – 5	4.45	4.8	5.15	V	
BR Pin Clamp Voltage	$V_{BR(CLAMP)}$	V_{CC} = 32 V	7 – 5	6	6.4	7	V	
BR Function Disabling Threshold	$V_{BR(DIS)}$	V_{CC} = 32 V	7 – 5	0.3	0.48	0.7	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		4 – 5	26	29	32	V	
Thermal Shutdown Operating Temperature	$T_{j(TSD)}$		−	130	−	−	°C	

[1] $V_{CC(BIAS)} > V_{CC(OFF)}$ always.

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Notes
MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}		8 – 1	650	–	–	V	STR-W605×S
				800	–	–		STR-W6072S
Drain Leakage Current	I_{DSS}		8 – 1	–	–	300	μA	
On Resistance	$R_{DS(ON)}$		8 – 1	–	–	3.95	Ω	STR-W6051S
				–	–	3.6		STR-W6072S
				–	–	2.8		STR-W6052S
				–	–	1.9		STR-W6053S
Switching Time	t_f		8 – 1	–	–	250	ns	
Thermal Resistance								
Channel to Frame Thermal Resistance[(2)]	θ_{ch-F}		–	–	–	2.63	°C/W	STR-W6051S
				–	–	2.26		STR-W6052S
				–	–	2.03		STR-W6072S
				–	–	1.95		STR-W6053S

(2) The thermal resistance between the channels of the MOSFET and the internal frame.

3. Performance Curves

3.1 Derating Curves

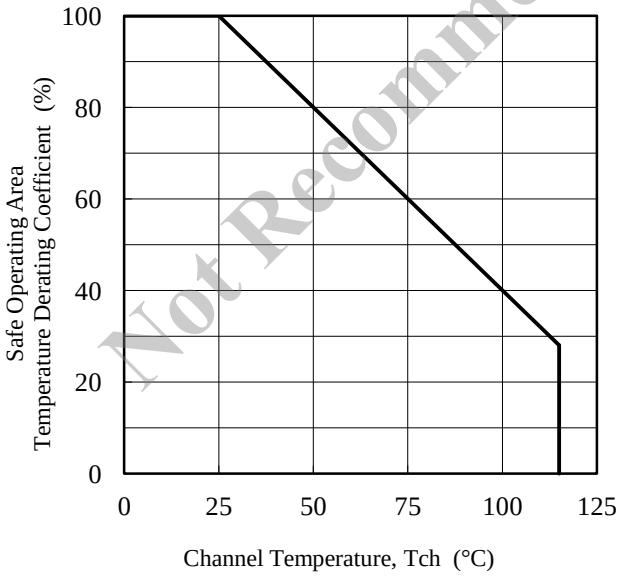


Figure 3-1 SOA Temperature Derating Coefficient Curve

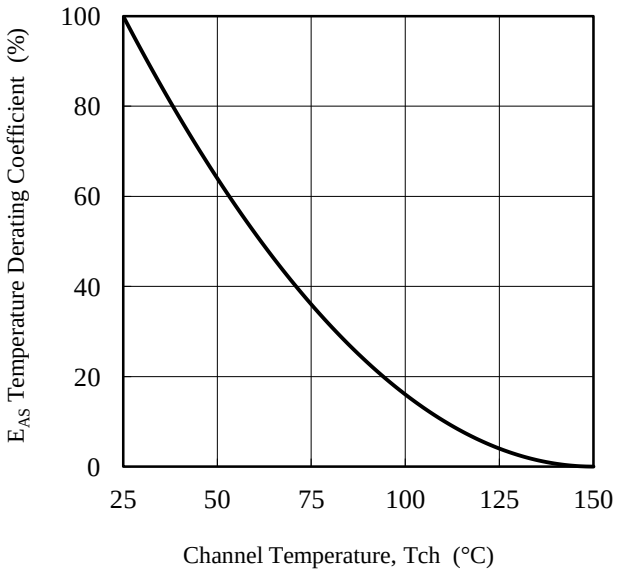
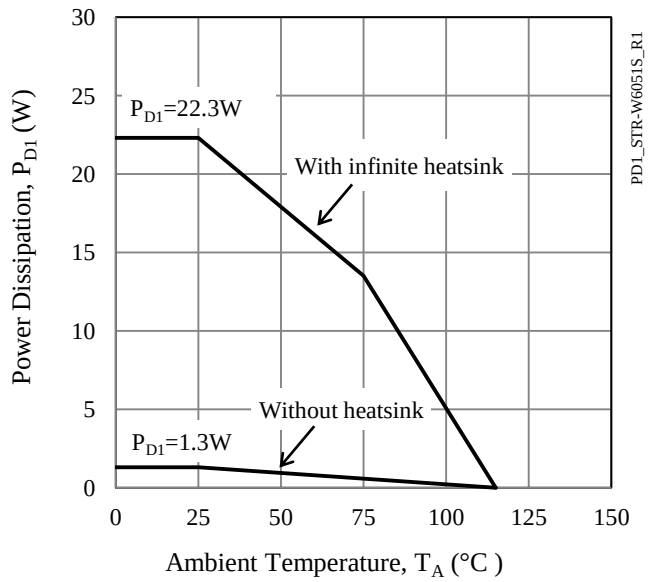


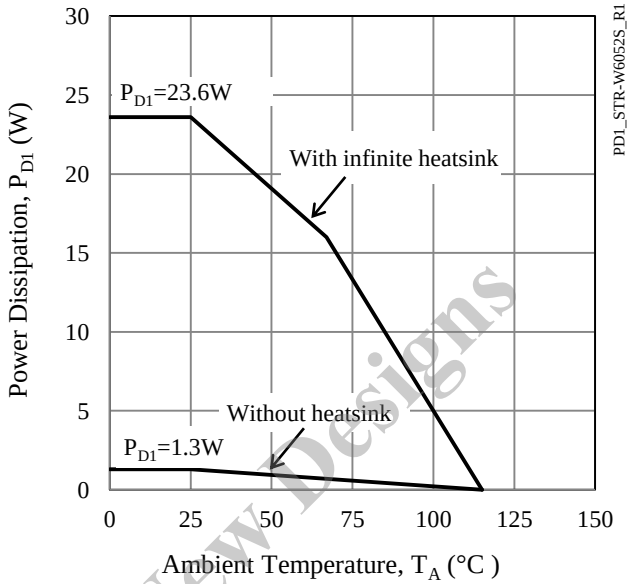
Figure 3-2 Avalanche Energy Derating Coefficient Curve

3.2 Ambient Temperature versus Power Dissipation Curves

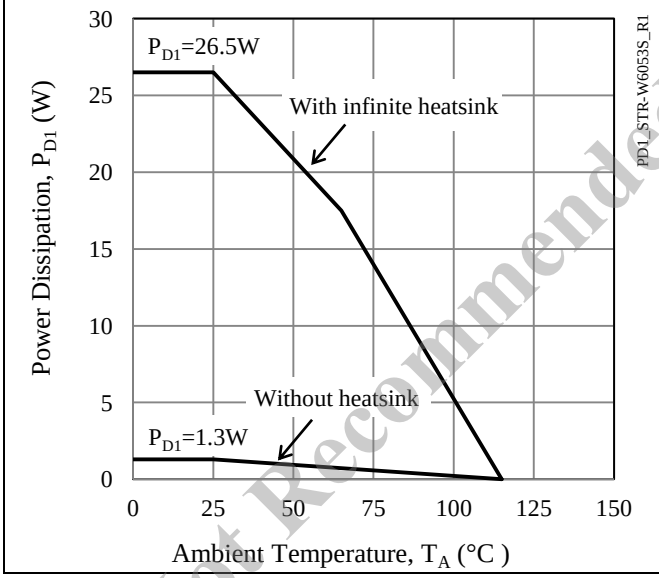
• **STR-W6051S**



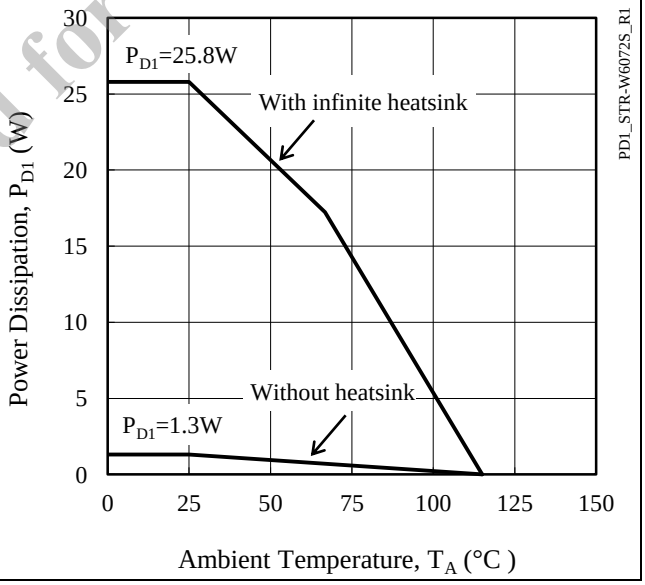
• **STR-W6052S**



• **STR-W6053S**



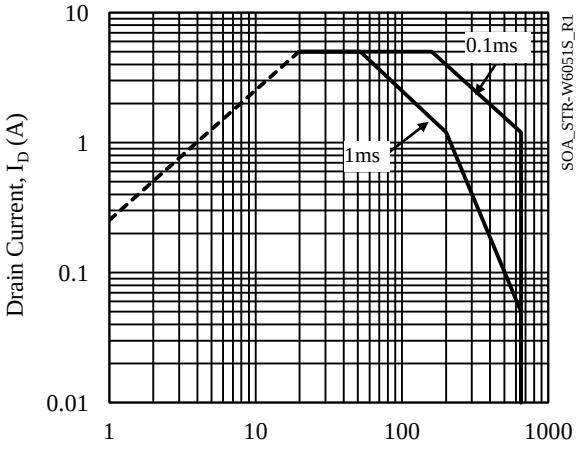
• **STR-W6072S**



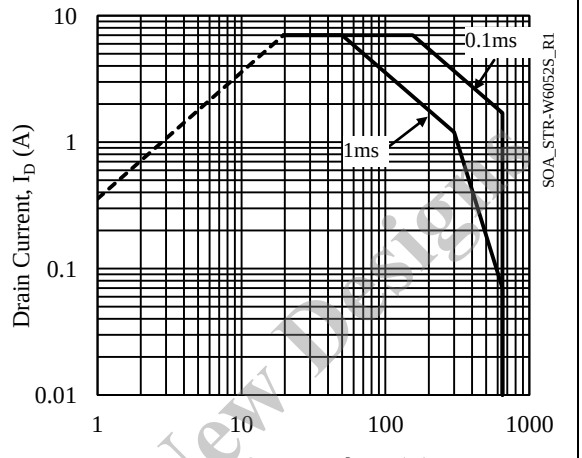
3.3 MOSFET Safe Operating Area Curves

- When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 3-1.
- The broken line in the safe operating area curve is the drain current curve limited by on-resistance.
- Unless otherwise specified, T_A = 25 °C, Single pulse

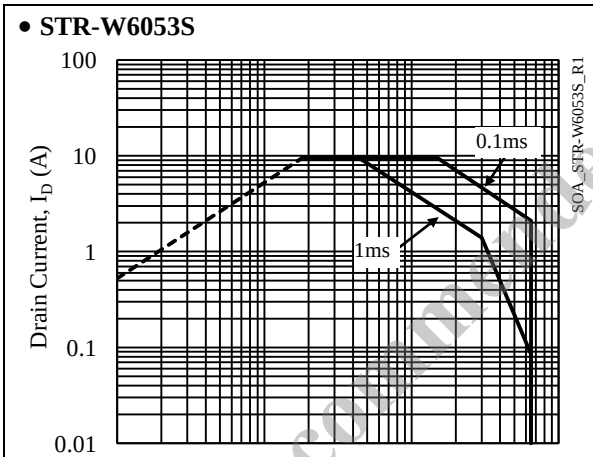
• STR-W6051S



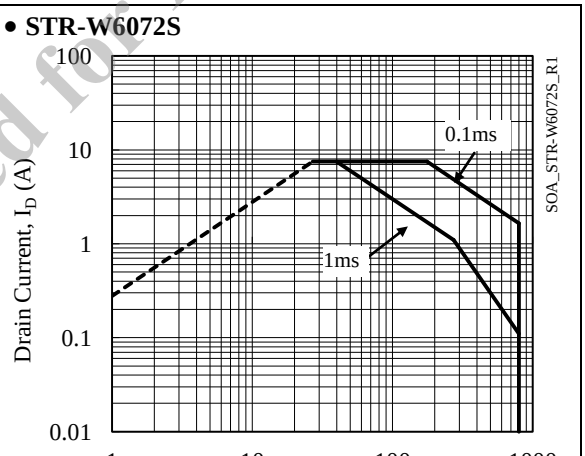
• STR-W6052S



• STR-W6053S

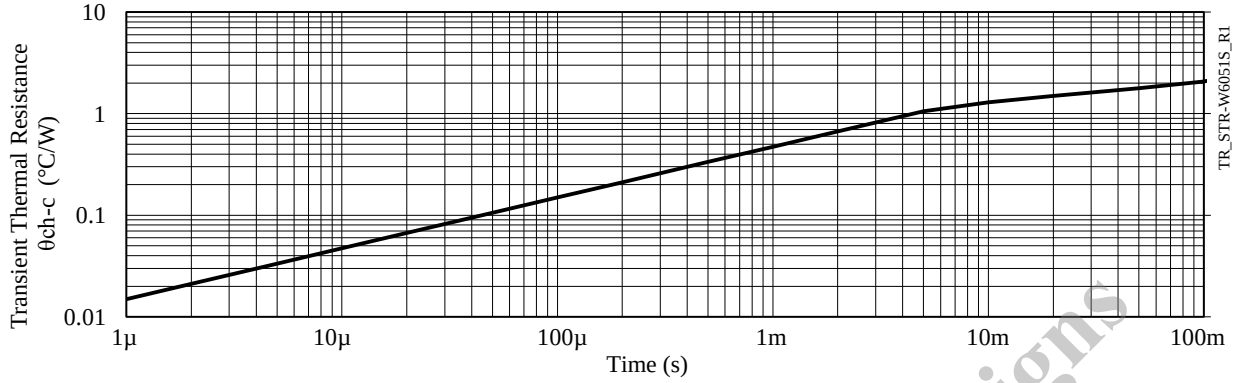


• STR-W6072S

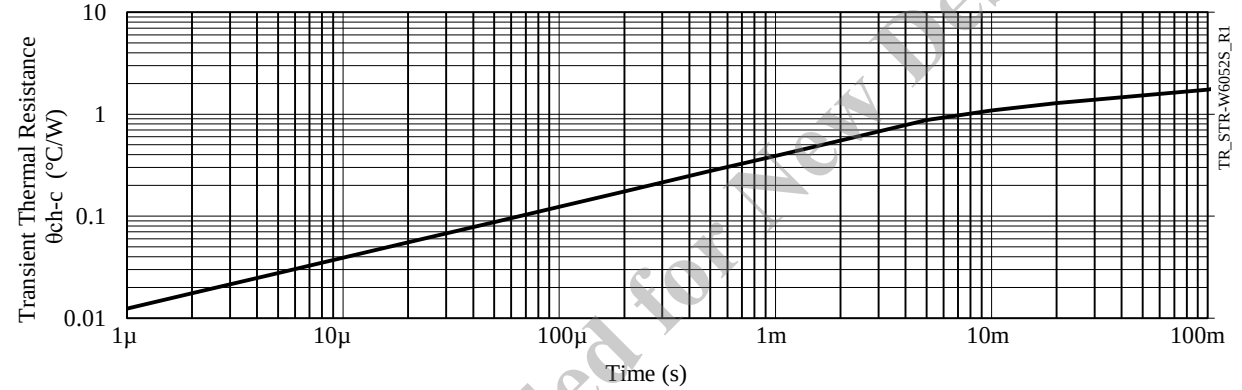


3.4 Transient Thermal Resistance Curves

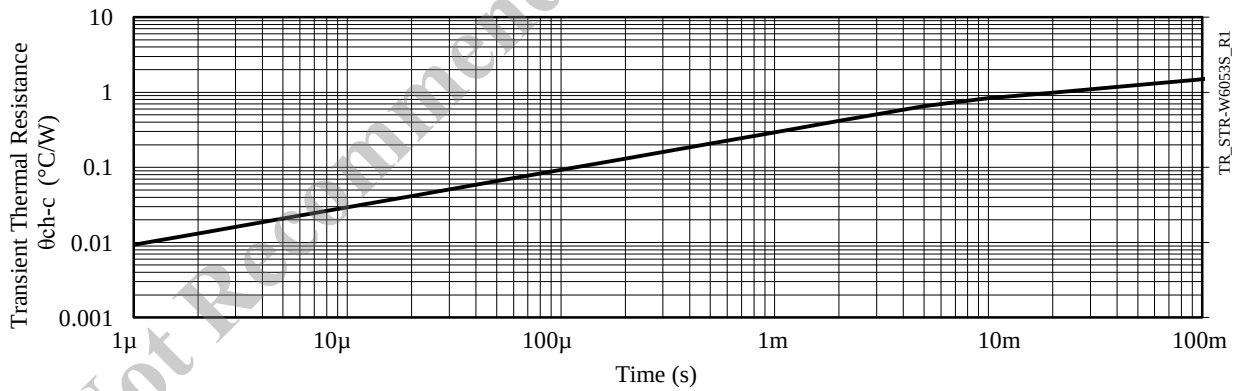
• **STR-W6051S**



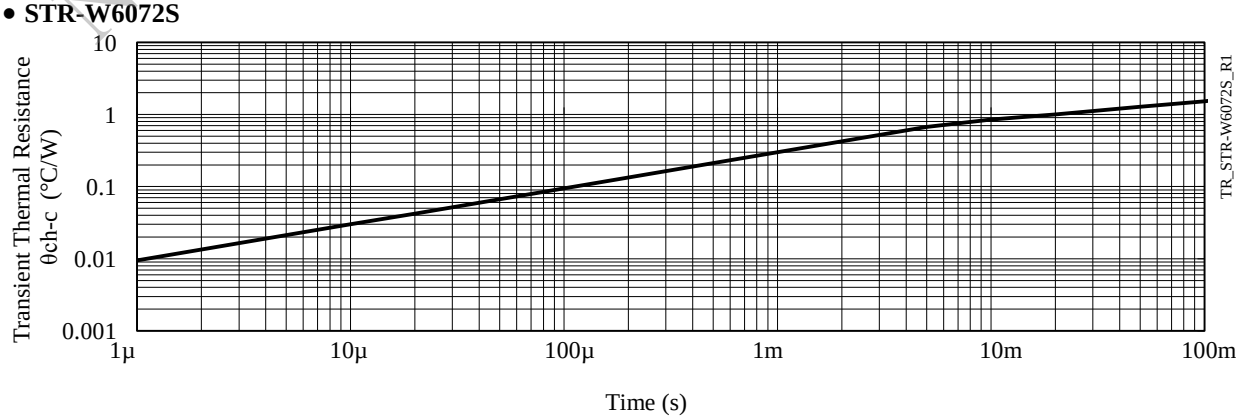
• **STR-W6052S**



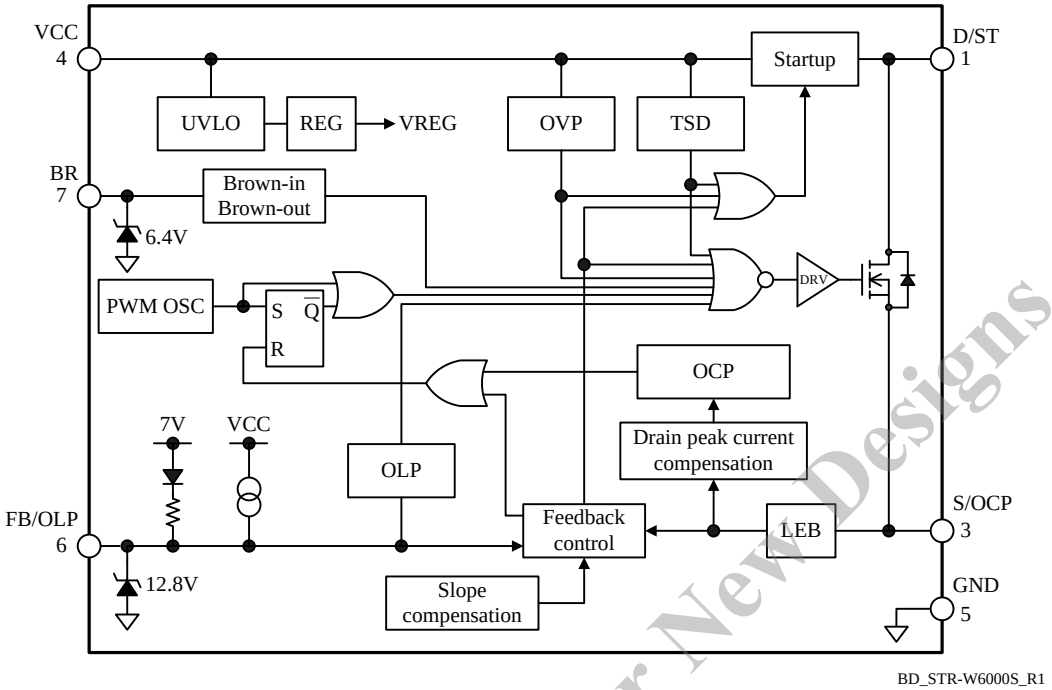
• **STR-W6053S**



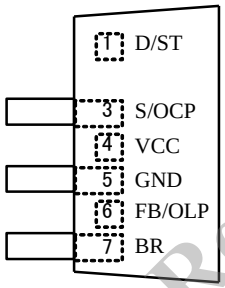
• **STR-W6072S**



4. Functional Block Diagram



5. Pin Configuration Definitions



(LF2003)

Pin	Name	Descriptions
1	D/ST	MOSFET drain and startup current input
2	–	(Pin removed)
3	S/OCP	MOSFET source and overcurrent protection (OCP) signal input
4	VCC	Power supply voltage input for control part and overvoltage protection (OVP) signal input
5	GND	Ground
6	FB /OLP	Constant voltage control signal input and over load protection (OLP) signal input
7	BR	Brown-In and Brown-Out detection voltage input

6. Typical Application Circuit

- The following drawings show circuits enabled and disabled the Brown-In/Brown-Out function.
- The PCB traces D/ST pins should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that D/ST pin has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

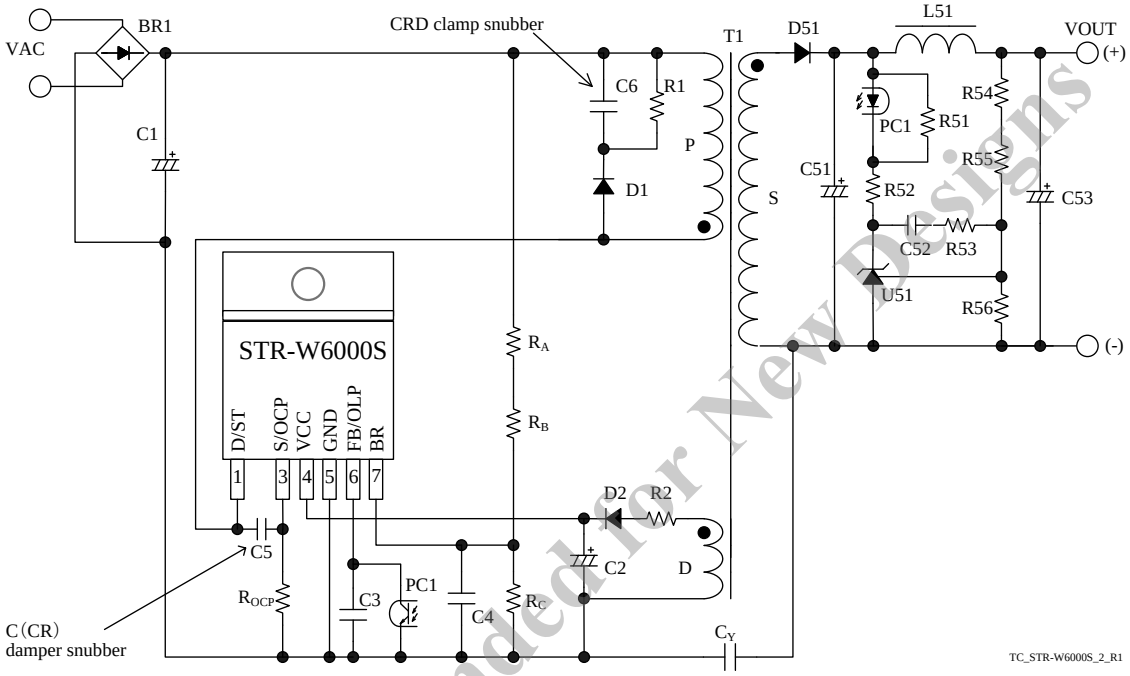


Figure 6-1 Typical application circuit (enabled Brown-In/Brown-Out function, DC line detection)

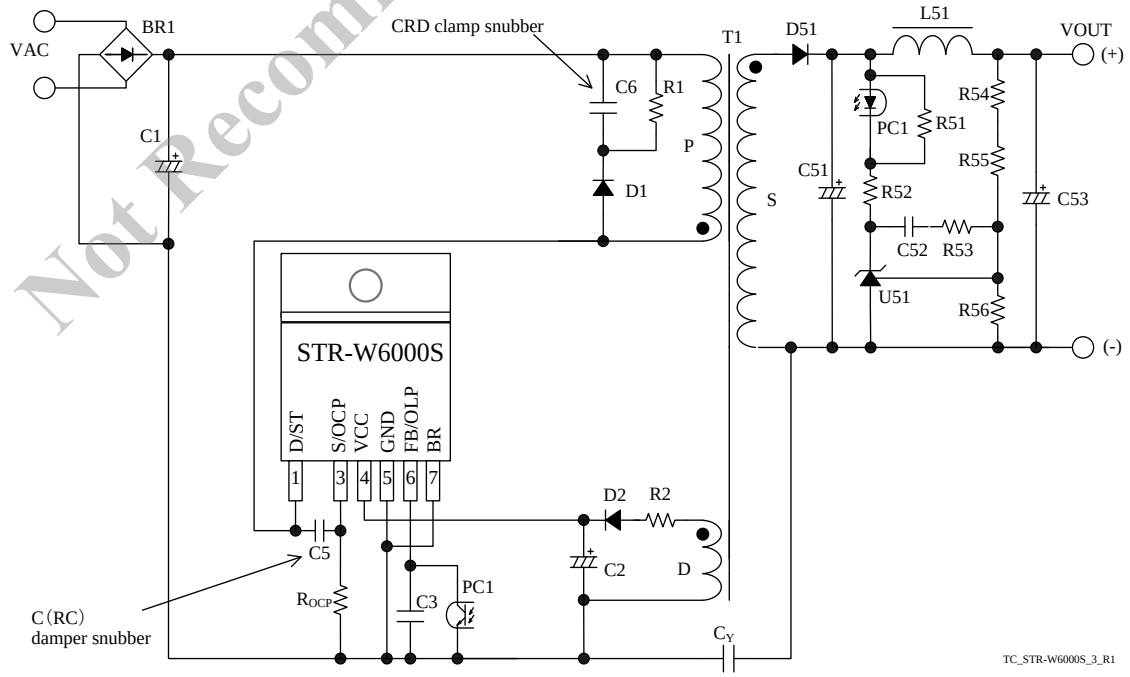
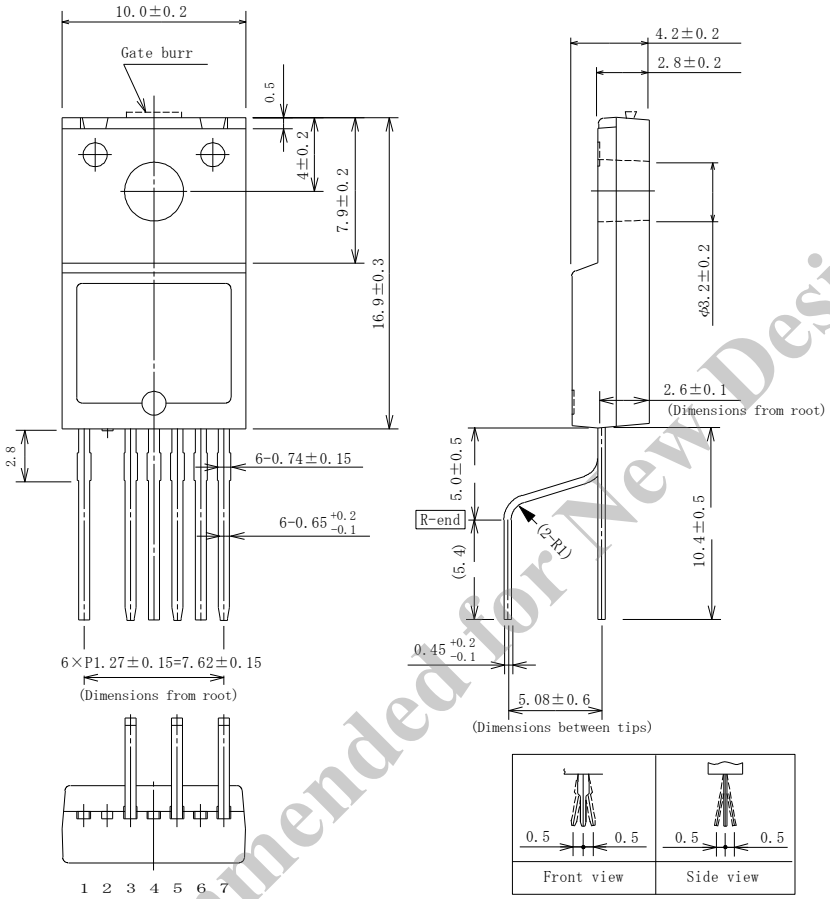


Figure 6-2 Typical application circuit (disabled Brown-In/Brown-Out function)

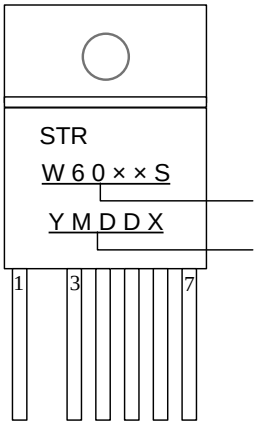
7. Package Outline

- TO220F-6L
- The pin 2 is removed to provide greater creepage and clearance isolation between the high voltage pin (pin 1: D/ST) and the low voltage pin (pin 3: S/OCP).



NOTES:
1) Dimension is in millimeters
2) Leadform: LF No.2003
3) Gate burr indicates protrusion of 0.3 mm (max).
4) Pb-free. Device composition compliant with the RoHS directive

8. Marking Diagram



Part Number

Lot Number
Y is the last digit of the year (0 to 9)
M is the month (1 to 9, O, N or D)
DD is a day (01 to 31)
X is the Sanken Control Symbol

9. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

9.1 Startup Operation

Figure 9-1 shows the circuit around IC. Figure 9-2 shows the start up operation.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)}$ = 40 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{STARTUP}$ = − 2.5 mA, charges C2 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the control circuit starts operation.

During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 9-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate value of auxiliary winding voltage is about 15 V to 20 V, taking account of the winding turns of D winding so that VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 10.5\ (V) < V_{CC} < 26\ (V) \quad (1)$$

The oscillation start timing of IC depends on Brown-In / Brown-Out function (refer to Section 9.8).

- Without Brown-In / Brown-Out function (BR pin voltage is $V_{BR(DIS)}$ = 0.48 V or less)
  When VCC pin voltage increases to $V_{CC(ON)}$, the IC starts switching operation, As shown in Figure 9-2.

  The startup time of IC is determined by C2 capacitor value. The approximate startup time t_{START} (shown in Figure 9-2) is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STRATUP}|} \quad (2)$$

  where,
  t_{START} : Startup time of IC (s)
  $V_{CC(INT)}$: Initial voltage on VCC pin (V)

- With Brown-In / Brown-Out function
  When BR pin voltage is more than $V_{BR(DIS)}$ = 0.48 V and less than $V_{BR(IN)}$ = 5.6 V, the Bias Assist Function (refer to Section 9.3) is disabled. Thus, VCC pin voltage repeats increasing to $V_{CC(ON)}$ and decreasing to $V_{CC(OFF)}$ (shown in Figure 9-3). When BR pin voltage becomes $V_{BR(IN)}$ or more, the IC starts switching operation.

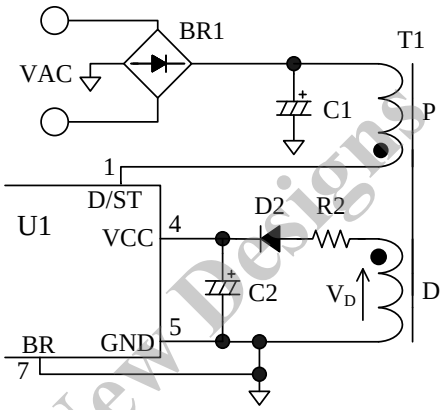


Figure 9-1 VCC pin peripheral circuit
(Without Brown-In / Brown-Out)

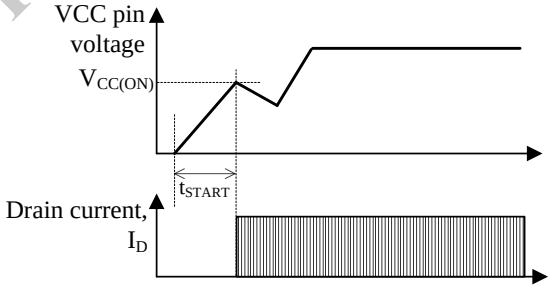


Figure 9-2 Startup operation
(Without Brown-In / Brown-Out)

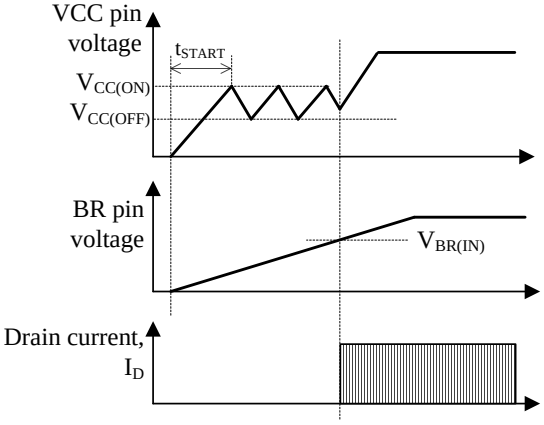


Figure 9-3 Startup operation
(With Brown-In / Brown-Out)

9.2 Undervoltage Lockout (UVLO)

Figure 9-4 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

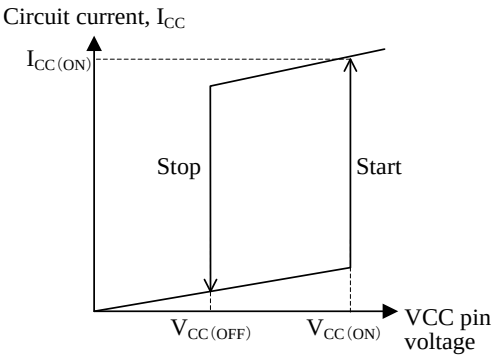


Figure 9-4 Relationship between VCC pin voltage and I_{CC}

9.3 Bias Assist Function

Figure 9-5 shows VCC pin voltage behavior during the startup period.

After VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. At the same time, the auxiliary winding voltage V_D increases in proportion to output voltage. These are all balanced to produce VCC pin voltage.

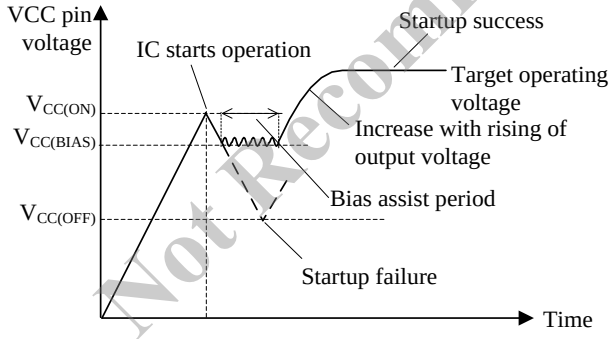


Figure 9-5 VCC pin voltage during startup period

The surge voltage is induced at output winding at turning off a power MOSFET. When the output load is light at startup, the surge voltage causes the unexpected feedback control. This results the lowering of the output power and VCC pin voltage. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the IC stops switching operation and a startup failure occurs. In order to prevent this, the Bias Assist function is activated when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$ = 9.5 V. While the Bias Assist function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, $I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept almost constant.

By the Bias Assist function, the value of C2 is allowed to be small and the startup time becomes shorter. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function becomes shorter.

It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

9.4 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Section 4 Functional Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 9-6 and Figure 9-7.

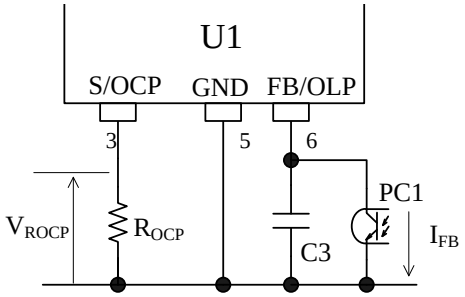


Figure 9-6 FB/OLP pin peripheral circuit

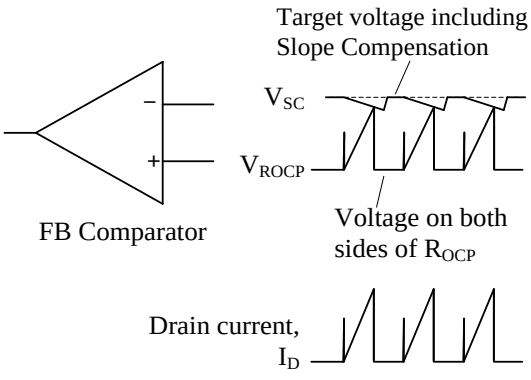


Figure 9-7 Drain current, I_D, and FB comparator operation in steady operation

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 9-8. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

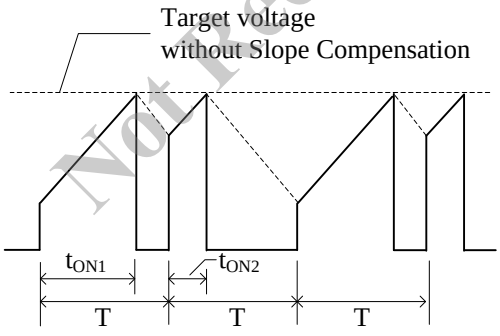


Figure 9-8 Drain current, I_D, waveform in subharmonic oscillation

9.5 Leading Edge Blanking Function

The IC uses the peak-current-mode control method for the constant voltage control of output.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or overcurrent protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, t_{BW} = 390 ns is built-in. During t_{BW}, the OCP threshold voltage becomes about 1.7 V which is higher than the normal OCP threshold voltage (refer to Section 9.9).

9.6 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

9.7 Automatic Standby Mode Function

Automatic standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 15 % to 20 % of the maximum drain current (it is in the OCP state). The operation mode becomes burst oscillation, as shown in Figure 9-9. Burst oscillation mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

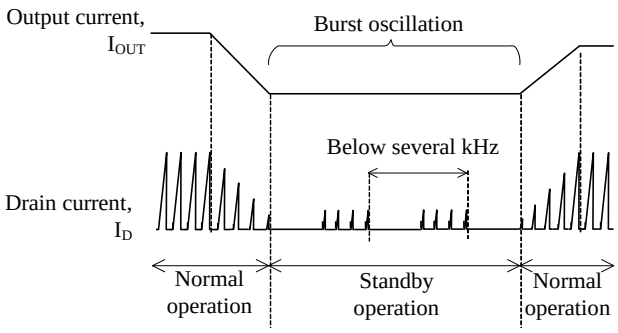


Figure 9-9 Auto Standby mode timing

Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst oscillation mode, audible noises can be reduced.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.5 V during the transition to the burst oscillation mode, the Bias Assist function is activated and stabilizes the Standby mode operation, because $I_{STARTUP}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary winding and/or reducing the value of R2 in Figure 10-2 (refer to Section 10.1 Peripheral Components for a detail of R2).

9.8 Brown-In and Brown-Out Function

This function stops switching operation when it detects low input line voltage, and thus prevents excessive input current and overheating.

This function turns on and off switching operation according to the BR pin voltage detecting the AC input voltage. When BR pin voltage becomes more than $V_{BR(DIS)}$ = 0.48 V, this function is activated.

Figure 9-10 shows waveforms of the BR pin voltage and the drain currnet.

Even if the IC is in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, when the AC input voltage decreases from steady-state and the BR pin voltage falls to $V_{BR(OUT)}$ = 4.8 V or less for the OLP Delay Time, t_{OLP} = 68 ms, the IC stops switching operation.

When the AC input voltage increases and the BR pin voltage reaches $V_{BR(IN)}$ = 5.6 V or more in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, the IC starts switching operation.

In case the Brown-In and Brown-Out function is unnecessary, connect the BR pin trace to the GND pin trace so that the BR pin voltage is $V_{BR(DIS)}$ or less.

This function is disabled during switching operation stop period in burst oscillation mode. When the BR pin voltage falls to $V_{BR(OUT)}$ or less in burst oscillation mode and the sum of switching operation period becomes t_{OLP} = 68 ms or more, the IC stops switching operation.

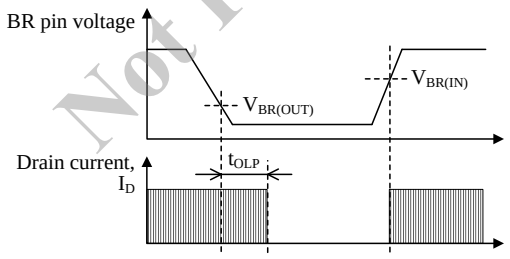


Figure 9-10 BR pin voltage and drain current waveforms

There are two types of detection method as follows:

9.8.1 DC Line Detection

Figure 9-11 shows BR pin peripheral circuit of DC line detection. There is a ripple voltage on C1 occurring at a half period of AC cycle. In order to detect each peak of the ripple voltage, the time constant of R_C and C4 should be shorter than a half period of AC cycle.

Since the cycle of the ripple voltage is shorter than t_{OLP}, the switching operation does not stop when only the bottom part of the ripple voltage becomes lower than $V_{BR(OUT)}$.

Thus it minimizes the influence of load conditions on the voltage detection.

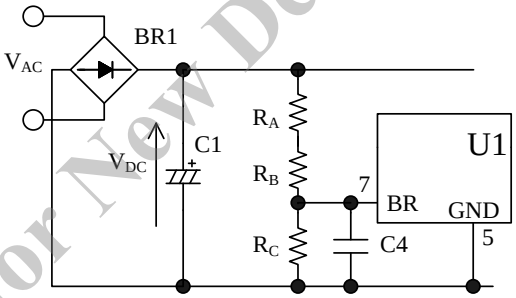


Figure 9-11 DC line detection

The components around BR pin:

- R_A and R_B are a few megohms. Because of high voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
- R_C is a few hundred kilohms
- C4 is 470 pF to 2200 pF for high frequency noise reduction

Neglecting the effect of both input resistance and forward voltage of rectifier diode, the reference value of C1 voltage when Brown-In and Brown-Out function is activated is calculated as follows:

$$V_{DC(OP)} = V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right) \quad (3)$$

where,

$V_{DC(OP)}$: C1 voltage when Brown-In and Brown-Out function is activated

$V_{BR(TH)}$: Any one of threshold voltage of BR pin (see Table 9-1)

Table 9-1 BR pin threshold voltage

Parameter	Symbol	Value (Typ.)
Brown-In Threshold Voltage	$V_{BR(IN)}$	5.6 V
Brown-Out Threshold Voltage	$V_{BR(OUT)}$	4.8 V

$V_{DC(OP)}$ can be expressed as the effective value of AC input voltage using Equation (4).

$$V_{AC(OP)RMS} = \frac{1}{\sqrt{2}} \times V_{DC(OP)} \quad (4)$$

R_A, R_B, R_C and C4 should be selected based on actual operation in the application.

9.8.2 AC Line Detection

Figure 9-12 shows BR pin peripheral circuit of AC line detection.

In order to detect the AC input voltage, the time constant of R_C and C4 should be longer than the period of AC cycle. Thus the response of BR pin detection becomes slow compared with the DC line detection.

This method detects the AC input voltage, and thus it minimizes the influence from load conditions.

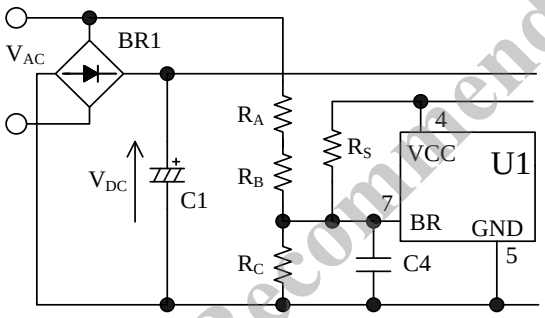


Figure 9-12 AC line detection

The components around BR pin:

- R_A and R_B are a few megohms. Because of high voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
- R_C is a few hundred kilohms
- R_S must be adjusted so that the BR pin voltage is more than $V_{BR(DIS)}$ = 0.48 V when the VCC pin voltage is $V_{CC(OFF)}$ = 8.1 V
- C4 is 0.22 µF to 1 µF for averaging AC input voltage and high frequency noise reduction.

Neglecting the effect of input resistance is zero, the reference effective value of AC input voltage when Brown-In and Brown-Out function is activated is calculated as follows:

$$V_{AC(OP)RMS} = \frac{\pi}{\sqrt{2}} \times V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right) \quad (5)$$

where,

$V_{AC(OP)RMS}$:The effective value of AC input voltage when Brown-In and Brown-Out function is activated

$V_{BR(TH)}$:Any one of threshold voltage of BR pin (see Table 9-1)

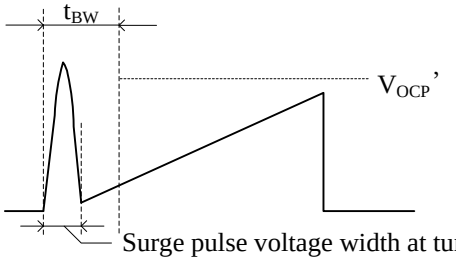
R_A, R_B, R_C and C4 should be selected based on actual operation in the application.

9.9 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

During Leading Edge Blanking Time (t_{BW}), OCP is disabled. When power MOSFET turns on, the surge voltage width of S/OCP pin should be less than t_{BW}, as shown in Figure 9-13. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (refer to Section □).

In addition, if a C (RC) damper snubber of Figure 9-14 is used, reduce the capacitor value of damper snubber.



Surge pulse voltage width at turning on

Figure 9-13 S/OCP pin voltage

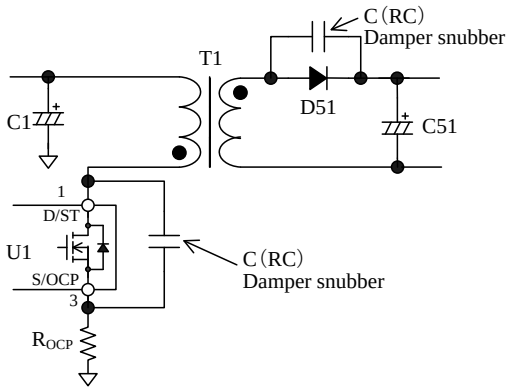


Figure 9-14 Damper snubber

< Input Compensation Function >

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to V_{OCP}. Thus, the peak current has some variation depending on the AC input voltage in OCP state.

In order to reduce the variation of peak current in OCP state, the IC incorporates a built-in Input Compensation function.

The Input Compensation Function is the function of correction of OCP threshold voltage depending with AC input voltage, as shown in Figure 9-15.

When AC input voltage is low (ON Duty is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (ON Duty is narrow).

The compensation signal depends on ON Duty. The relation between the ON Duty and the OCP threshold voltage after compensation V_{OCP}' is expressed as Equation (6). When ON Duty is broader than 36 %, the V_{OCP}' becomes a constant value $V_{OCP(H)}$ = 0.88 V

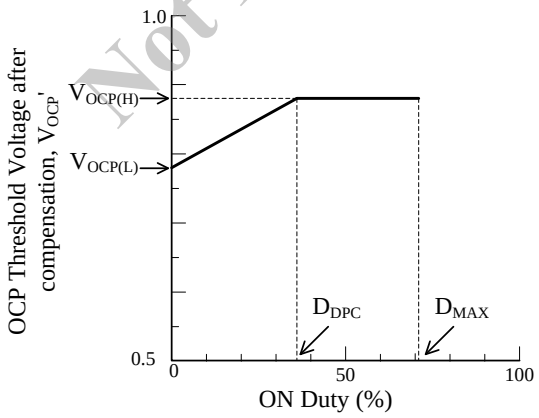


Figure 9-15 Relationship between ON Duty and Drain Current Limit after compensation

$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{ONDuty}{f_{OSC(AVG)}} \quad (6)$$

where,
$V_{OCP(L)}$: OCP Threshold Voltage at Zero ON Duty
DPC: OCP Compensation Coefficient
ONTime: On-time of power MOSFET
ONDuty: On duty of power MOSFET
$f_{OSC(AVG)}$: Average PWM Switching Frequency

9.10 Overload Protection Function (OLP)

Figure 9-16 shows the FB/OLP pin peripheral circuit, and Figure 9-17 shows each waveform for OLP operation.

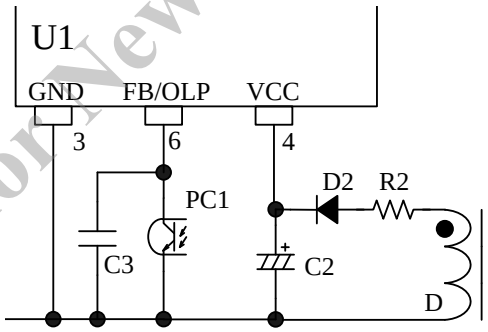


Figure 9-16 FB/OLP pin peripheral circuit

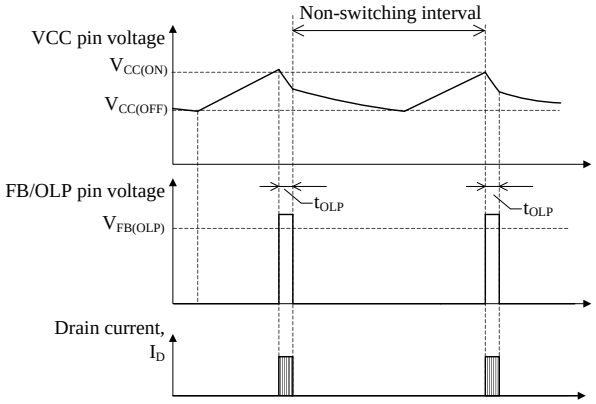


Figure 9-17 OLP operational waveforms

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and the FB/OLP pin voltage increases. When the FB/OLP pin voltage

increases to $V_{FB(OLP)}$ = 8.1 V or more for the OLP delay time, t_{OLP} = 68 ms or more, the OLP function is activated, the IC stops switching operation.

During OLP operation, Bias Assist Function is disabled. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops operation. After that, the IC reverts to the initial state by UVLO circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ by startup current. Thus the intermittent operation by UVLO is repeated in OLP state.

This intermittent operation reduces the stress of parts such as power MOSFET and secondary side rectifier diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

9.11 Overvoltage Protection (OVP)

When a voltage between VCC pin and GND pin increases to $V_{CC(OVP)}$ = 29 V or more, OVP function is activated, the IC stops switching operation. During OVP operation, the Bias Assist function is disabled, the intermittent operation by UVLO is repeated (refer to Section 9.10). When the fault condition is removed, the IC returns to normal operation automatically (refer to Figure 9-18).

In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as output voltage detection circuit open can be detected because the VCC pin voltage is proportional to output voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (7).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29\ (V) \quad (7)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

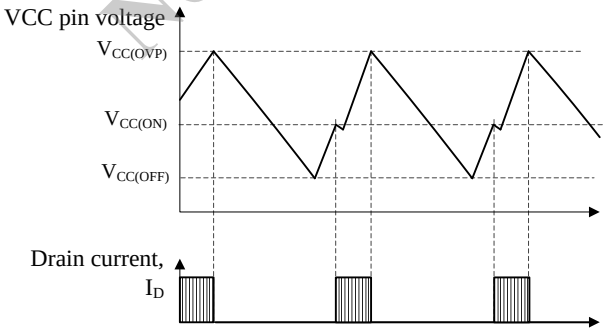


Figure 9-18 OVP operational waveforms

9.12 Thermal Shutdown Function (TSD)

When the temperature of control circuit increases to $T_{j(TSD)}$ = 130 °C or more, Thermal Shutdown function (TSD) is activated, the IC stops switching operation. During TSD operation, the Bias Assist function is disabled, the intermittent operation by UVLO is repeated (refer to Section 9.10). When the fault condition is removed and the temperature decreases to less than $T_{j(TSD)}$, the IC returns to normal operation automatically.

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

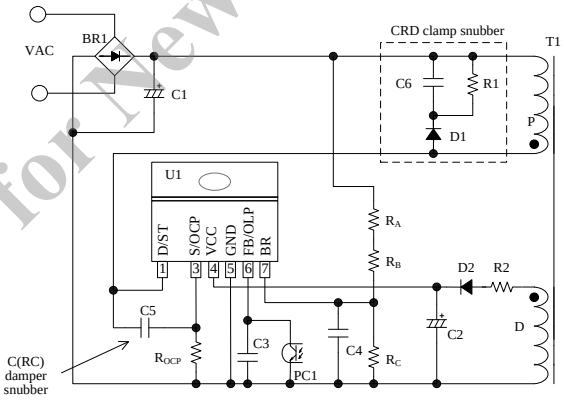


Figure 10-1 The IC peripheral circuit

- **Input and Output Electrolytic Capacitor**
  Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

- **S/OCP Pin Peripheral Circuit**
  In Figure 10-1, R_{OCP} is the resistor for the current detection. A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

- **VCC Pin Peripheral Circuit**
  The value of C2 in Figure 10-1 is generally recommended to be 10µ to 47µF (refer to Section 9.1 Startup Operation, because the startup time is determined by the value of C2).
  In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 10-2), and the Overvoltage Protection function (OVP) on the VCC

pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.
For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 10-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

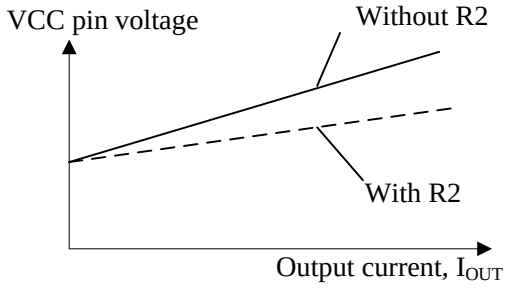


Figure 10-2 Variation of VCC pin voltage and power

- **FB/OLP Pin Peripheral Circuit**

C3 is for high frequency noise reduction and phase compensation, and should be connected close to these pins. The value of C3 is recommended to be about 2200 pF to 0.01µF, and should be selected based on actual operation in the application.

- **BR pin peripheral circuit**

Because R_A and R_B (see Figure 10-1) are applied high voltage and are high resistance, the following should be considered according to the requirement of the application:

- ▫ Select a resistor designed against electromigration, or
- ▫ Use a combination of resistors in series for that to reduce each applied voltage

See the section 9.8 about the AC input voltage detection function and the components around BR pin.
When the detection resistor (R_A, R_B, R_C) value is decreased and the C4 value is increased to prevent unstable operation resulting from noise at the BR pin, pay attention to the low efficiency and the slow response of BR pin.

- **Snubber Circuit**

In case the surge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 10-1);

- ・ A clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P.
- ・ A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.
  In case the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

- **Peripheral circuit of secondary side shunt regulator**

Figure 10-3 shows the secondary side detection circuit with the standard shunt regulator IC (U51).
C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047µF to 0.47µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

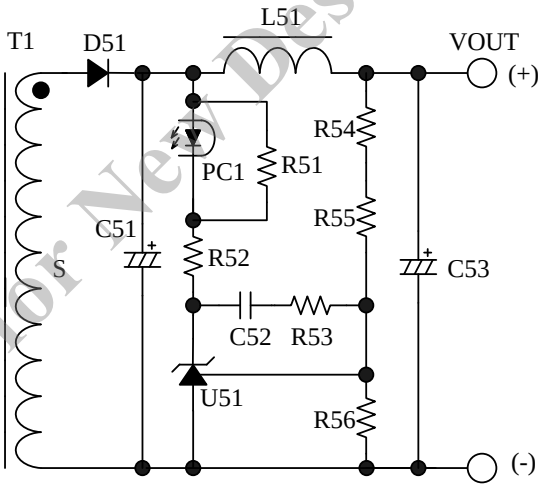


Figure 10-3 Peripheral circuit of secondary side shunt regulator (U51)

- **Transformer**

Apply proper design margin to core temperature rise by core loss and copper loss.
Because the switching currents contain high frequency currents, the skin effect may become a consideration.
Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.
If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- ▫ Increase the number of wires in parallel.
- ▫ Use litz wires.
- ▫ Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- ▫ The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- ▫ The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection function (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs.

Figure 10-4 shows the winding structural examples of two outputs.

Winding structural example (a):

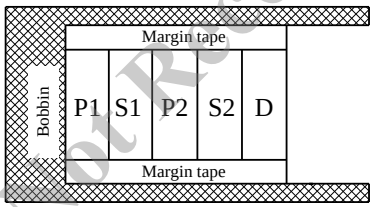
S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.

D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

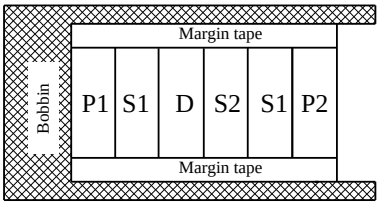
Winding structural example (b)

P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.

D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.



Winding structural example (a)



Winding structural example (b)

Figure 10-4 Winding structural examples

10.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-5 shows the circuit design example.

(1) Main Circuit Trace Layout

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout

Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 10-5 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout

This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) R_{OCP} Trace Layout

R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 10-5) which is close to the base of R_{OCP}.

(5) Peripheral components of the IC

The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:

This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET

breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations

Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design. Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

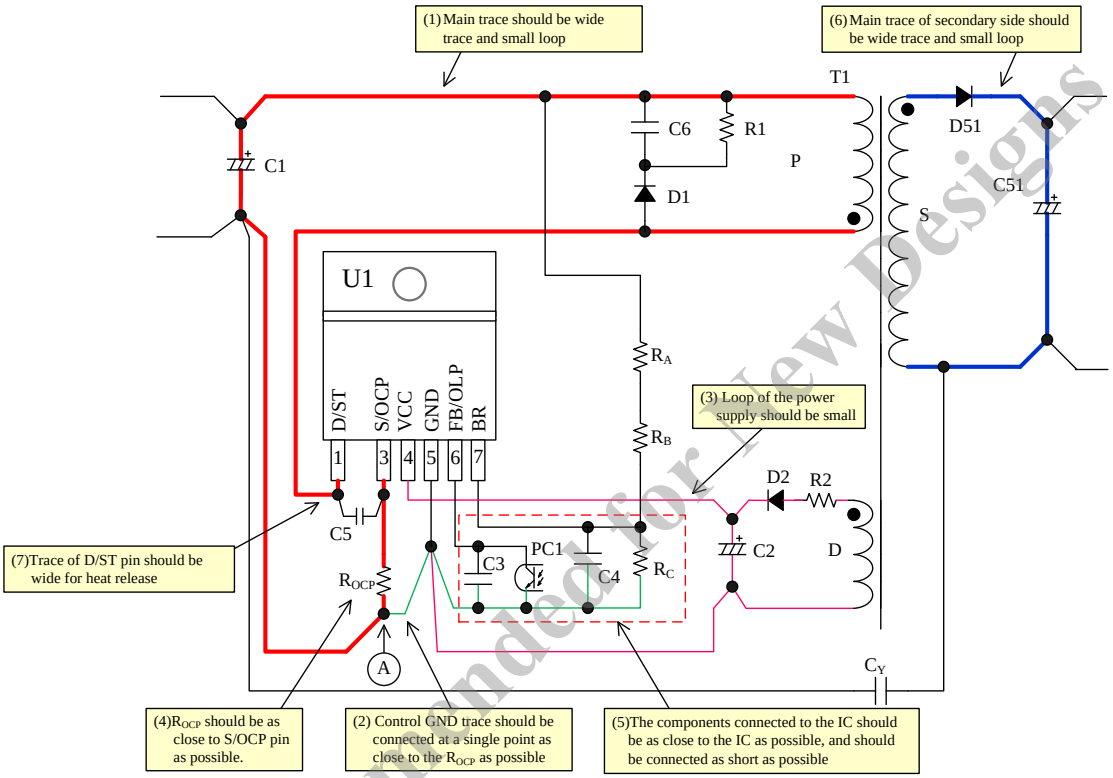


Figure 10-5 Peripheral circuit example around the IC

11. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of the four outputs circuit using STR-W6000S series without Brown-In and Brown-Out function.

The above circuit symbols correspond to these of Figure 11-1. Only the parts in the schematic are used. Other parts in PCB are leaved open. C11 and D4 are shorted.

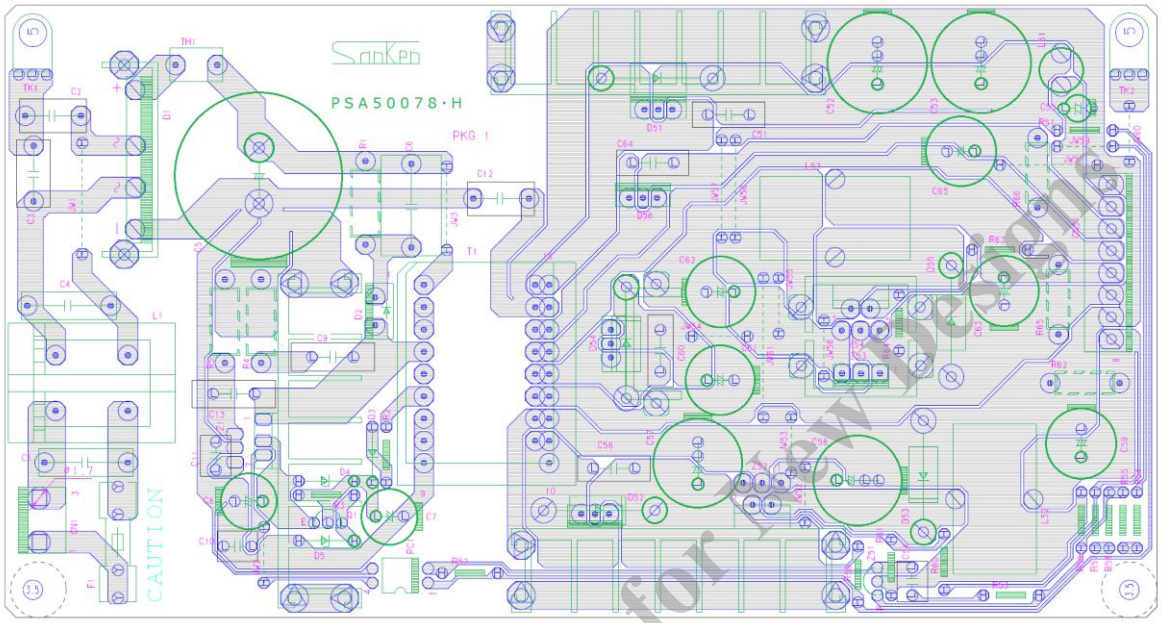


Figure 11-1 PCB circuit trace layout example

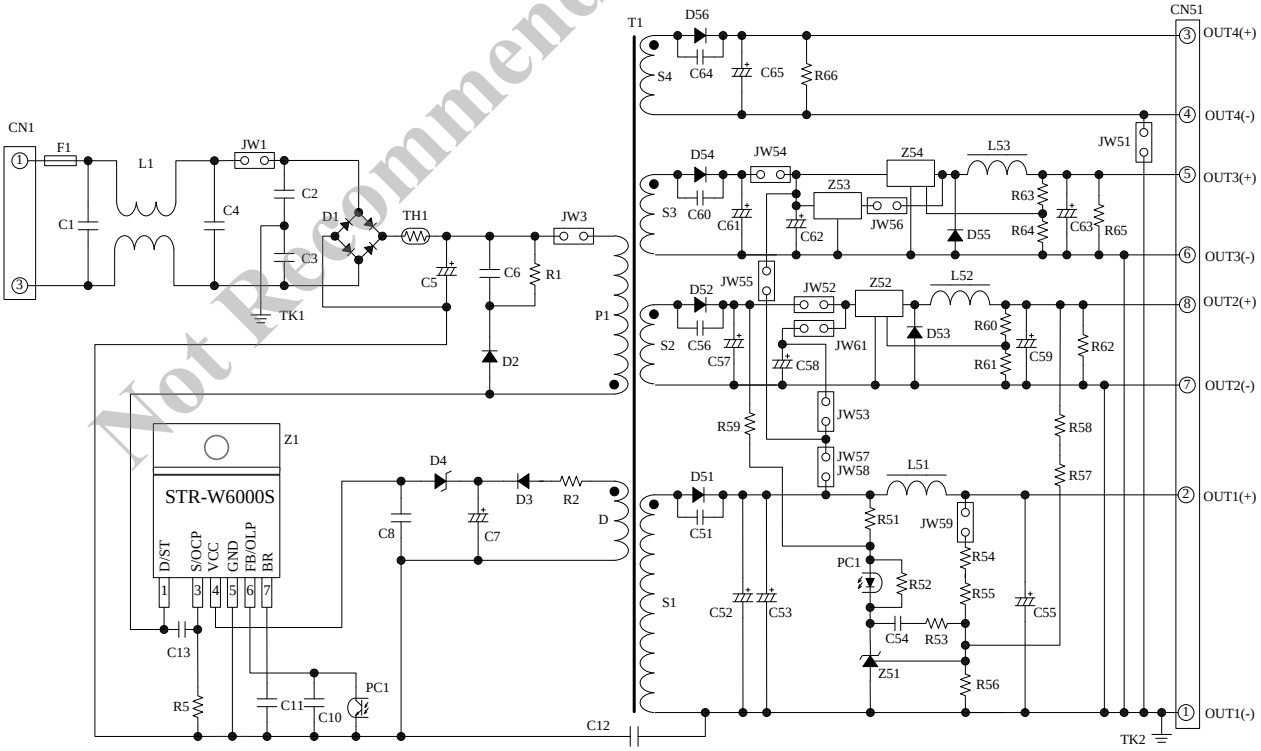


Figure 11-2 Circuit schematic for PCB circuit trace layout

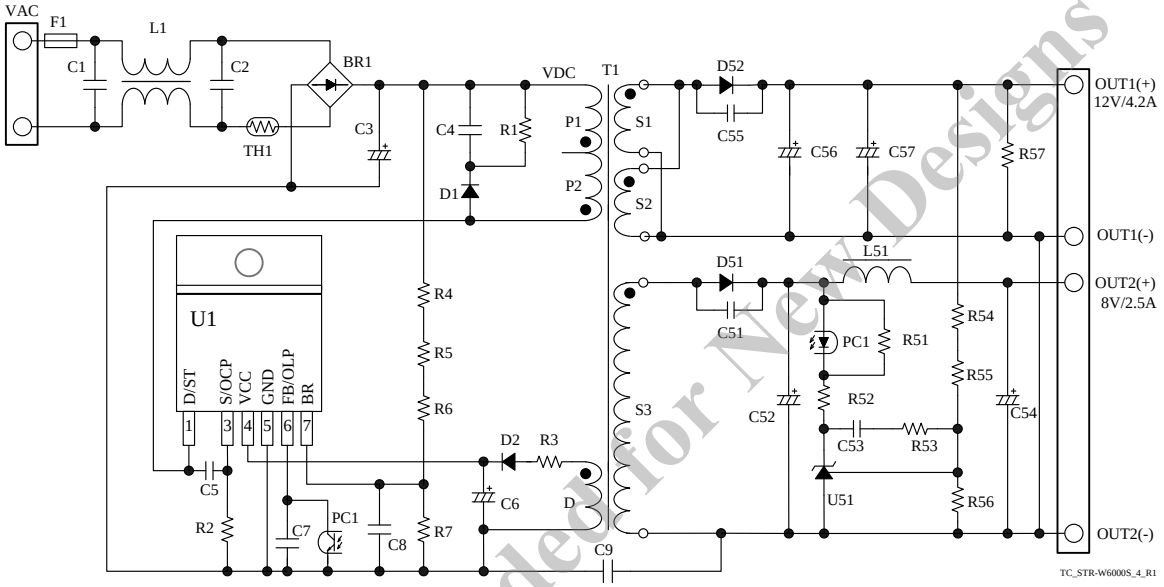
12. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

● Power supply specification

IC	STR-W6053S
Input voltage	AC85 V to AC265 V
Maximum output power	56 W (70.4 W_{PEAK})
Output 1	8 V / 2.5 A
Output 2	12 V / 3 A (4.2 A_{PEAK})

● Circuit schematic



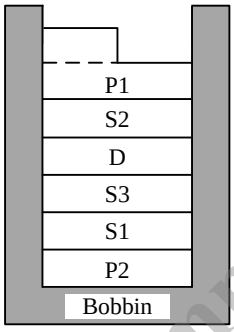
● Bill of materials

Symbol	Part type	Ratings(1)	Recommended Sanken Parts	Symbol	Part type	Ratings(1)	Recommended Sanken Parts
F1	Fuse	AC 250 V, 6 A		PC1	Photo-coupler	PC123 or equiv	
L1 (2)	CM inductor	2.2 mH		U1	IC	—	STR-W6053S
TH1 (2)	NTC thermistor	Short		T1	Transformer	See the specification	
BR1	General	600 V, 6 A		L51	Inductor	5 µH	
D1	Fast recovery	1000 V, 0.5 A	EG01C	D51	Schottky	100 V, 10 A	FMEN-210A
D2	Fast recovery	200 V, 1 A	AL01Z	D52	Fast recovery	150 V, 10 A	FMEN-210B
C1 (2)	Film, X2	0.1 µF, 275 V		C51 (2)	Ceramic	470 pF, 1 kV	
C2 (2)	Film, X2	0.1 µF, 275 V		C52	Electrolytic	1000 µF, 16 V	
C3	Electrolytic	220 µF, 400 V		C53 (2)	Ceramic	0.15 µF, 50 V	
C4	Ceramic	3300 pF, 2 kV		C54	Electrolytic	1000 µF, 16 V	
C5 (2)	Ceramic	Open		C55 (2)	Ceramic	470 pF, 1 kV	
C6	Electrolytic	22 µF, 50V		C56	Electrolytic	1500 µF, 25 V	
C7 (2)	Ceramic	0.01 µF		C57	Electrolytic	1500 µF, 25 V	
C8 (2)	Ceramic	1000 pF		R51	General	1.5 kΩ	
C9	Ceramic, Y1	2200 pF, 250 V		R52	General	1 kΩ	
R1 (3)	Metal oxide	56 kΩ, 2 W		R53 (2)	General	33 kΩ	
R2	General	0.27 Ω, 1 W		R54 (2)	General, 1%	3.9 kΩ	
R3	General	5.6 Ω		R55	General, 1%	22 kΩ	
R4 (3)	General	2.2MΩ		R56	General, 1%	6.8 kΩ	
R5 (3)	General	2.2MΩ		R57	General	Open	
R6 (3)	General	2.2MΩ		U51	Shunt regulator	V_{REF} = 2.5 V TL431or equiv	
R7 (2)	General	470kΩ					

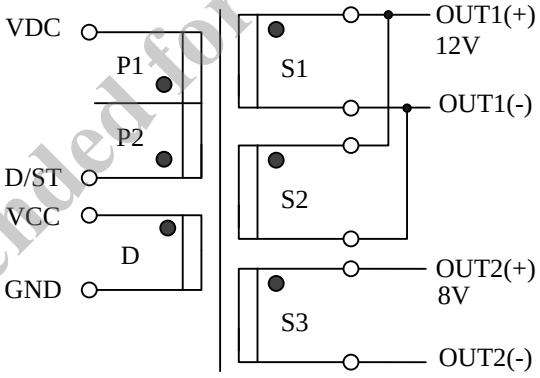
(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

● Transformer specification
- ▫ Primary inductance, L_P : L_P : 315 µH
- ▫ Core size : EER28L
- ▫ Al-value : 163 nH/N^2 (Center gap of about 0.8 mm)
- ▫ Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction
Primary winding 1	P1	26	TEX – φ 0.35 × 2	Two-layers, solenoid winding
Primary winding 2	P2	18	TEX – φ 0.35 × 2	Single-layer, solenoid winding
Auxiliary winding	D	10	TEX – φ 0.23 × 2	Single-layer, space winding
Output winding 1	S1	7	φ 0.4 × 4	Single-layer, space winding
Output winding 2	S2	7	φ 0.4 × 4	Single-layer, space winding
Output winding 3	S3	5	φ 0.4 × 4	Single-layer, space winding



Cross-section view



●: Start at this pin

OPERATING PRECAUTIONS

In the case that you use Sanken products or design your products by using Sanken products, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor products. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration. In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Remarks About Using Thermal Silicone Grease

- When thermal silicone grease is used, it shall be applied evenly and thinly. If more silicone grease than required is applied, it may produce excess stress.
- The thermal silicone grease that has been stored for a long period of time may cause cracks of the greases, and it cause low radiation performance. In addition, the old grease may cause cracks in the resin mold when screwing the products to a heatsink.
- Fully consider preventing foreign materials from entering into the thermal silicone grease. When foreign material is immixed, radiation performance may be degraded or an insulation failure may occur due to a damaged insulating plate.
- The thermal silicone greases that are recommended for the resin molded semiconductor should be used.
  Our recommended thermal silicone grease is the following, and equivalent of these.

Type	Suppliers
G746	Shin-Etsu Chemical Co., Ltd.
YG6260	Momentive Performance Materials Japan LLC
SC102	Dow Corning Toray Co., Ltd.

Cautions for Mounting to a Heatsink

- When the flatness around the screw hole is insufficient, such as when mounting the products to a heatsink that has an extruded (burred) screw hole, the products can be damaged, even with a lower than recommended screw torque. For mounting the products, the mounting surface flatness should be 0.05mm or less.
- Please select suitable screws for the product shape. Do not use a flat-head machine screw because of the stress to the products. Self-tapping screws are not recommended. When using self-tapping screws, the screw may enter the hole diagonally, not vertically, depending on the conditions of hole before threading or the work situation. That may stress the products and may cause failures.
- Recommended screw torque: 0.588 to 0.785 N･m (6 to 8 kgf･cm).
- For tightening screws, if a tightening tool (such as a driver) hits the products, the package may crack, and internal stress fractures may occur, which shorten the lifetime of the electrical elements and can cause catastrophic failure. Tightening with an air driver makes a substantial impact. In addition, a screw torque higher than the set torque can be applied and the package may be damaged. Therefore, an electric driver is recommended.
  When the package is tightened at two or more places, first pre-tighten with a lower torque at all places, then tighten with the specified torque. When using a power driver, torque control is mandatory.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
  - 260 ± 5 °C 10 ± 1 s (Flow, 2 times)
  - 380 ± 10 °C 3.5 ± 0.5 s (Soldering iron, 1 time)
- Soldering should be at a distance of at least 1.5 mm from the body of the products.

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least 1MΩ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.

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