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1 Introduction

This datasheet provides the STR71x pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STR71x microcontroller memory, registers and peripherals. please refer to the STR71x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

Table 2. Device overview

Features	STR710 FZ1	STR710 FZ2	STR710 RZ	STR711 FR0	STR711 FR1	STR711 FR2	STR712 FR0	STR712 FR1	STR712 FR2	STR715 FRx
Flash - Kbytes	128+16	256+16	0	64+16	128+16	256+16	64+16	128+16	256+16	64+16
RAM - Kbytes	32	64	64	16	32	64	16	32	64	16
Peripheral Functions	CAN, EMI, USB, 48 I/Os			USB, 30 I/Os			CAN, 32 I/Os			32 I/Os
Operating Voltage	3.0 to 3.6 V									
Operating Temperature	-40 to +85°C or 0 to 70° C									
Packages	**T**=LQFP144 20 x 20 **H**=LFBGA144 10 x10			**T**=LQFP64 10 x10						

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2 Description

ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

3 System architecture

Package choice: low pin-count 64-pin or feature-rich 144-pin LQFP or BGA

The STR71x family is available in 5 main versions.

The 144-pin versions have the full set of all features including CAN, USB and External Memory Interface (EMI).

- **STR710F:** 144-pin BGA or LQFP with CAN, USB and EMI
- **STR710R:** Flashless 144-pin BGA or LQFP with CAN, USB and EMI (no internal Flash memory)

The three 64-pin versions (LQFP) do not include External Memory Interface.

- **STR715F:** 64-pin LQFP without CAN or USB
- **STR711F:** 64-pin LQFP with USB
- **STR712F:** 64-pin LQFP with CAN

High speed Flash memory (STR71xF)

The Flash program memory is organized in two banks of 32-bit wide Burst Flash memories enabling true read-while-write (RWW) operation. Device Bank 0 is up to 256 Kbytes in size, typically for the application program code. Bank 1 is 16 Kbytes, typically used for storing data constants. Both banks are accessed by the CPU with zero wait states @ 33 MHz

Bank 0 memory endurance is 10K write/erase cycles and Bank 1 endurance is 100K write/erase cycles. Data retention is 20 years at 85°C on both banks. The two banks can be accessed independently in read or write. Flash memory can be accessed in two modes:

- Burst mode: 64-bit wide memory access at up to 50 MHz.
- Direct 32-bit wide memory access for deterministic operation at up to 33 MHz.

The STR7 embedded Flash memory can be programmed using In-Circuit Programming or In-Application programming.

IAP (in-application programming): The IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): The ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector Write Protection
- Flash Debug Protection (locks JTAG access)

Refer to the STR7 Flash Programming Reference manual for details.

Optional external memory (STR710)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710 (144-pin) supports four 16-Mbyte banks of external memory. Wait states are programmable individually for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Flexible power management

To minimize power consumption, you can program the STR71x to switch to SLOW, WAIT, LPWAIT (low power wait), STOP or STANDBY mode depending on the current system activity in the application.

Flexible clock control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 66 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers. The microcontroller core, APB1 and APB2 peripherals are in separate clock domains and can be programmed to run at different frequencies during application runtime. The clock to each peripheral is gated with an individual control bit to optimize power usage by turning off peripherals any time they are not required.

Voltage regulators

The STR71x requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off during low power operation.

Low voltage detectors

Both the Main Voltage Regulator and the Low Power Voltage Regulator contain each a low voltage detection circuitry which keep the device under reset when the corresponding controlled voltage value (V_{18} or V_{18BKP}) falls below 1.35V (+/- 10%). This enhances the security of the system by preventing the MCU from going into an unpredictable state.

An external reset circuit must be used to provide the RESET at V_{33} power-up. It is not sufficient to rely on the RESET generated by the LVD in this case. This is because LVD operation is guaranteed only when V_{33} is within the specification.

3.1 On-chip peripherals

CAN interface (STR710 and STR712)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB interface (STR710 and STR711)

The full-speed USB interface is USB V2.0 compliant and provides up to 16 bidirectional/32 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer, isochronous transfers and USB Suspend/Resume functions.

Standard timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler

Three timers each provide up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

The fourth timer is not connected to the I/O ports. It can be used by the application software for general timing functions.

Realtime clock (RTC)

The RTC provides a set of continuously running counters driven by the 32 kHz external crystal. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71x is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32 kHz external crystal.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 1.25 Mb/s.

Smartcard interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smartcard interface as defined by ISO 7816-3. It includes Smartcard clock generation and provides support features for synchronous cards.

Buffered serial peripheral interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5 Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or round robin mode. Resolution is 12-bit with a sampling frequency of up to 1 kHz. The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

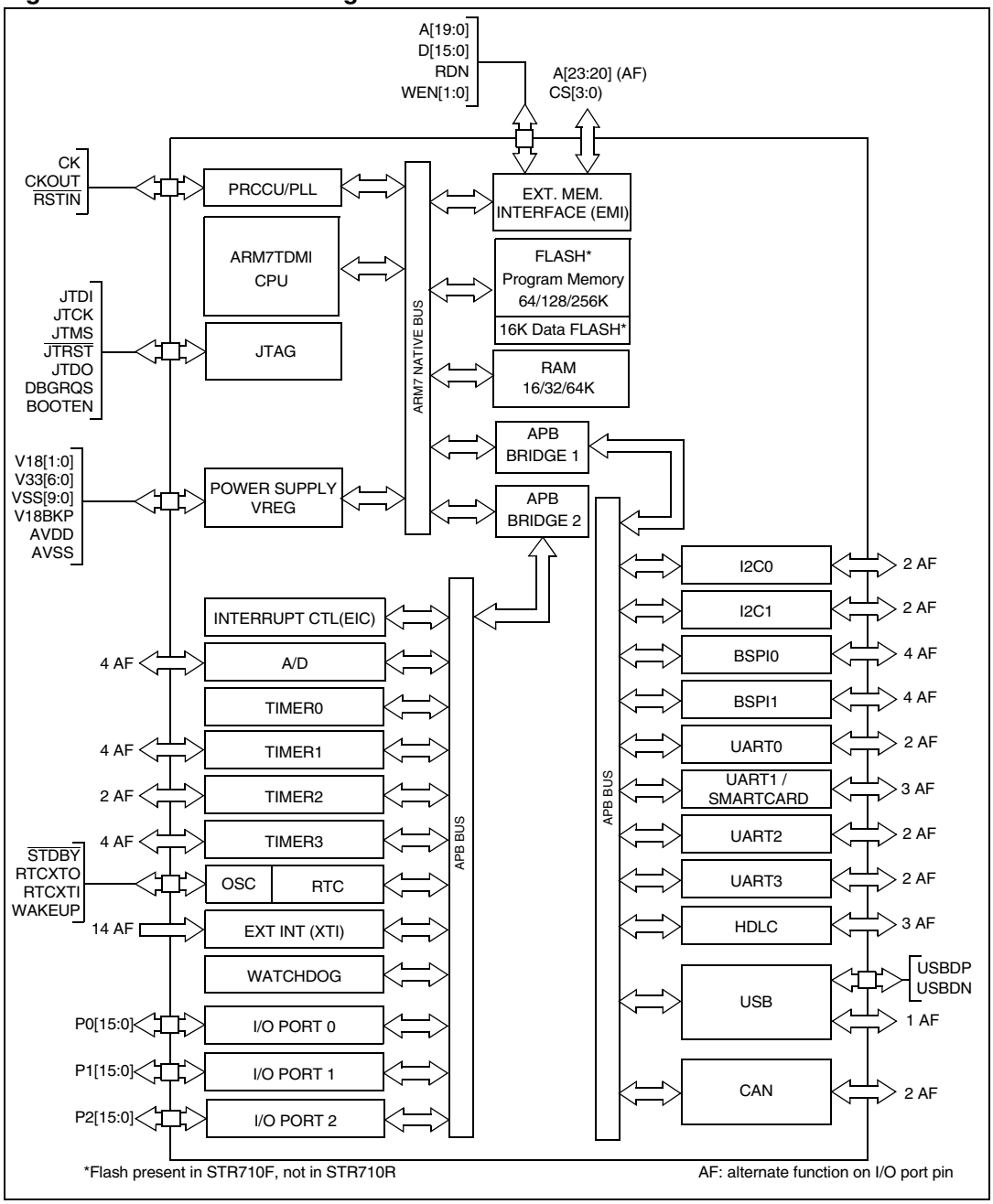
I/O ports

The 48 I/O ports are programmable as Inputs or Outputs.

External interrupts

Up to 14 external interrupts are available for application use or to wake up the application from STOP mode.

Figure 1. STR71x block diagram



3.2 Related documentation

Available from www.arm.com:

ARM7TDMI Technical reference manual

Available from http://www.st.com:

STR71x Reference manual

STR7 Flash programming manual

AN1774 - STR71x Software development getting started

AN1775 - STR71x Hardware development getting started

AN1776 - STR71x Enhanced interrupt controller

AN1777 - STR71x memory mapping

AN1780 - Real time clock with STR71x

AN1781 - Four 7 segment display drive using the STR71x

The above is a selected list only, a full list STR71x application notes can be viewed at http://www.st.com.

3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

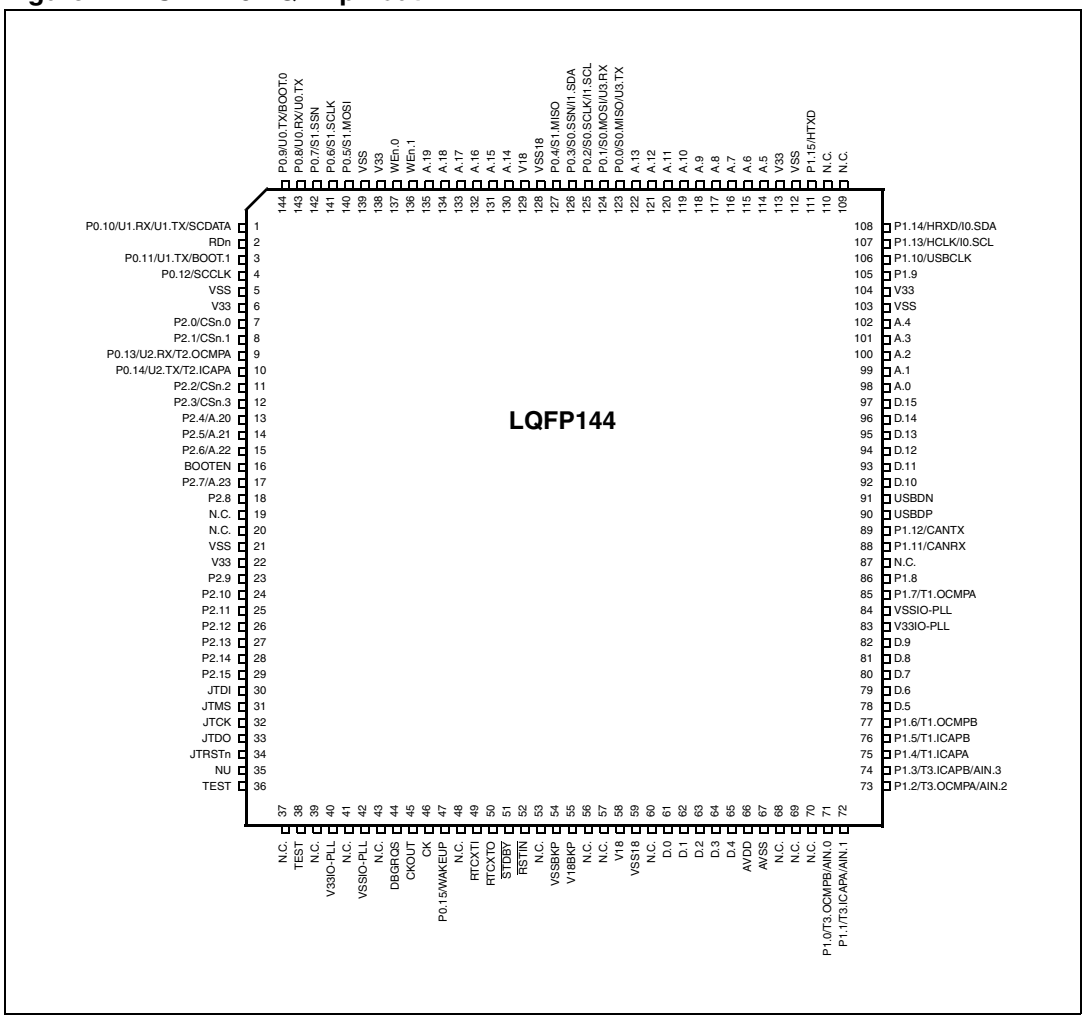


Table 3. STR710 BGA ball connections

	A	B	C	D	E	F	G	H	J	K	L	M
1	P0.10	P2.0	P2.1	VSS	P2.2	P2.6	BOOT EN	P2.12	P2.13	P2.15	JTDI	N.C.
2	VSS	RDn	P0.11	V33	P2.3	P2.8	P2.9	JTMS	JTRSTn	TEST	TEST	N.C.
3	V33	P0.9	P0.12	P0.13	P2.4	N.C.	P2.10	JTCK	NU	V33	N.C.	DBG RQS
4	P0.6	P0.7	P0.8	P0.14	P2.5	N.C.	P2.11	JTDO	CK	CKOUT	VSSIO-PLL	N.C.
5	A.19	WEn.1	WEn.0	P0.5	P2.7	VSS	P2.14	N.C.	RTCX-TO	RTCXTI	N.C.	P0.15
6	P0.3	A.15	A.16	A.17	A.18	V33	V18	N.C.	N.C.	V18BKP	VSS BKP	$\overline{\text{STDBY}}$
7	P0.2	P0.1	P0.4	VSS18	V18	A.14	D.12	D.1	D.0	nc	VSS18	$\overline{\text{RSTIN}}$
8	A.9	A.10	A.11	A.13	P0.0	A.0	D.11	P1.12/ CANTX	N.C.	AVSS	D.3	D.2
9	VSS	V33	A.5	A.6	V33	D.15	D.10	P1.8	D.9	P1.0	N.C.	N.C.
10	A.8	N.C.	P1.15	P1.13	VSS	D.14	USBDN	P1.7	D.8	P1.5	P1.1	D.4
11	A.7	N.C.	P1.14	P1.10	A.2	D.13	USBDP	VSS	D.5	P1.4	P1.3	AVDD
12	A.12	A.4	A.3	P1.9	A.1	P1.11/ CANRX	N.C.	V33IO-PLL	P1.6	D.7	D.6	P1.2

Legend / abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8 V/2 V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8 V / 2 V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5 V tolerant.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
1	A1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B2	$\overline{RD}$	O	5)					X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	C2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	C3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
5	D1	V_{SS}	S								Ground voltage for digital I/Os[4]		
6	D2	V_{33}	S								Supply voltage for digital I/Os[4]		
7	B1	P2.0/$\overline{CS}$.0	I/O	8)	C_T		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output **Note:** This pin is forced to output push-pull 1 mode at reset to allow boot from external memory	
8	C1	P2.1/$\overline{CS}$.1	I/O	pu 2)	C_T		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	D3	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
10	D4	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	E1	P2.2/$\overline{CS}$.2	I/O	pu 2)	C_T		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 2 output	
12	E2	P2.3/$\overline{CS}$.3	I/O	pu 2)	C_T		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 3 output	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
13	E3	P2.4/A.20	I/O	pd[3]	C_T		8mA	X	X		Port 2.4	External Memory Interface: address bus
14	E4	P2.5/A.21	I/O	pd[3]	C_T		8mA	X	X		Port 2.5	
15	F1	P2.6/A.22	I/O	pd[3]	C_T		8mA	X	X		Port 2.6	
16	G1	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins	
17	E5	P2.7/A.23	I/O	pd[3]	C_T		8mA	X	X		Port 2.7	External Memory Interface: address bus
18	F2	P2.8	I/O	pu	C_T	X	4mA	X	X		Port 2.8	External interrupt INT2
19	F3	N.C.									Not connected (not bonded)	
20	F4	N.C.									Not connected (not bonded)	
21	F5	V_{SS}	S								Ground voltage for digital I/Os[4]	
22	F6	V_{33}	S								Supply voltage for digital I/Os[4]	
23	G2	P2.9	I/O	pu	C_T	X	4mA	X	X		Port 2.9	External interrupt INT3
24	G3	P2.10	I/O	pu	C_T	X	4mA	X	X		Port 2.10	External interrupt INT4
25	G4	P2.11	I/O	pu	C_T	X	4mA	X	X		Port 2.11	External interrupt INT5
26	H1	P2.12	I/O	pu	C_T		4mA	X	X		Port 2.12	
27	J1	P2.13	I/O	pu	C_T		4mA	X	X		Port 2.13	
28	G5	P2.14	I/O	pu	C_T		4mA	X	X		Port 2.14	
29	K1	P2.15	I/O	pu	C_T		4mA	X	X		Port 2.15	
30	L1	JTDI	I		T_T						JTAG Data input. External pull-up required.	
31	H2	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.	
32	H3	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.	
33	H4	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.	
34	J2	JTRST	I		T_T						JTAG Reset Input. External pull-up required.	
35	J3	NU									Reserved, must be forced to ground.	
36	K2	TEST									Reserved, must be forced to ground.	
37	M1	N.C.									Not connected (not bonded)	
38	L2	TEST									Reserved, must be forced to ground.	
39	L3	N.C.									Not connected (not bonded)	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
40	K3	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference	
41	M4	N.C.									Not connected (not bonded)	
42	L4	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]	
43	M2	N.C.									Not connected (not bonded)	
44	M3	DBGRQS	I		C_T						Debug Mode request input (active high)	
45	K4	CKOUT	O				8mA		X		Clock output (f_{PCLK2}) **Note:** Enabled by CKDIS register in APB Bridge 2	
46	J4	CK	I		C						Reference clock input	
47	M5	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input. **Note:** This port is input only.
48	L5	N.C.									Not connected (not bonded)	
49	K5	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit	
50	J5	RTCXTO									Output of 32 kHz oscillator amplifier circuit	
51	M6	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby	
52	M7	$\overline{RSTIN}$	I		C_T					X	Reset input	
53	H5	N.C.									Not connected (not bonded)	
54	L6	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.	
55	K6	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.	
56	J6	N.C.									Not connected (not bonded)	
57	H6	N.C.									Not connected (not bonded)	
58	G6	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
59	L7	V_{SS18}	S								Stabilization for main voltage regulator.		
60	K7	N.C.									Not connected (not bonded)		
61	J7	D.0	I/O	6)			8mA				External Memory Interface: data bus		
62	H7	D.1	I/O	6)			8mA						
63	M8	D.2	I/O	6)			8mA						
64	L8	D.3	I/O	6)			8mA						
65	M10	D.4	I/O	6)			8mA						
66	M11	V_{DDA}	S								Supply voltage for A/D Converter		
67	K8	V_{SSA}	S								Ground voltage for A/D Converter		
68	J8	N.C.									Not connected (not bonded)		
69	M9	N.C.									Not connected (not bonded)		
70	L9	N.C.									Not connected (not bonded)		
71	K9	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
72	L10	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
73	M12	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
74	L11	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
75	K11	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
76	K10	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
77	J12	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
78	J11	D.5	I/O	6)			8mA				External Memory Interface: data bus		
79	L12	D.6	I/O	6)			8mA						
80	K12	D.7	I/O	6)			8mA						
81	J10	D.8	I/O	6)			8mA						
82	J9	D.9	I/O	6)			8mA						

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
83	H12	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[4]		
84	H11	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]		
85	H10	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
86	H9	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
87	G12	N.C.									Not connected (not bonded)		
88	F12	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
89	H8	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
90	G11	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
91	G10	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
92	G9	D.10	I/O	6)			8mA				External Memory Interface: data bus		
93	G8	D.11	I/O	6)			8mA						
94	G7	D.12	I/O	6)			8mA						
95	F11	D.13	I/O	6)			8mA						
96	F10	D.14	I/O	6)			8mA						
97	F9	D.15	I/O	6)			8mA						
98	F8	A.0	O	7)			8mA		X		External Memory Interface: address bus		
99	E12	A.1	O	7)			8mA		X				
100	E11	A.2	O	7)			8mA		X				
101	C12	A.3	O	7)			8mA		X				
102	B12	A.4	O	7)			8mA		X				
103	E10	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
104	E9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
105	D12	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
106	D11	P1.10/ USBCLK	I/O	pd	C/ T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
107	D10	P1.13/HCLK/ I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	C11	P1.14/HRXD/ I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	B11	N.C.									Not connected (not bonded)		
110	B10	N.C.									Not connected (not bonded)		
111	C10	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	A9	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
113	B9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
114	C9	A.5	O	[7]			8mA		X		External Memory Interface: address bus		
115	D9	A.6	O	[7]			8mA		X				
116	A11	A.7	O	[7]			8mA		X				
117	A10	A.8	O	[7]			8mA		X				
118	A8	A.9	O	[7]			8mA		X				
119	B8	A.10	O	[7]			8mA		X				
120	C8	A.11	O	[7]			8mA		X				
121	A12	A.12	O	[7]			8mA		X				
122	D8	A.13	O	[7]			8mA		X				
123	E8	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
124	B7	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
125	A7	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
126	A6	P0.3/S0.$\overline{SS}$/ I1.SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
127	C7	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
128	D7	V_{SS18}	S								Stabilization for main voltage regulator.		
129	E7	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
130	F7	A.14	O	7)			8mA		X		External Memory Interface: address bus		
131	B6	A.15	O	7)			8mA		X				
132	C6	A.16	O	7)			8mA		X				
133	D6	A.17	O	7)			8mA		X				
134	E6	A.18	O	7)			8mA		X				
135	A5	A.19	O	7)			8mA		X				
136	B5	$\overline{WE}$.1	O	5)			8mA		X		External Memory Interface: active low MSB write enable output		
137	C5	$\overline{WE}$.0	O	5)			8mA		X		External Memory Interface: active low LSB write enable output		
138	A3	V_{33}	S								Supply voltage for digital I/Os[4]		
139	A2	V_{SS}	S								Ground voltage for digital I/Os[4]		
140	D5	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
141	A4	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
142	B4	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

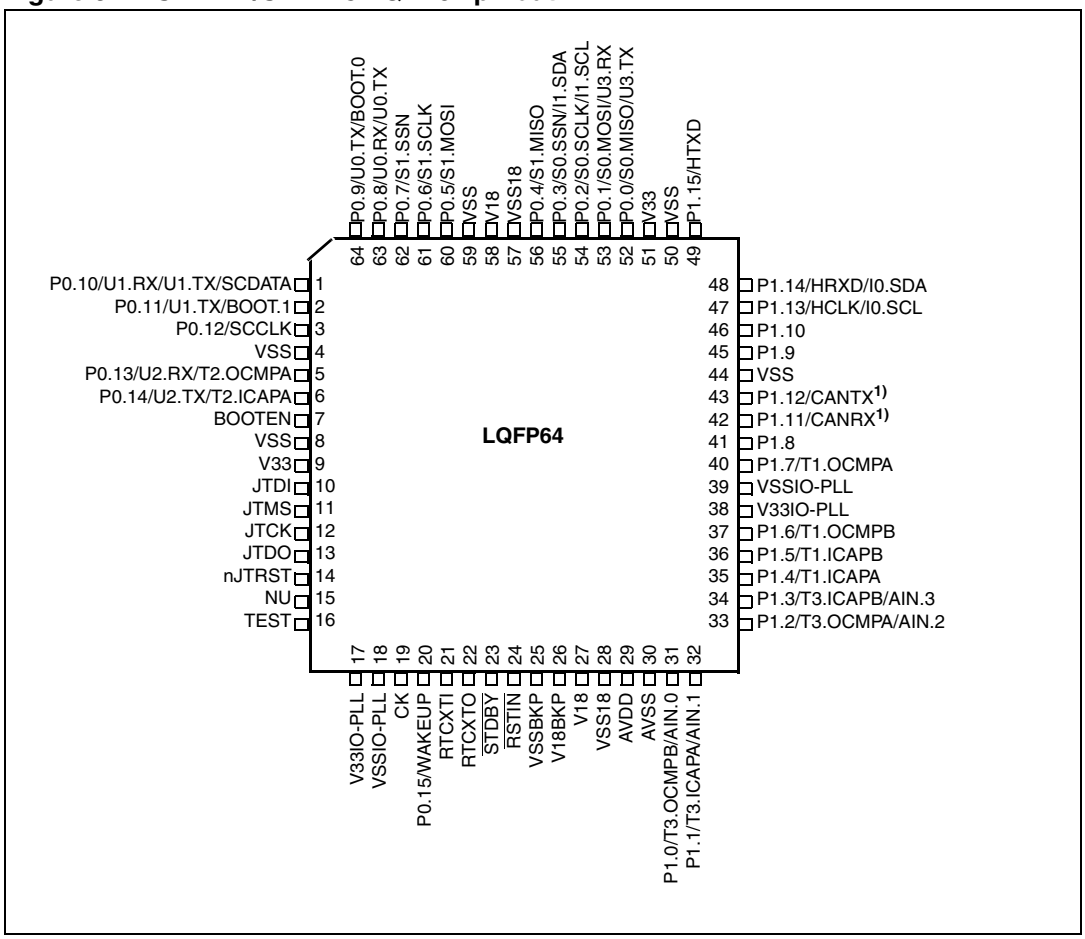
Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
143	C4	P0.8/U0.RX/ U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	B3	P0.9/U0.TX/ BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*) to be used by the External Memory Interface.
3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*).
4. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.
5. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Output Push-Pull.
6. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Hi-Z.
7. During the reset phase, these pins are in input pull-down state. When reset is released, they are configured as Output Push-Pull.
8. During the reset phase, this pin is in input floating state. When reset is released, it is configured as Output Push-Pull.

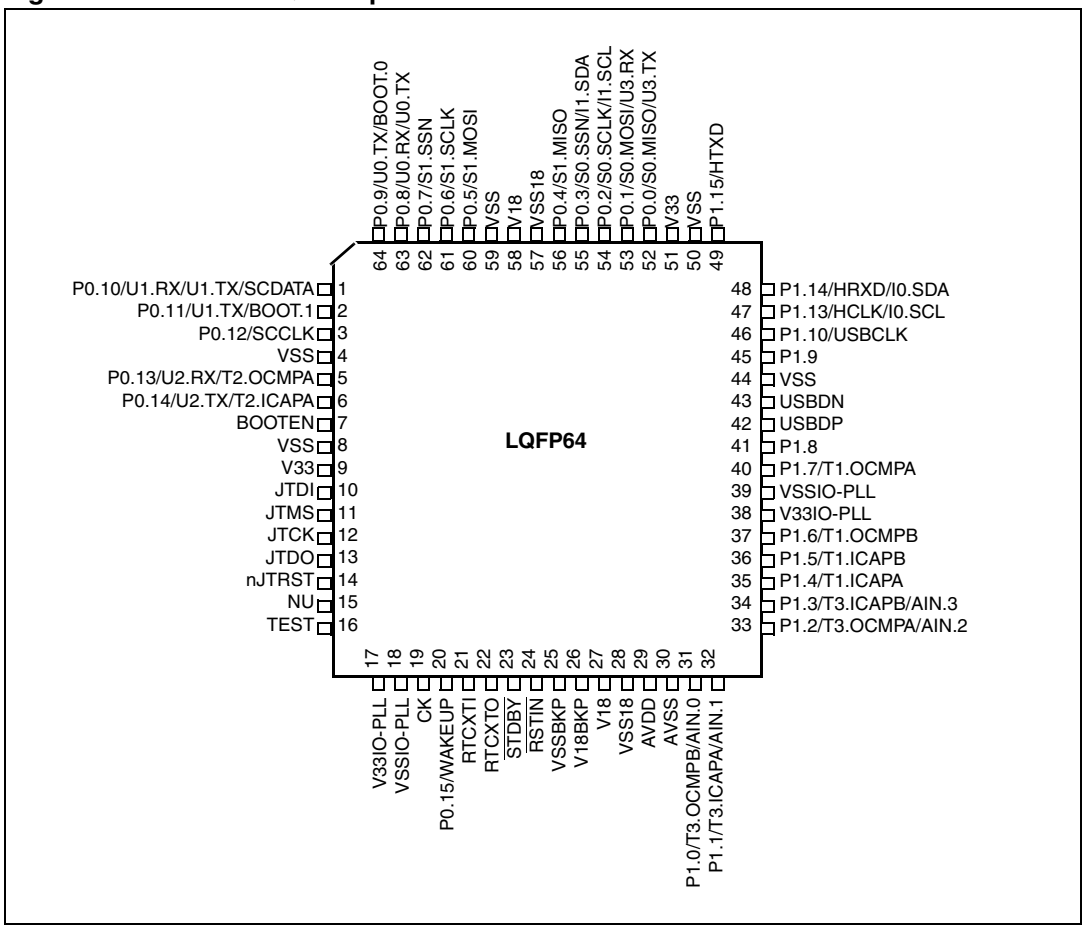
3.4 Pin description for 64-pin packages

Figure 3. STR712/STR715 LQFP64 pinout



1. CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Figure 4. STR711 LQFP64 pinout



Legend / abbreviations for *Table 5*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8V / 2V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 5. STR711/STR712/STR715 pin description

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
											Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
4	V_{SS}	S								Ground voltage for digital I/Os[2]		
5	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
6	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
7	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins		
8	V_{SS}	S								Ground voltage for digital I/Os[2]		
9	V_{33}	S								Supply voltage for digital I/Os[2]		
10	JTDI	I		T_T						JTAG Data input. External pull-up required.		
11	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.		
12	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.		
13	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.		
14	JTRST	I		T_T						JTAG Reset Input. External pull-up required.		
15	NU									Reserved, must be forced to ground.		
16	TEST									Reserved, must be forced to ground.		
17	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
18	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
19	CK	I		C						Reference clock input		

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
20	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input.	
										Note: This port is input only.		
21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby.		
24	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.		
26	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
28	V_{SS18}	S								Stabilization for main voltage regulator.		
29	V_{DDA}	S								Supply voltage for A/D Converter		
30	V_{SSA}	S								Ground voltage for A/D Converter		
31	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
35	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
36	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
37	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
38	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
39	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
40	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
41	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
42	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
43	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
42	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
43	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
44	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
45	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
46	P1.10/USBCLK	I/O	pd	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
47	P1.13/HCLK/I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
48	P1.14/HRXD/I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
49	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
50	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
51	V_{33}	S								Supply voltage for digital I/O circuitry[2]		

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n° LQFP64	Pin name	Type	Reset state[1]	Input: Input level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

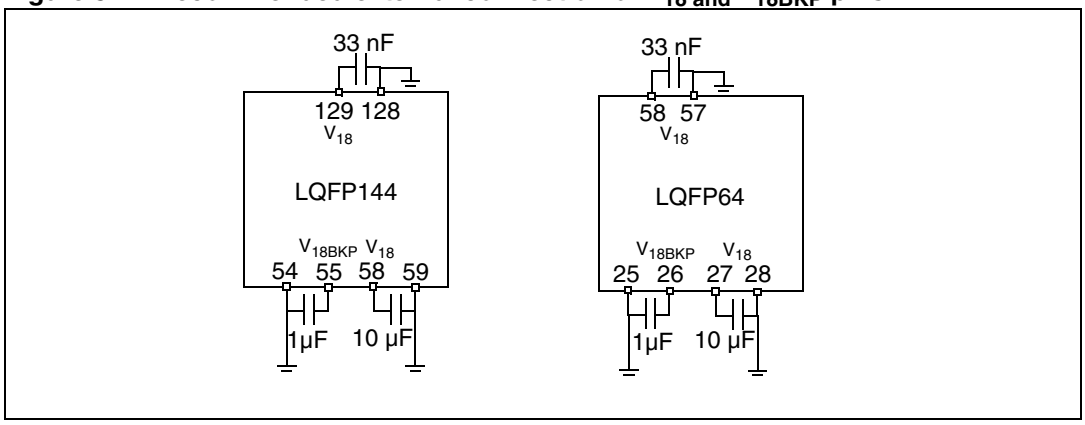
Table 5. STR711/STR712/STR715 pin description (continued)

Pin n° LQFP64	Pin name	Type	Reset state[1]	Input: Input level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
63	P0.8/U0.RX/U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
										Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
64	P0.9/U0.TX/BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.

3.5 External connections

Figure 5. Recommended external connection of V_{18} and V_{18BKP} pins



3.6 I/O port configuration

Table 6. Port bit configuration table

Configuration mode		Input buffer	PxD register		PxC2 register	PxC1 register	PxC0 register
			Read access	Write access			
INPUT	TTL Input Floating	TTL floating	I/O pin	don't care	0	0	1
	CMOS Input Floating	CMOS floating	I/O pin	don't care	0	1	0
	CMOS Input Pull-Down (IPUPD)	CMOS Pull-Down	I/O pin	0	0	1	1
	CMOS Input Pull-Up (IPUPD)	CMOS Pull-Up	I/O pin	1	0	1	1
	Analog input	AIN	0	don't care	0	0	0
OUTPUT	Output Open-Drain	N.A.	I/O pin	0 or 1	1	0	0
	Output Push-Pull	N.A.	last value written	0 or 1	1	0	1
	Alternate Function Open-Drain	CMOS floating	I/O pin	don't care	1	1	0
	Alternate Function Push-Pull	CMOS floating	I/O pin	don't care	1	1	1

Legend:

AIN: Analog Input

CMOS: CMOS Input levels

IPUPD: Input Pull Up /Pull Down

TTL: TTL Input levels

N.A.: not applicable. In Output mode, a read access to the port gets the output latch value.

3.7 Memory mapping

Figure 6. Memory map

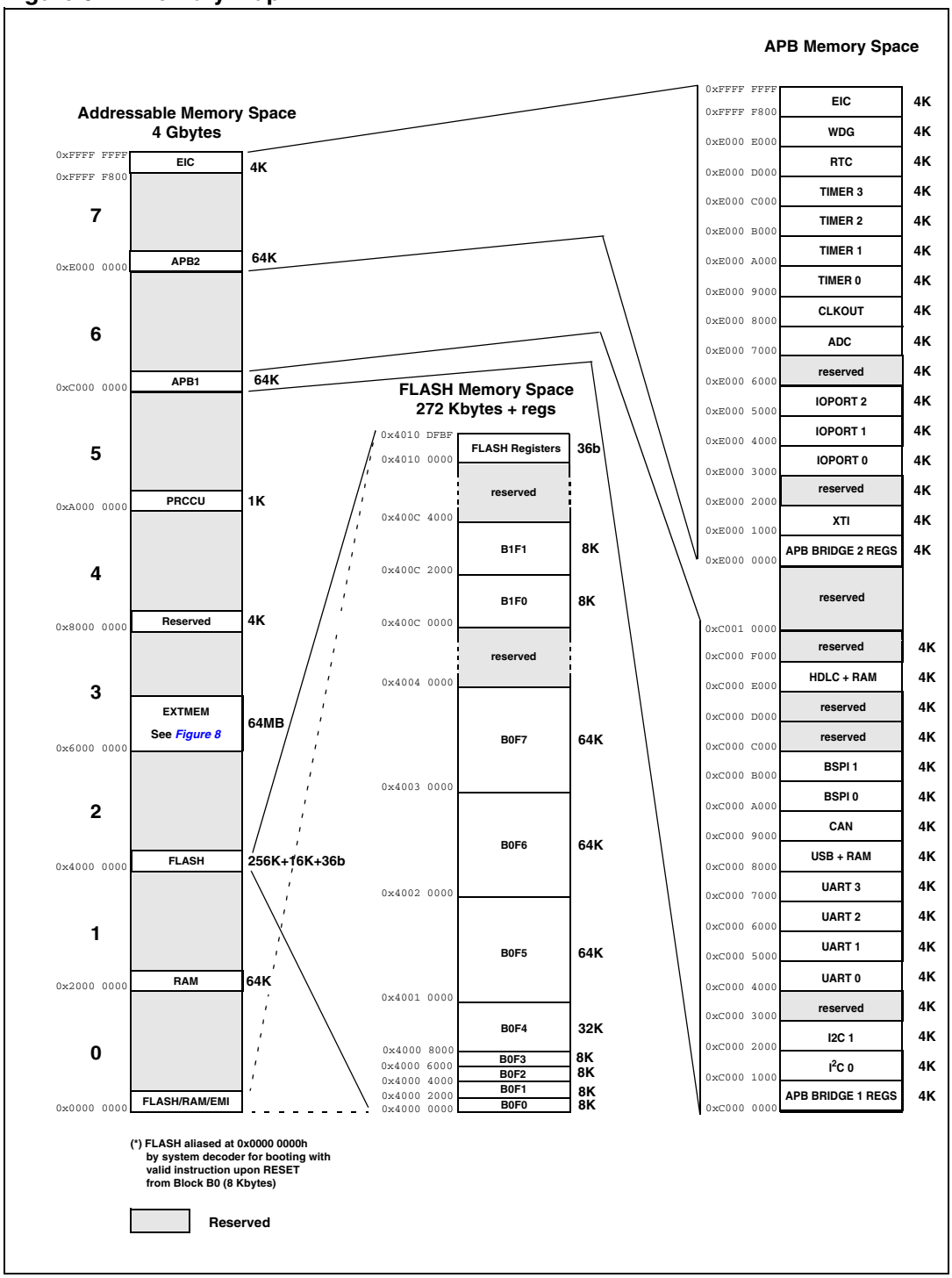


Figure 7. Mapping of Flash memory versions

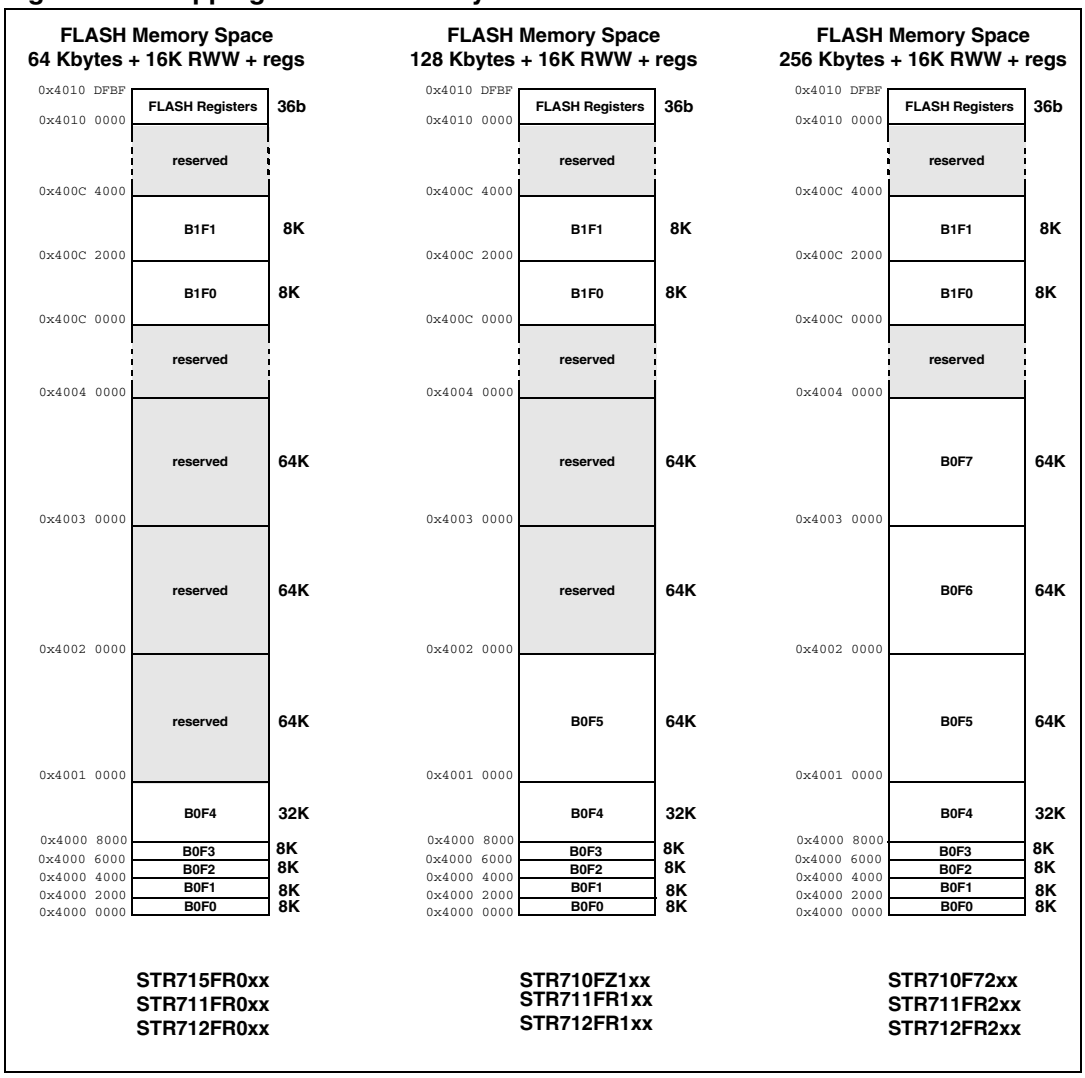
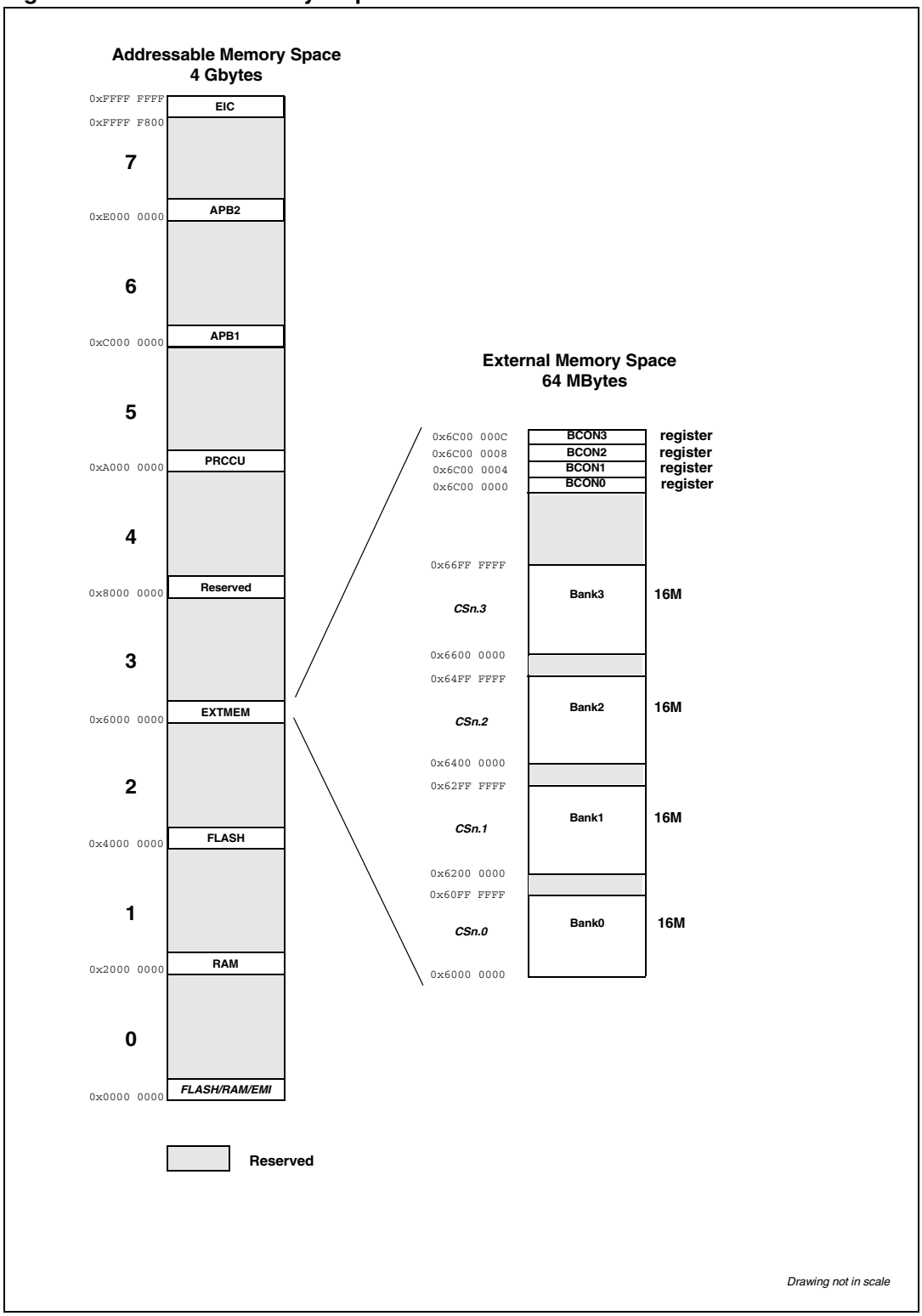


Table 7. RAM memory mapping

Part number	RAM size	Start address	End address
STR715FR0xx STR711FR0xx STR712FR0xx	16 Kbytes	0x2000 0000	0x2000 3FFF
STR710FZ1xx STR711FR1xx STR712FR1xx	32 Kbytes	0x2000 0000	0x2000 7FFF
STR710FR2xx STR710Rxx STR711FR2xx STR712FR2xx	64 Kbytes	0x2000 0000	0x2000 FFFF

Figure 8. External memory map



4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{33}=3.3V (for the 3.0V≤V_{33}≤3.6V voltage range) and V_{18}=1.8V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

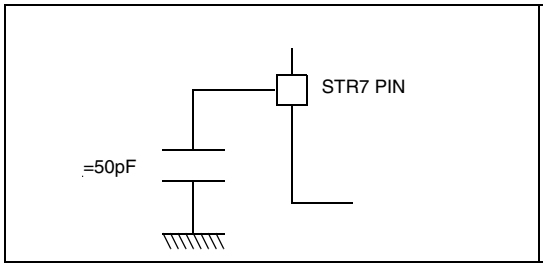
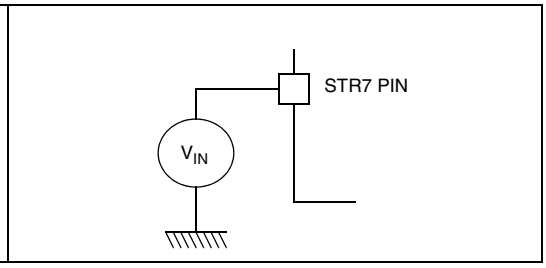


Figure 10. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{33}- V_{SS}	External 3.3V Supply voltage (including AV_{DD} and $V_{33IO-PLL}$)[2]	-0.3	4.0	V
V_{18BKP} - V_{SSBKP}	Digital 1.8V Supply voltage on V_{18BKP} backup supply [2]	-0.3	2.0	
V_{IN}	Input voltage on true open drain pin (P0.10) [1]	V_{SS}-0.3	+5.5	
	Input voltage on any other pin [1]	V_{SS}-0.3	V_{33}+0.3	
$\|\Delta V_{33x}\|$	Variations between different 3.3V power pins	50	50	mV
$\|\Delta V_{18x}\|$	Variations between different 1.8V power pins [5]	25	25	
$\|V_{SSX}$ - $V_{SS}\|$	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 49*		
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
I_{V33}	Total current into $V_{33}/V_{33IO-PLL}$ power lines (source) [2]	150	mA
I_{VSS}	Total current out of $V_{SS}/V_{SSIO-PLL}$ ground lines (sink) [2]	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ [1] [3]	Injected current on $\overline{RSTIN}$ pin	± 5	
	Injected current on CK pin	± 5	
	Injected current on any other pin [4]	± 5	
$\Sigma I_{INJ(PIN)}$ [1]	Total injected current (sum of all I/O and control pins) [4]	± 25	

The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected. Data based on T_A = 25 °C.

All 3.3V power (V_{33}, AV_{DD}, $V_{33IO-PLL}$) and ground (V_{SS}, AV_{SS}, $V_{SSIO-PLL}$) pins must always be connected to the external 3.3V supply.

Negative injection disturbs the analog performance of the device. See note in *Section 4.3.11: ADC characteristics on page 66*.

When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Only when using external 1.8V power supply. All the power (V_{18}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8V supply.

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 73*)		

4.3 Operating conditions

Subject to general operating conditions for V_{33}, and T_A.

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU Clock frequency	Accessing SRAM or external memory with 0 wait states	0	66	MHz
		Accessing FLASH in burst mode	0	50	
		Executing from FLASH with RWW	0	45 [1)]	
		Accessing FLASH with 0 wait states	0	33	
f_{PCLK}	Internal APB Clock frequency		0	33	MHz
V_{33}	Standard Operating Voltage (includes V_{33I0_PLL})		3.0	3.6	V
V_{18BKP}	Backup Operating Voltage		1.4	1.8	V
T_A	Ambient temperature range	6 Partnumber Suffix	-40	85	°C

1. Data guaranteed by characterization, not tested in production

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{V33}	V_{33} rise time rate	Subject to general operating conditions for T_A.	20			µs/V
					20	ms/V

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 34* and *Figure 10 on page 34*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{33} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8V (except if explicitly mentioned)

Subject to general operating conditions for V_{33}, and T_A.

Table 13. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD} [4]	Supply current in RUN mode	f_{MCLK}=66 MHz, RAM execution	73.6	100	mA
		f_{MCLK}=32 MHz, Flash non-burst execution	49.3		
	Supply current in STOP mode	T_A=25°C	10	50[3]	µA
	Supply current in STANDBY mode	OSC32K bypassed	12	30	µA

Notes:

1. Typical data are based on T_A=25°C, V_{33}=3.3V.
2. Data based on characterization results, tested in production at V_{33}, f_{MCLK} max. and T_A max.
3. Based on device characterisation, device power consumption in STOP mode at T_A 25°C is predicted to be 30µA or less in 99.730020% of parts.
4. The conditions for these consumption measurements are described in application note AN2100.

Table 14. Typical power consumption data

Symbol	Parameter		Conditions	Typical current on V33	Unit
I_{DDRUN}	RUN mode current from RAM	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	23	mA
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	40	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	50	
			MCLK = 64 MHz, PCLK1 = PCLK2 = 32 MHz	63	
		All periphs OFF	MCLK = 16 MHz	16	
			MCLK = 32 MHz	26	
			MCLK = 48 MHz	39	
			MCLK = 64 MHz	48	
	RUN mode current from FLASH	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	27	
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	47	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	62	
		All periphs OFF	MCLK = 16 MHz	21	
			MCLK = 32 MHz	36	
			MCLK = 48 MHz	53	
I_{DDSLOW}	SLOW mode current		MCLK = CK_AF (32 kHz), MVR off	1.7	
I_{DDWAIT}	WAIT mode current (all periphs ON)		PCLK1 = PCLK2 = 1 MHz	13	
$I_{DDLPWAIT}$	LPWAIT mode current		CK_AF (32 kHz), Main VReg off, FLASH in power-down	37	µA
I_{DDSTOP}	STOP mode current		Main VReg off, FLASH in power down, RTC on	18	
			Main VReg off, FLASH in power down, RTC off	10	
I_{DDSB}	STANDBY mode current		LP VReg on, LVD on, RTC on	10	
			LP VReg off (ext 1.8V on V18BKP), LVD on, RTC on	9	
			LP VReg off (ext1.8V on V18BKP), LVD off, RTC on	5	
			LP VReg off (ext 1.8V on V18BKP), LVD off, RTC off	1	

Figure 11. STOP I_{DD} vs. V_{33}

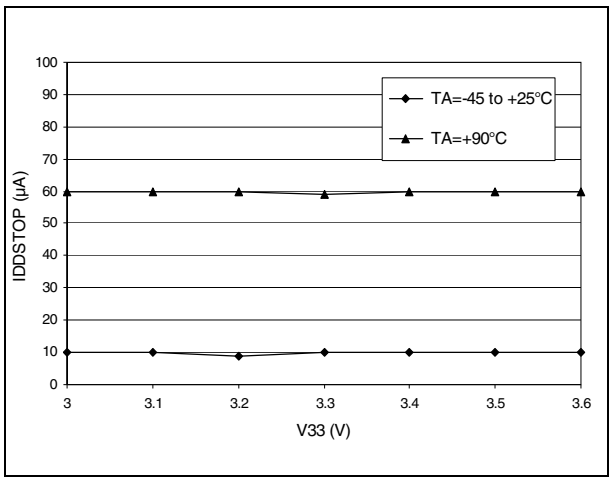


Figure 12. STANDBY I_{DD} vs. V_{33}

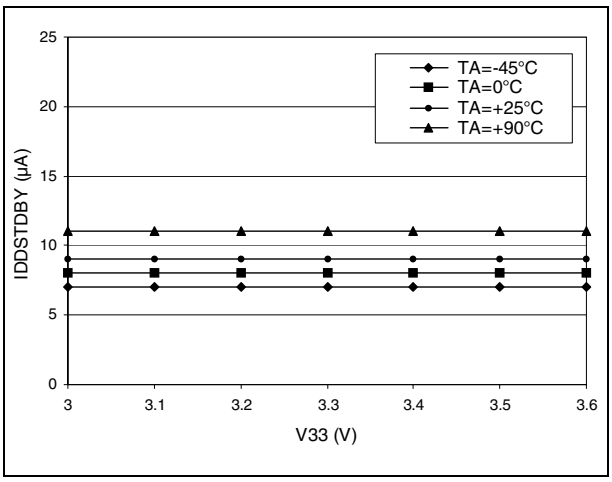
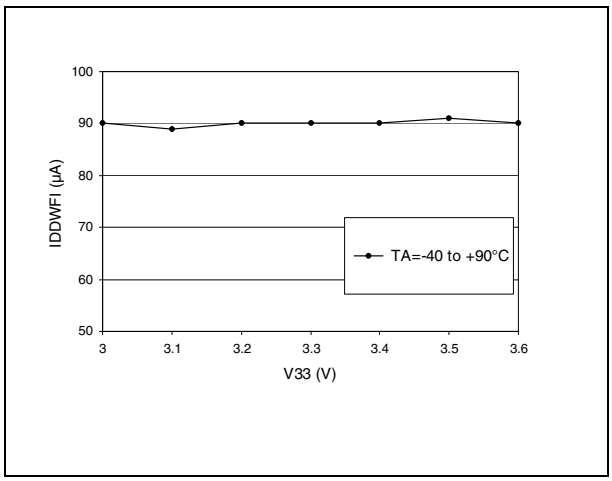


Figure 13. WFI I_{DD} vs. V_{33}



On-chip peripherals

Table 15. Peripheral current consumption

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(PLL1)}$	PLL1 supply current	T_A= 25°C	3.42	mA
$I_{DD(PLL2)}$	PLL2 supply current		5.81	
$I_{DD(TIM)}$	TIM Timer supply current [1]	T_A= 25°C, f_{PCLK1}= f_{PCLK2}=33 MHz	0.88	
$I_{DD(BSPI)}$	BSPI supply current [2]		1.1	
$I_{DD(UART)}$	UART supply current [2]		1.05	
$I_{DD(I2C)}$	I2C supply current [2]		0.45	
$I_{DD(ADC)}$	ADC supply current when converting [5]		1.89	
$I_{DD(HDLC)}$	HDLC supply current [2]		1.82	
$I_{DD(USB)}$	USB supply current [2]		2.08	
$I_{DD(CAN)}$	CAN supply current [2]		1.11	

Notes:

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16MHz. No IC/OC programmed (no I/O pads toggling).
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.2 Clock and timing characteristics

External clock sources

Subject to general operating conditions for V_{33}, and T_A.

Table 16. CK external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	External clock source frequency		0		16.5	MHz
V_{CKH}	CK input pin high level voltage		$0.7xV_{33}$		V_{33}	V
V_{CKL}	CK input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(CK)}$ $t_{w(CK)}$	CK high or low time [1]		25			ns
$t_{r(CK)}$ $t_{f(CK)}$	CK rise or fall time [1]				20	
$C_{IN(CK)}$	CK input capacitance[1]			5		pF
DuCy(XT1)	Duty cycle		40		60	%
I_L	CK Input leakage current	$V_{SS} \leq V_{IN} \leq V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 14. CK external clock source

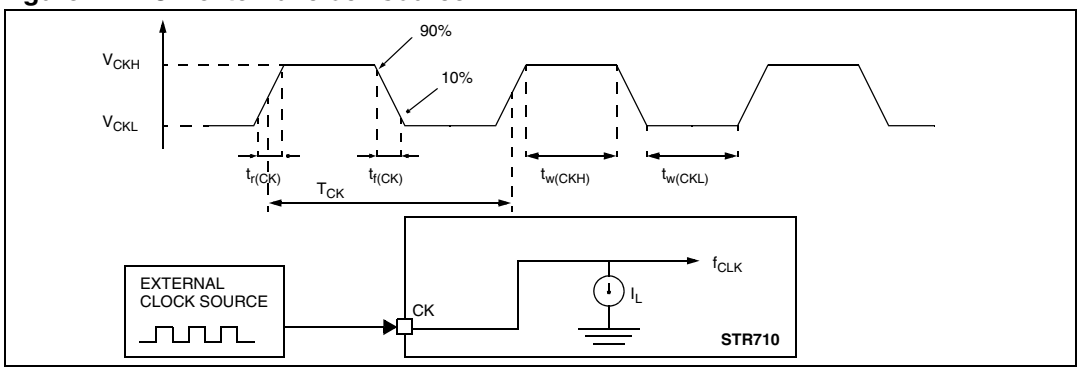


Table 17. RTCXT1 external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RTCXT1}	External clock source frequency		0		500	kHz
$V_{RTCXT1H}$	RTCXT1 input pin high level voltage		$0.7xV_{33}$		V_{33}	V
$V_{RTCXT1L}$	RTCXT1 input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(RTCXT1)}$ $t_{w(RTCXT1)}$	RTCXT1 high or low time [1]		100			ns
$t_{r(RTCXT1)}$ $t_{f(RTCXT1)}$	RTCXT1 rise or fall time [1]				5	
$C_{IN(RTCXT1)}$	RTCXT1 input capacitance[1]			5		pF
DuCy(RTCXT1)	Duty cycle		30		70	%
I_L	RTCXT1 Input leakage current	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

OSC32K crystal / ceramic resonator oscillator

The STR7 RTC clock can be supplied with a 32 kHz Crystal/Ceramic resonator oscillators. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 18. 32K oscillator characteristics ($f_{OSC32K=}$ 32.768 kHz)

Symbol	Parameter	Conditions	Typ	Unit
R_F	Feedback resistor		2.7	MΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)[1)]	R_S=40K Ω	12.5	pF
i_2	RTCXT2 driving current	V_{33}=3.3 V V_{IN}=V_{SS}	3.2	µA
g_m	Oscillator Transconductance		8	µA/V
$t_{SU(OSC32KHZ)}$[2)]	Startup time	V_{33} is stabilized	5	s

Notes:

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
2. $t_{SU(OSC32KHZ)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 15. Typical application with a 32 kHz crystal

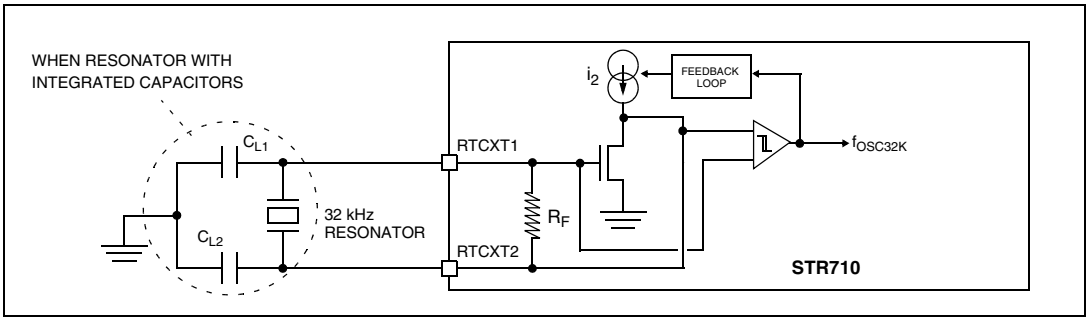
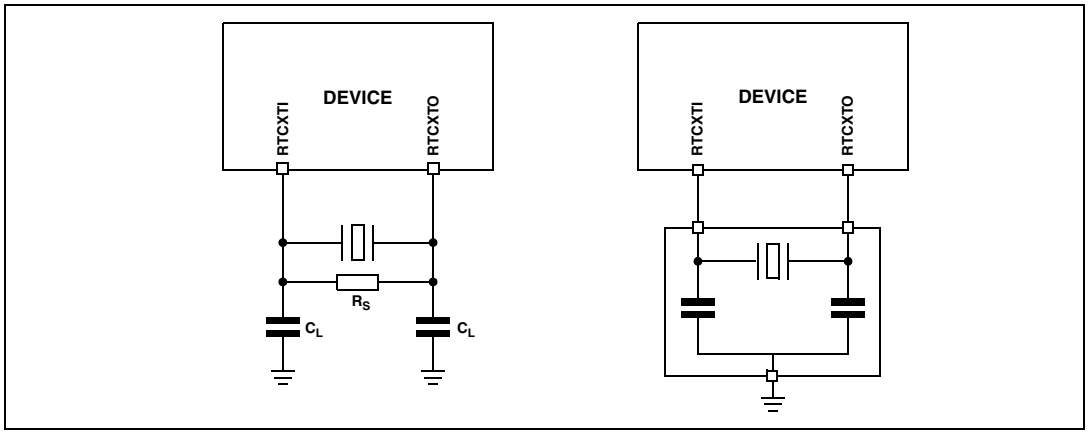


Figure 16. RTC crystal oscillator and resonator



PLL electrical characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. PLL1 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock				165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs

Table 19. PLL1 characteristics (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$\Delta t_{JITTER1}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 20. PLL2 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK2}$	PLL multiplier output clock				140	MHz
f_{PLL2}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1	3.0		5	MHz
t_{LOCK2}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
$\Delta t_{JITTER2}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 21. Low-power mode wakeup timing

Symbol	Parameter	Typ	Unit
$t_{WULPWFI}$	Wakeup from LPWFI mode	26(1)	µs
t_{WUSTOP}	Wakeup from STOP mode	2048	CLK Cycles (2)
t_{WUSTBY}	Wakeup from STANDBY mode	2048 CLK Cycles + 8 CLK2 Cycles(3)	Cycles

1. Clock selected is CK2_16, Main VReg OFF and Flash in power-down
2. The CLK clock is derived from the external oscillator.
3. Refer to Figure 7. Reset General Timing in the STR71xF Reference Manual (UM0084)

4.3.3 Memory characteristics

Flash memory

V_{33} = 3.0 to 3.6V, T_A = -40 to 85 °C unless otherwise specified.

Table 22. Flash memory characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ	Max[1]	
t_{PW}	Word Program			40		µs
t_{PDW}	Double Word Program			60		µs
t_{PB0}	Bank 0 Program (256K)	Double Word Program		1.6	2.1	s
t_{PB1}	Bank 1 Program (16K)	Double Word Program		130	170	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed Preprogrammed		2.3 1.9	4.0 3.3	s
t_{ES}	Sector Erase (8K)	Not preprogrammed Preprogrammed		0.7 0.6	1.1 1.0	s
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed Preprogrammed		8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed Preprogrammed		0.9 0.8	1.5 1.3	s
t_{RPD}[2]	Recovery when disabled				20	µs
t_{PSL}[2]	Program Suspend Latency				10	µs
t_{ESL}[2]	Erase Suspend Latency				300	µs
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
t_{RET}	Data Retention (Bank 0 and Bank 1)	T_A=85°	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

Notes:

1. T_A=45°C after 0 cycles. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

In the case of an ARM7 CPU, in order to write robust code that can withstand all kinds of stress, such as very strong electromagnetic disturbance, it is mandatory that the Data Abort, Prefetch Abort and Undefined Instruction exceptions are managed by the application software. This will prevent the code going into an undefined state or performing any unexpected operation.

Table 23. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{33}=3.3 V, T_A=+25°C, f_{MCLK}=32 MHz conforms to IEC 1000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{33}=3.3 V, T_A=+25°C, f_{MCLK}=32 MHz conforms to IEC 1000-4-4	4A

Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 24. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC4M}/f_{HCLK}]		Unit
				16/ 48 MHz	16/8 MHz	
S_{EMI}	Peak level	V_{33}=3.3 V, T_A=+25°C, LQFP64 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	17	19	dBµV
			30 MHz to 130 MHz	17	16	
			130 MHz to 1 GHz	11	11	
			SAE EMI Level	4	3	-

Notes:

1. Not tested in production.
2. BGA and LQFP devices have similar EMI characteristics.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Table 25. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical sensitivities

Table 26. Static and dynamic latch-up

Symbol	Parameter	Conditions	Class[1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}=3.3 V, f_{OSC4M}=4 MHz, f_{MCLK}=32 MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{33} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 27. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage 1)	CMOS ports			$0.3V_{33}$	V
V_{IH}	Input high level voltage 1)		$0.7V_{33}$			
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.8		V
V_{IL}	Input low level voltage 1)	P0.15 WAKEUP		0.9	0.8	V
V_{IH}	Input high level voltage 1)		2	1.35		
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.4		V
V_{IL}	Input low level voltage 1)	TTL ports			0.8	V
V_{IH}	Input high level voltage 1)		2.0			
$I_{INJ(PIN)}$	Injected Current on any I/O pin				± 4	mA
$\Sigma I_{INJ(PIN)}$ 3)	Total injected current (sum of all I/O and control pins)				± 25	
I_{lkg}	Input leakage current 4)	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA
R_{PU}	Weak pull-up equivalent resistor5)	$V_{IN}=V_{SS}$	110	150	700	kΩ
R_{PD}	Weak pull-down equivalent resistor5)	$V_{IN}=V_{33}$	110	150	700	kΩ
C_{IO}	I/O pin capacitance			5		pF

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 35* for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 18* to *Figure 19*).

Figure 17. R_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

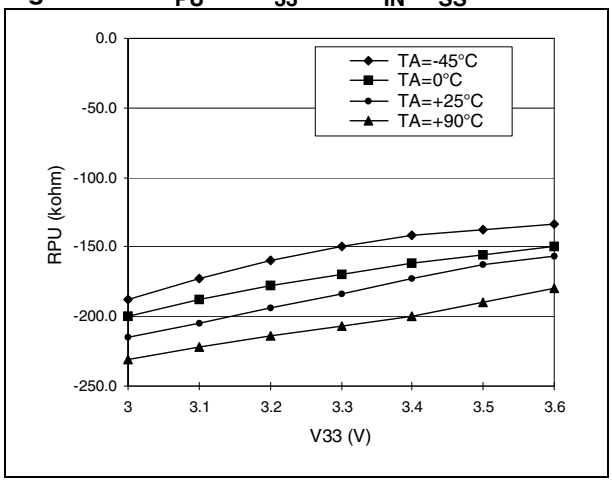


Figure 18. I_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

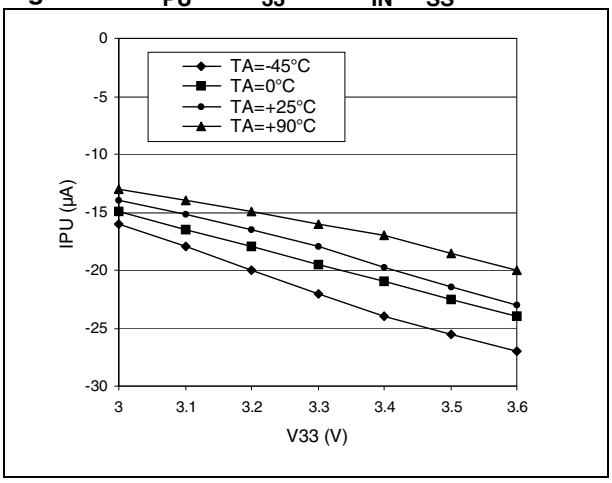


Figure 19. R_{PD} vs. V_{33} with $V_{IN}=V_{33}$

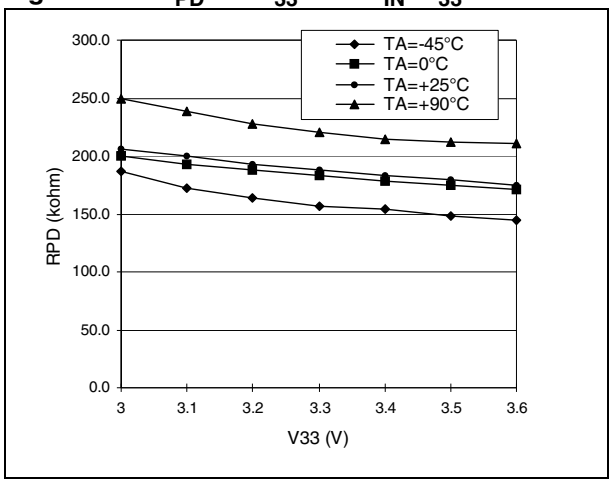
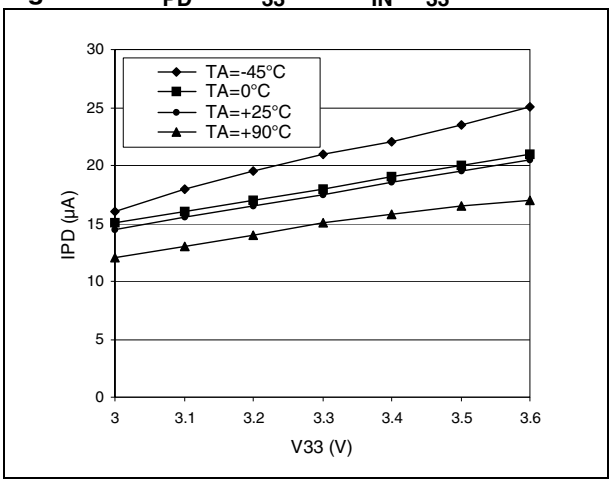


Figure 20. I_{PD} vs. V_{33} with $V_{IN}=V_{33}$



Output driving current

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 28. Output driving current

I/O type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+4mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4mA	V_{33}-0.8		
High Current	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+8mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8mA	V_{33}-0.8		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 9* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 9* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{V33}.

Figure 21. Typical V_{OL} and V_{OH} at V_{33}=3.3V (high current ports)

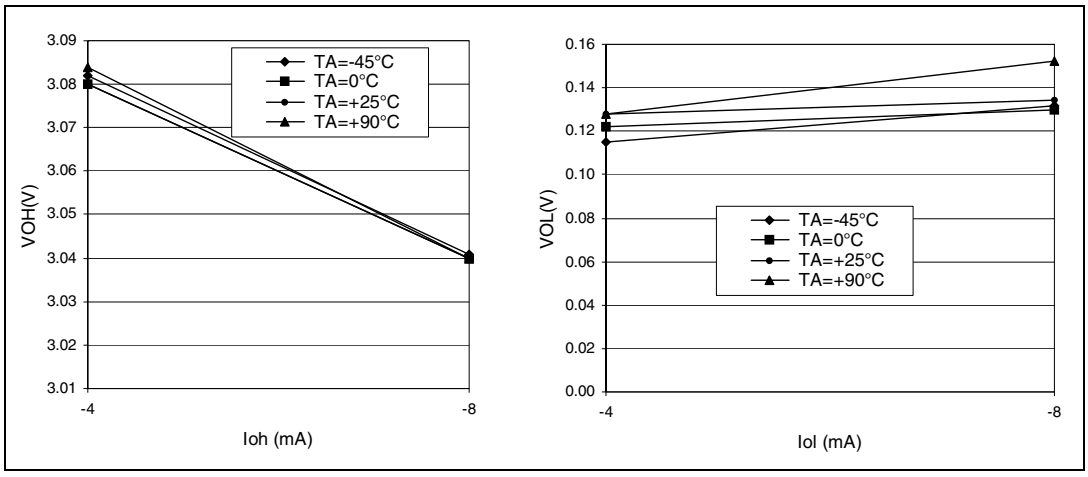


Figure 22. Typical V_{OL} vs. V_{33}

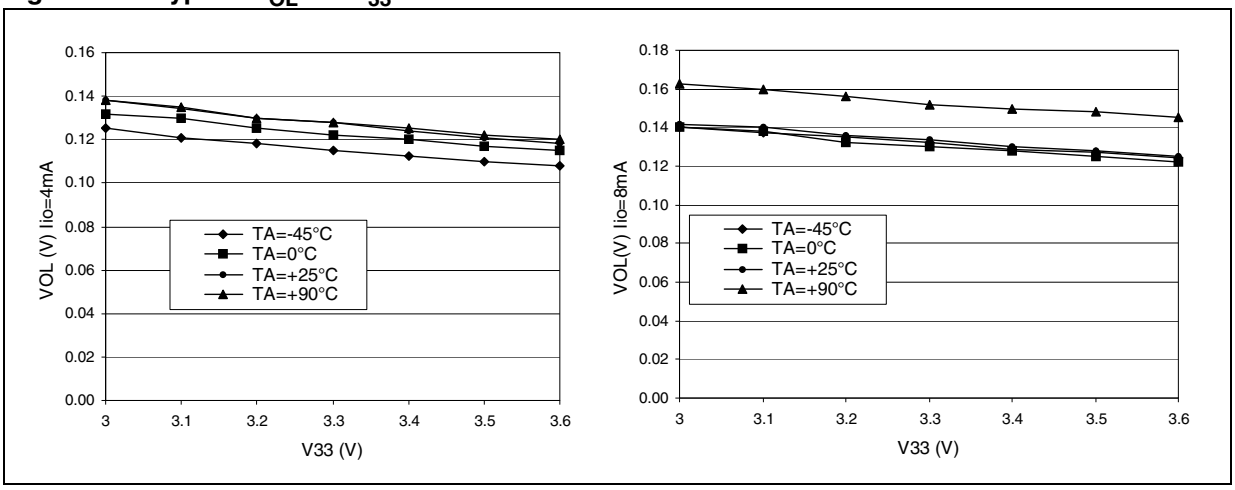
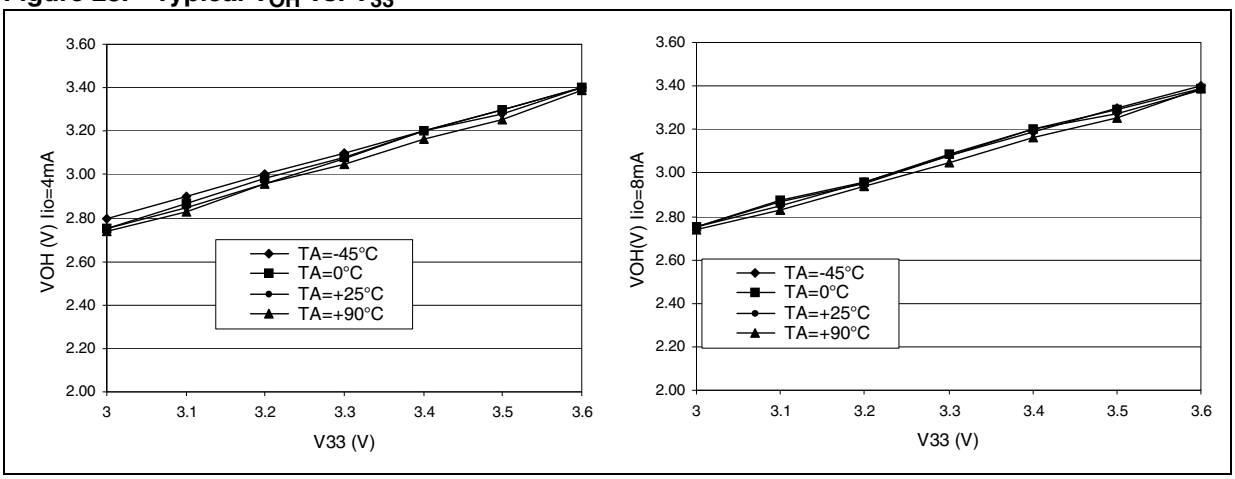


Figure 23. Typical V_{OH} vs. V_{33}



$\overline{\text{RSTIN}}$ pin

The $\overline{\text{RSTIN}}$ pin input driver is CMOS. A permanent pull-up is present which is the same as as R_{PU} (see *Table 27 on page 51*)

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 29. $\overline{\text{RESET}}$ pin characteristics

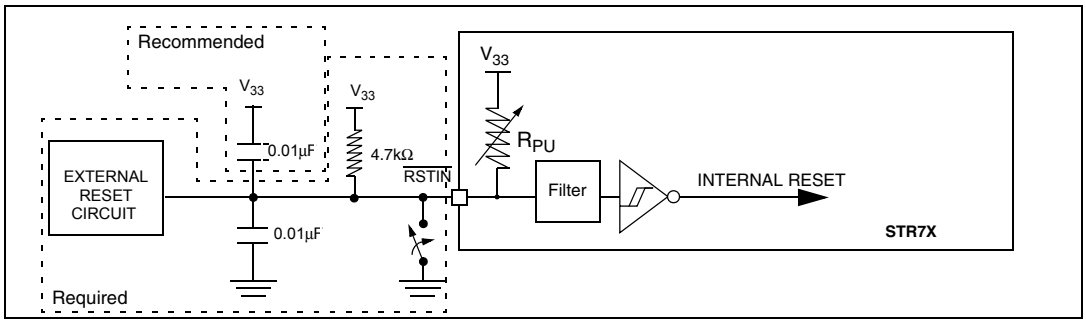
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(RSTINn)}$	$\overline{\text{RSTIN}}$ Input low level voltage [1]				0.8	V
$V_{IH(RSTINn)}$	$\overline{\text{RSTIN}}$ Input high level voltage [1]		2			
$V_{F(RSTINn)}$	$\overline{\text{RSTIN}}$ Input filtered pulse[2]				500	ns
$V_{NF(RSTINn)}$	$\overline{\text{RSTIN}}$ Input not filtered pulse[2]		1.2			µs

Notes:

1. Data based on characterization results, not tested in production.

2) Data guaranteed by design, not tested in production.

Figure 24. Recommended $\overline{\text{RSTIN}}$ pin protection.[1]



Notes:

1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 18*).
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the $\overline{\text{RSTIN}}$ pin can go below the $V_{IL(RSTINn)}$ max. level specified in *Table 29*. Otherwise the reset will not be taken into account internally.

4.3.6 TIM timer characteristics

Subject to general operating conditions for V_{33}, f_{MCLK}, and T_A unless otherwise specified.

Refer to *Section 4.3.5: I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 30. TIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time		1			t_{PCLK2}
		f_{PCLK2} = 30 MHz	33.3			ns
f_{EXT}	Timer external clock frequency	$f_{CK\_TIM(MAX)} = f_{MCLK}$	0		$f_{CK\_TIM}/4$	MHz
		$f_{CK\_TIM} = f_{MCLK}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution				16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected		1		65536	t_{PCLK2}
		f_{PCLK2} = 30 MHz	0.033		2184	µs
T_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{PCLK}
		f_{PCLK2} = 30 MHz			143.1	s

4.3.7 EMI - external memory interface

Subject to general operating conditions for V_{DD}, f_{HCLK}, and T_A unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Table 31. EMI general characteristics

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	1 / f_{MCLK}
t_C	Memory cycle time wait states	t_{MCLK} x (1 + [C_LENGTH])

Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Figure 25. Read cycle timing: 16-bit read on 16-bit memory

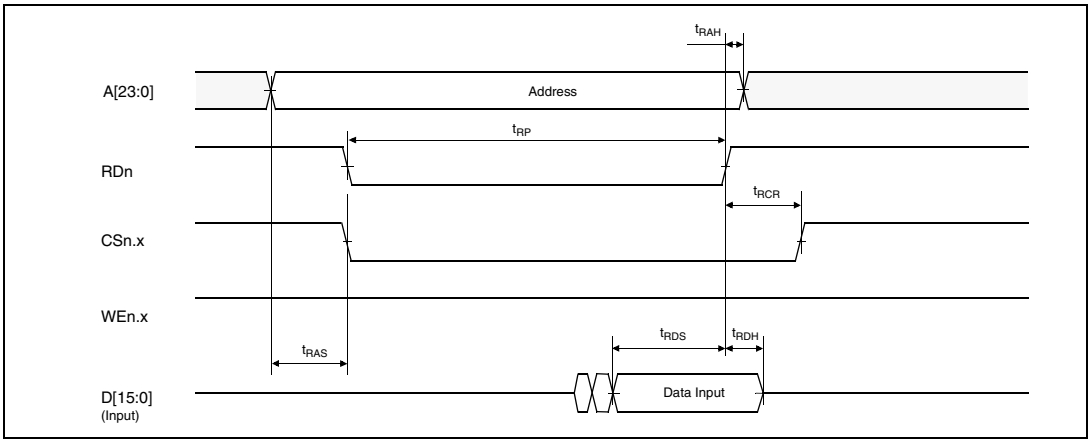
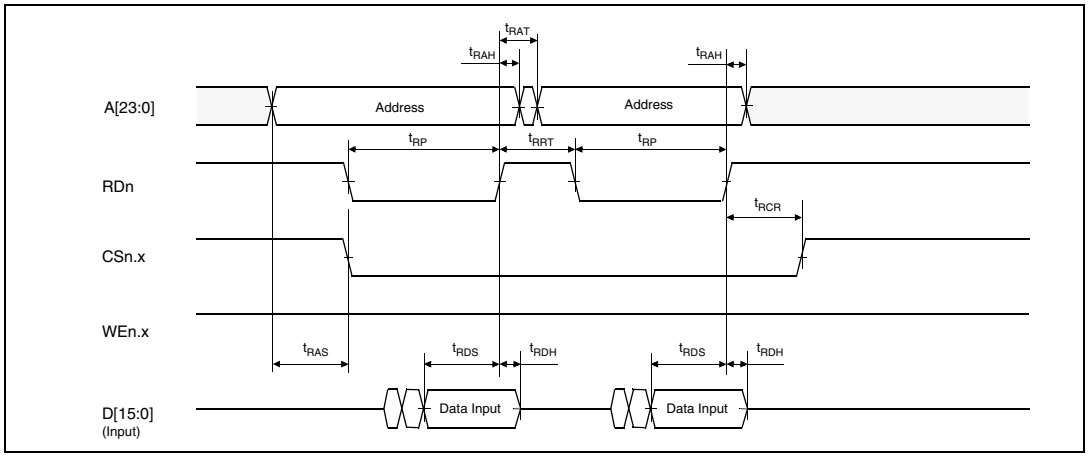


Figure 26. Read cycle timing: 32-bit read on 16-bit memory



See *Table 32* for read timing data.

Figure 27. Read cycle timing: 16-bit read on 8-bit memory

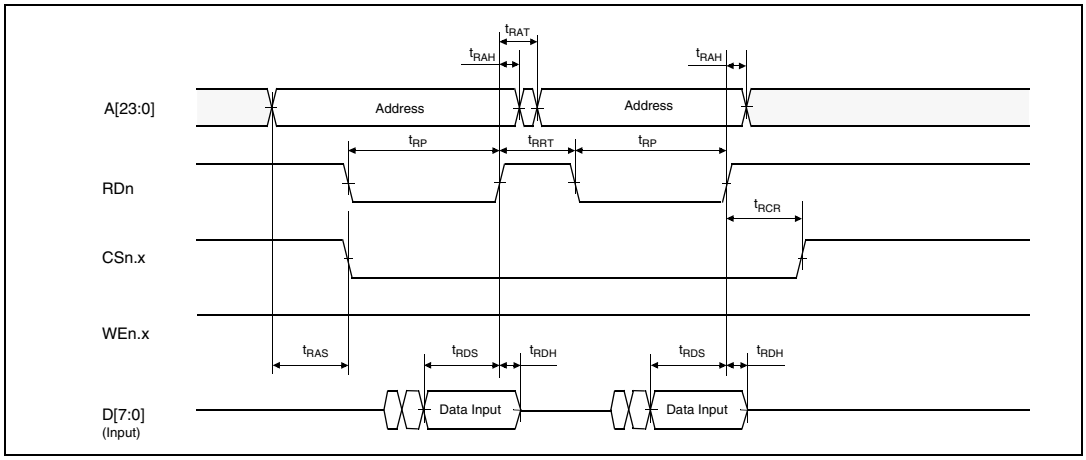
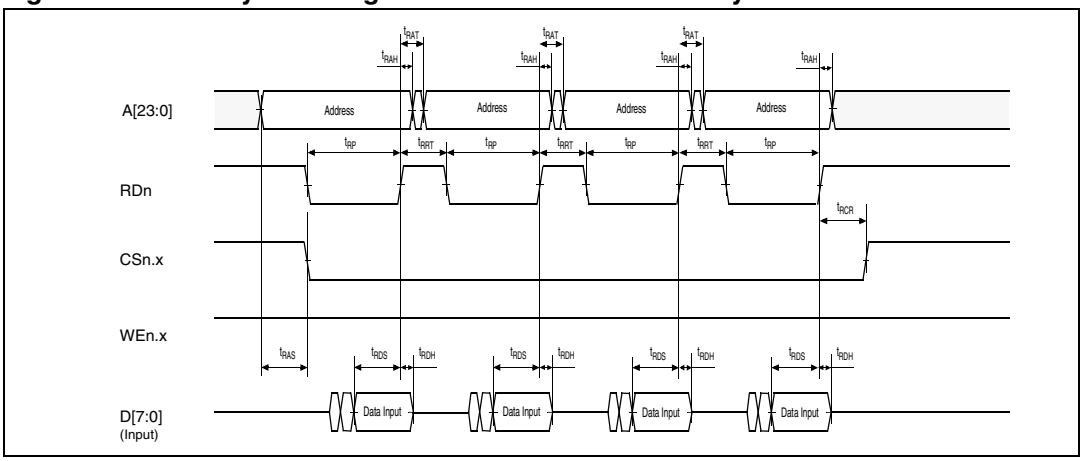


Figure 28. Read cycle timing: 32-bit read on 8-bit memory



See *Table 32* for read timing data.

Figure 29. Write cycle timing: 16-bit write on 16-bit memory

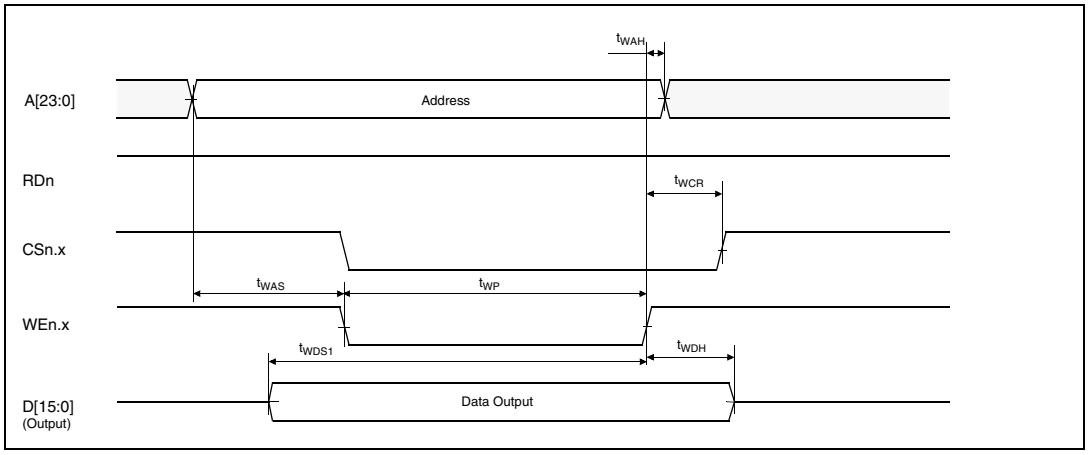
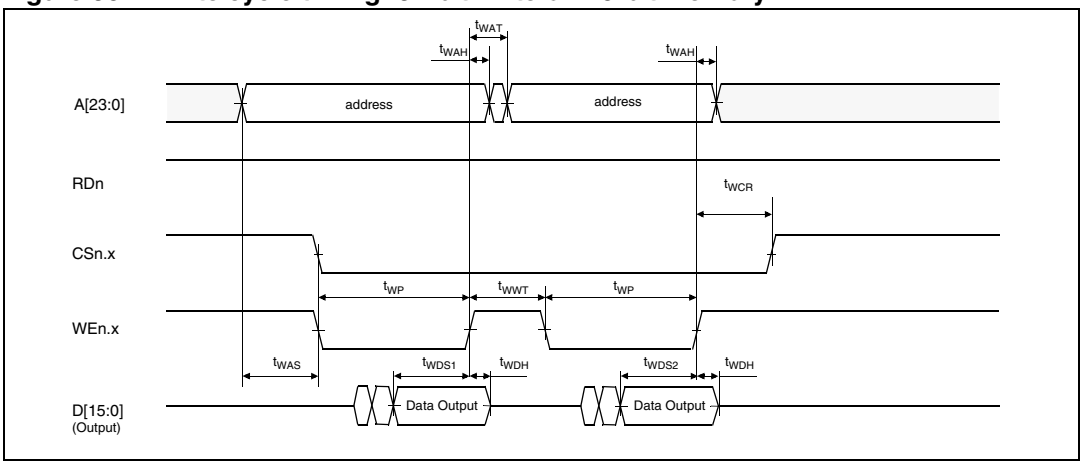


Figure 30. Write cycle timing: 32-bit write on 16-bit memory



See *Table 44* for write timing data.

Figure 31. Write cycle timing: 16-bit write on 8-bit memory

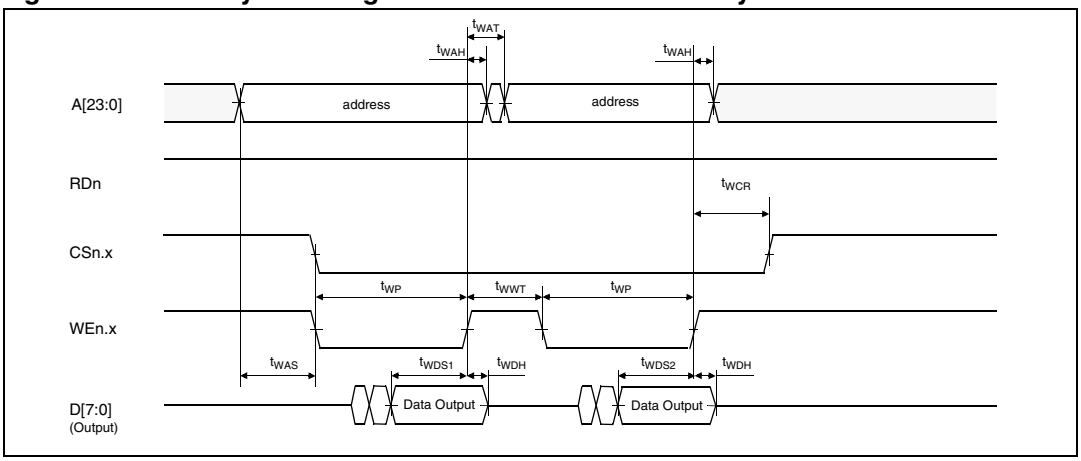
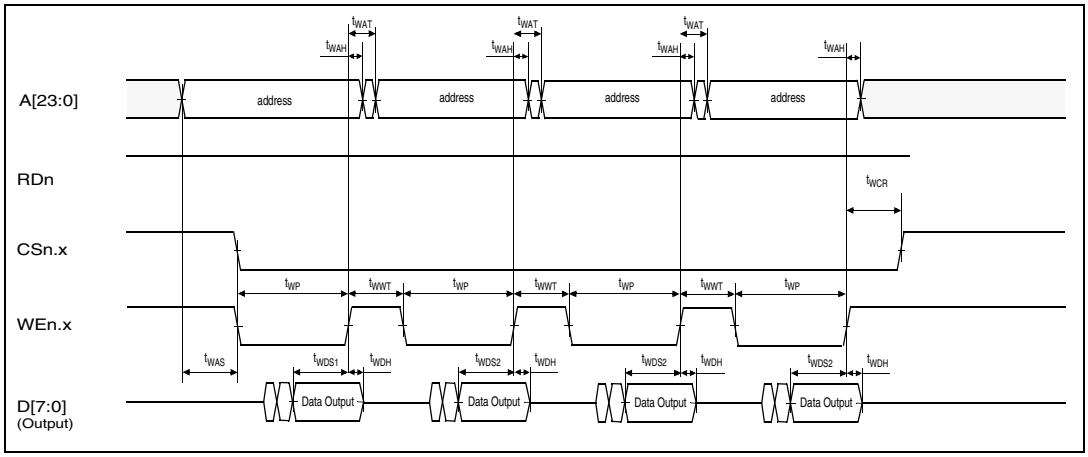


Figure 32. Write cycle timing: 32-bit write on 8-bit memory



See *Table 33* for write timing data.

4.3.8 I²C - inter IC control interface

Subject to general operating conditions for V_{33}, f_{PCLK1}, and T_A unless otherwise specified.

The STR7 I²C interface meets the requirements of the Standard I²C communications protocol described in the following table with the restriction mentioned below:

Note: ***Restriction:*** *The I/O pins which SDA and SCL are mapped to are not "True" Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{33} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{33}. Consequently, when using this I²C in a multi-master network, it is not possible to power off the STR7X while some another I²C master node remains powered on: otherwise, the STR7X will be powered by the protection diode.*

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 34. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C[5]		Unit
		Min [1]	Max [1]	Min [1]	Max [1]	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0 [3]		0 [2]	900 [3]	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

Notes:

1. Data based on standard I^2C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time $t_{h(SDA)}$ is not applicable.
4. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
5. f_{PCLK1}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
6. The following table gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Figure 33. Typical application with I²C bus and timing diagram

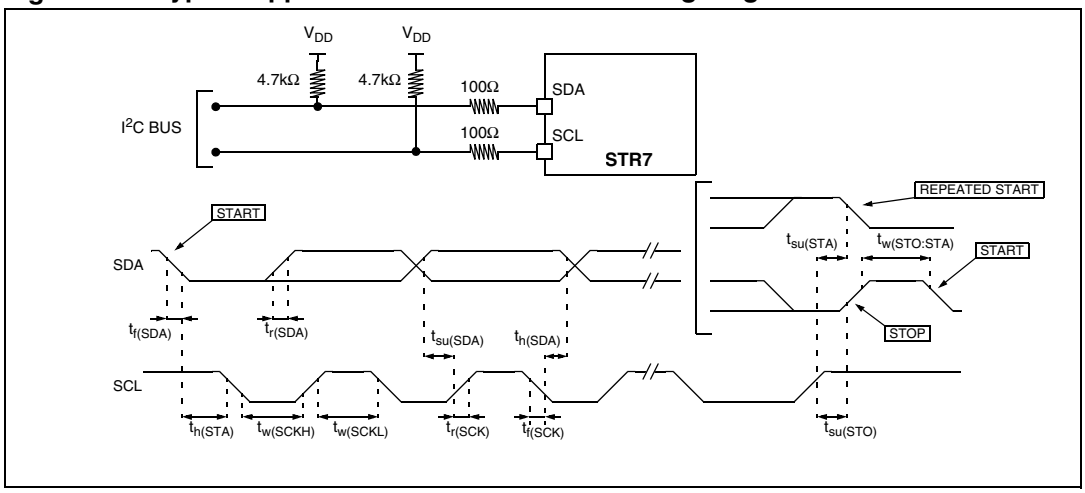


Table 35. SCL Frequency Table (f_{PCLK1}=8 MHz.,V_{33} = 3.3 V)

f_{SCL} (kHz)	I2CCCR Value
	R_P=4.7kΩ
400	83
300	85h
200	8Ah
100	24h
50	4Ch
20	C4h

Legend:

R_P = External pull-up resistance

f_{SCL} = I²C speed

NA = Not achievable

Note: For speeds around 200 kHz, achieved speed can have ± 5% tolerance

For other speed ranges, achieved speed can have ± 2% tolerance

The above variations depend on the accuracy of the external components used.

4.3.9 BSPI - buffered serial peripheral interface

Subject to general operating conditions for V_{DD}, T_A and f_{PCLK1} ,unless otherwise specified.

Refer to *I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics ($\overline{SS}$, SCK, MOSI, MISO).

Table 36. BSPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master	$f_{PCLK1}/254$	$f_{PCLK1}/6$ 5.5	MHz
		Slave	0	$f_{PCLK1}/8$ 3.3	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	capacitive charge C=50 pF		14	ns
$t_{su(\overline{SS})}$ (1)	$\overline{SS}$ setup time	Slave	0		
$t_{h(\overline{SS})}$ (1)	$\overline{SS}$ hold time	Slave	0		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master f_{PCLK1}=33 MHz, presc = 6	73		
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master Slave	7 0		
$t_{h(MI)}$ 1)(2) $t_{h(SI)}$ 1)(2)	Data input hold time	Master Slave	$1xt_{PCLK1}$ $2xt_{PCLK1}$		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master f_{PCLK1}=33 MHz Slave f_{PCLK1}=33 MHz	30 60		
$t_{a(SO)}$ 1)(3)	Data output access time	Slave	0	$1.5xt_{PCLK1}+42$	
		Slave f_{PCLK1}=33 MHz	0	87	
$t_{dis(SO)}$ (1)(4)	Data output disable time	Slave	0	42	
$t_{v(SO)}$ (1)(2)	Data output valid time	Slave (after enable edge)		$3xt_{PCLK1}+45$	
		f_{PCLK1}=33 MHz		135	
$t_{h(SO)}$ (1)	Data output hold time	Slave (after enable edge)	0		
$t_{v(MO)}$ (1)(2)	Data output valid time	Master (after enable edge)		$2xt_{PCLK1}+12$	
		f_{PCLK1}=33 MHz		72	
$t_{h(MO)}$ (1)	Data output hold time	Master (after enable edge)	0		

1. Data based on design simulation and/or characterisation results, not tested in production.
2. Depends on f_{PCLK1}. For example, if f_{PCLK1}=8 MHz, then t_{PCLK1} = $1/f_{PCLK1}$ =125 ns and $t_{v(MO)}$ = 255 ns.
3. Min. time is the minimum time to drive the output and the max. time is the maximum time to validate the data.
4. Min time is the minimun time to invalidate the output and the max time is the maximum time to put the data in Hi-Z.

Figure 34. SPI slave timing diagram with CPHA=0[1)]

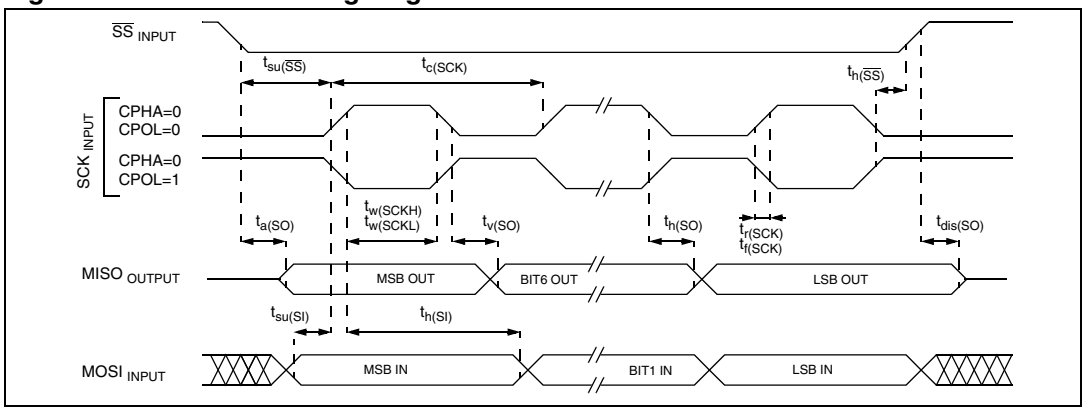


Figure 35. SPI slave timing diagram with CPHA=1[1)]

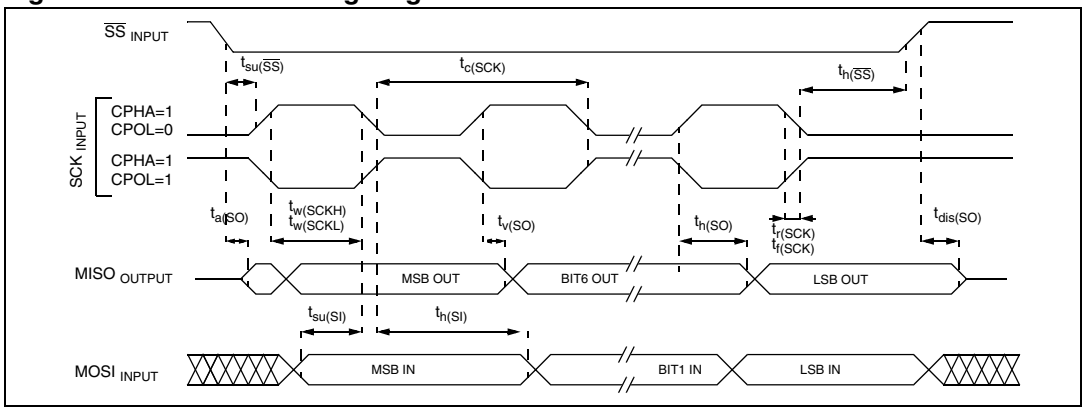
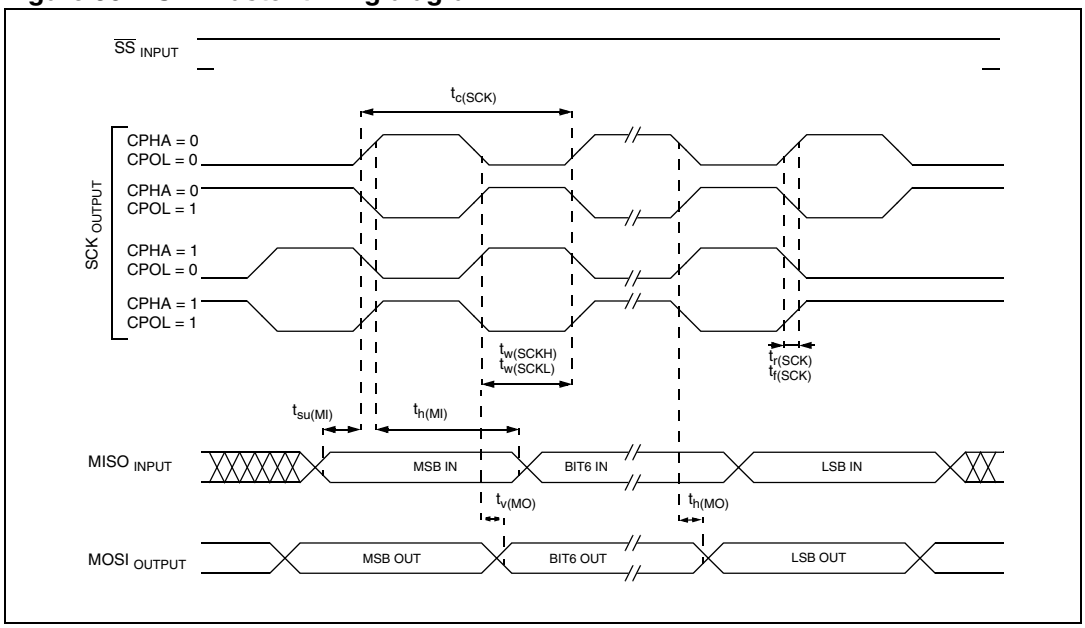


Figure 36. SPI master timing diagram[1)]



1. Measurement points are done at CMOS levels: $0.3xV_{33}$ and $0.7xV_{33}$

4.3.10 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 37. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 38. USB DC characteristics

Symbol	Parameter	Conditions	Min.(1)(2)	Max.(1)(2)	Unit
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 37. USB: data signal rise and fall time

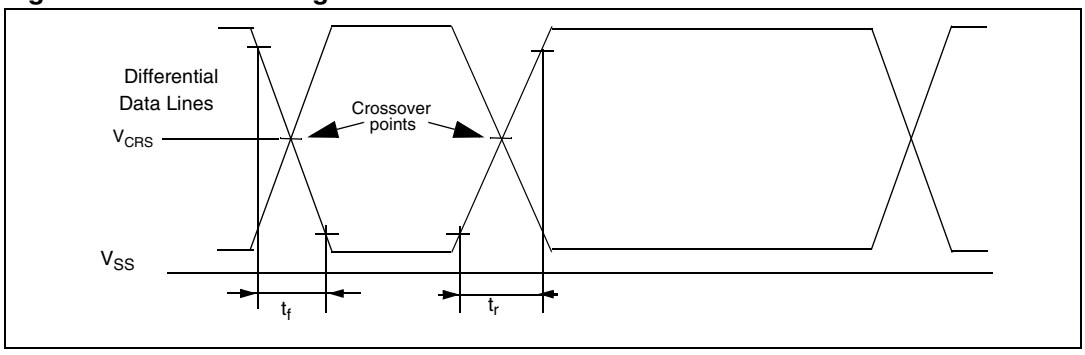


Table 39. USB: Full speed driver electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

4.3.11 ADC characteristics

Subject to general operating conditions for AV_{DD}, f_{PCLK2}, and T_A unless otherwise specified.

Table 40. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{MOD}	Modulator Oversampling frequency				2.1	MHz
V_{AIN}	Conversion voltage range [2][3]		0		2.5	V
I_{lkg}	Negative input leakage current on analog pins	$V_{IN}<V_{SS}$, $\lvert I_{IN} \rvert <$ 400µA on adjacent analog pin		5	6	µA
PBR	Passband Ripple				0.1	dB
SINAD	S/N and Distortion		56	63		dB
THD	Total Harmonic Distortion		60	74		dB
Z_{IN}	Input Impedance	f_{MOD} = 2 MHz	1			MΩ
C_{ADC}	Internal sample and hold capacitor				3.2	pF
t_{CONV}	Total Conversion time (including sampling time)		2048/ f_{MOD} (max)			
I_{ADC}	Normal mode	T_A = 27 °C		2.5	3.0	mA
	Standby mode	T_A = 27 °C			1	µA

Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and AV_{DD}-AV_{SS}=3.3V. They are given only as design guidelines and are not tested.
2. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
3. Calibration is needed once after each power-up.

Table 41. ADC accuracy with f_{PCLK2} = 20 MHz, f_{ADC}=10 MHz, AV_{DD}=3.3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC_DATA(0V)	Converted code when AIN=0V [1]		2370		2565	Decimal code
ADC_DATA(2.5V)	Converted code when AIN=2.5V [1]		1480		1680	
VCM	Center voltage of Sigma-Delta Modulator[1]		1.23	1.25	1.30	V
TUE	Total unadjusted error	In this type of ADC, calibration is necessary to correct gain error and offset errors. Once calibrated, the TUE is limited to the ILE.				
$\|E_D\|$	Differential linearity error[1]			1.96	2.19	LSB
$\|E_L\|$	Integral linearity error [1]			2.36	3.95	

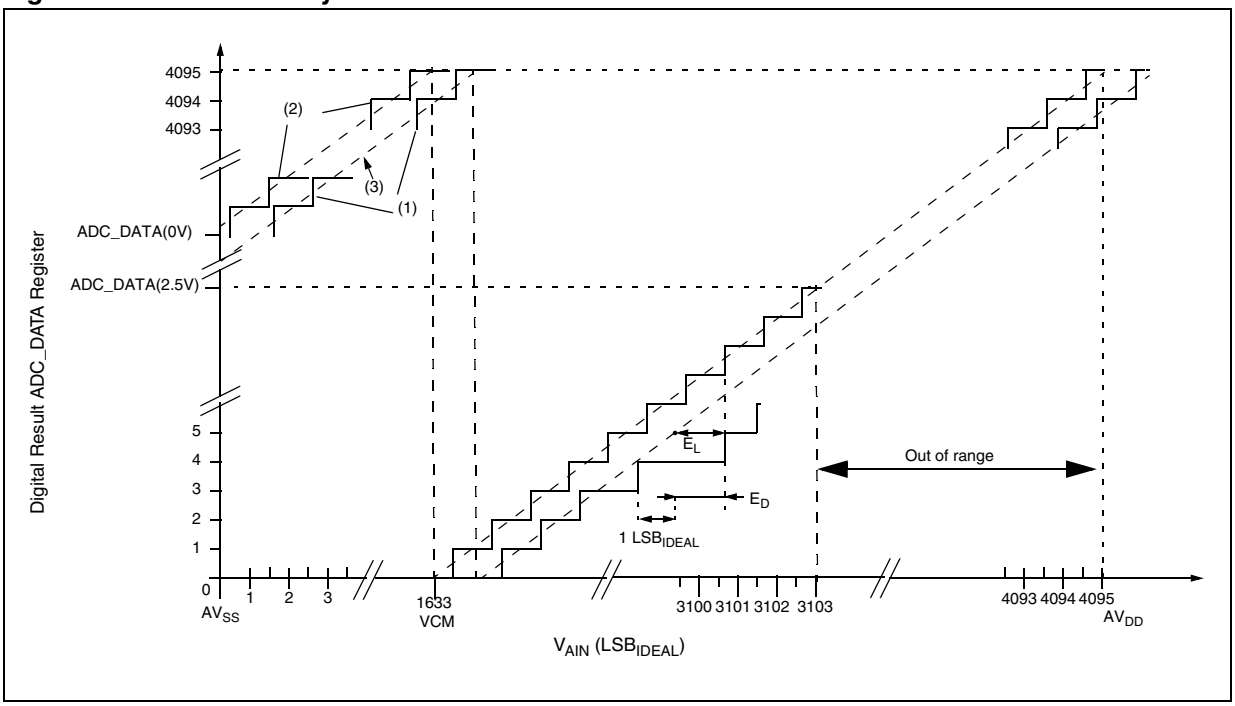
Data are based on characterisation and are not tested in production.

ADC Accuracy vs. Negative Injection Current

Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.

Figure 38. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line

Legend for *Figure 38*

E_D=Differential Linearity Error: maximum deviation between actual steps and the ideal one.
E_L=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Equation 1

$$1LSB_{IDEAL} = \frac{AVDD - AVSS}{4095}$$

Analog power supply and reference pins

The AV_{DD} and AV_{SS} pins are the analog power supply of the A/D converter cell. They act as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see*: General PCB design guidelines*).

General PCB design guidelines

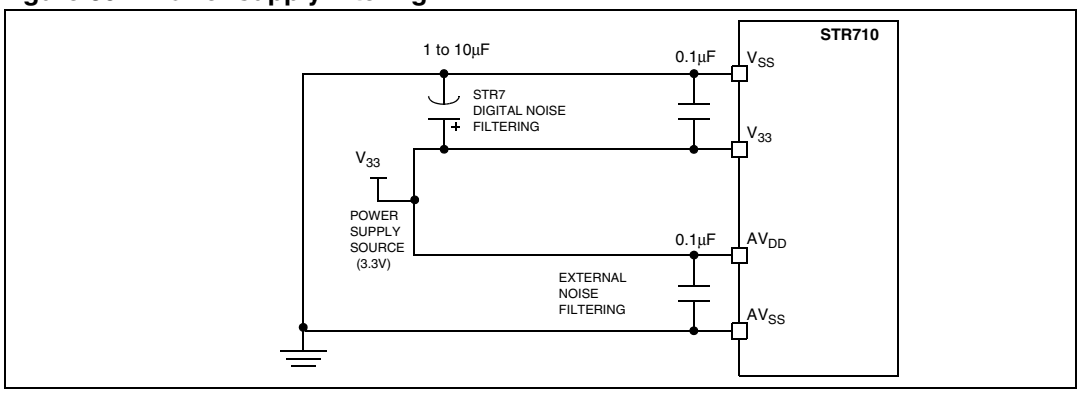
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 39*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as AV_{DD} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

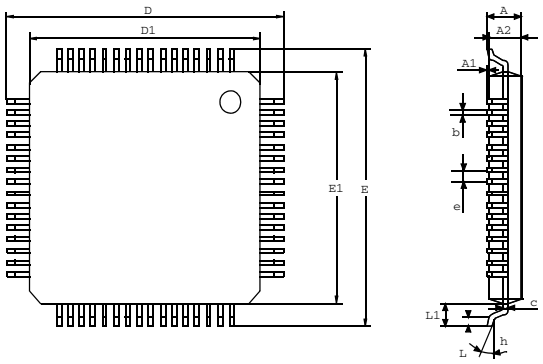
Figure 39. Power supply filtering



5 Package characteristics

5.1 Package mechanical data

Figure 40. 64-Pin low profile quad flat package (10x10)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

Recommended footprint (dimensions in mm)

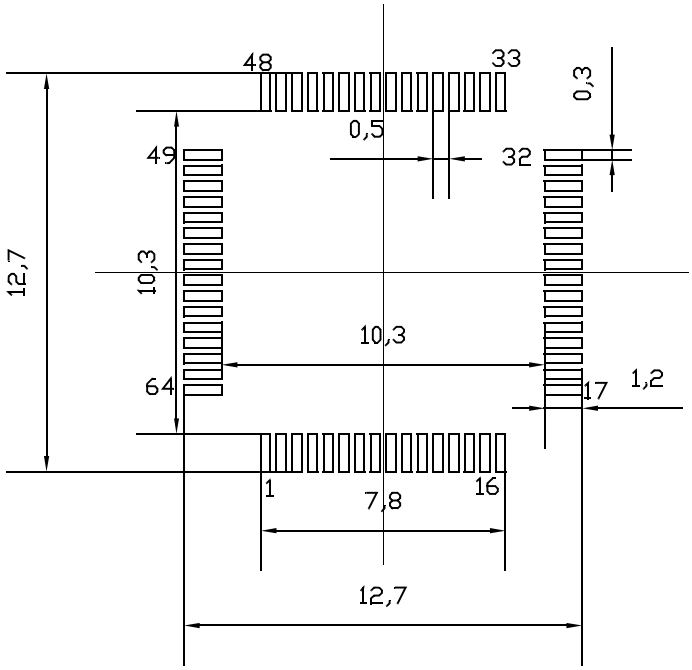
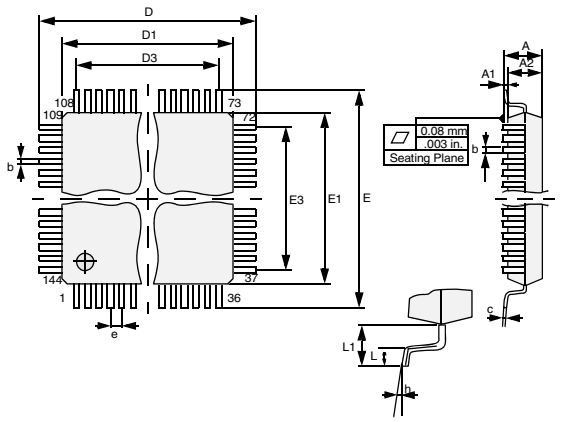


Figure 41. 144-Pin low profile quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

1.Values in inches are converted from mm and rounded to 3 decimal digits.

Jedec Ref. MS-026-BFB

Recommended footprint (dimensions in mm)

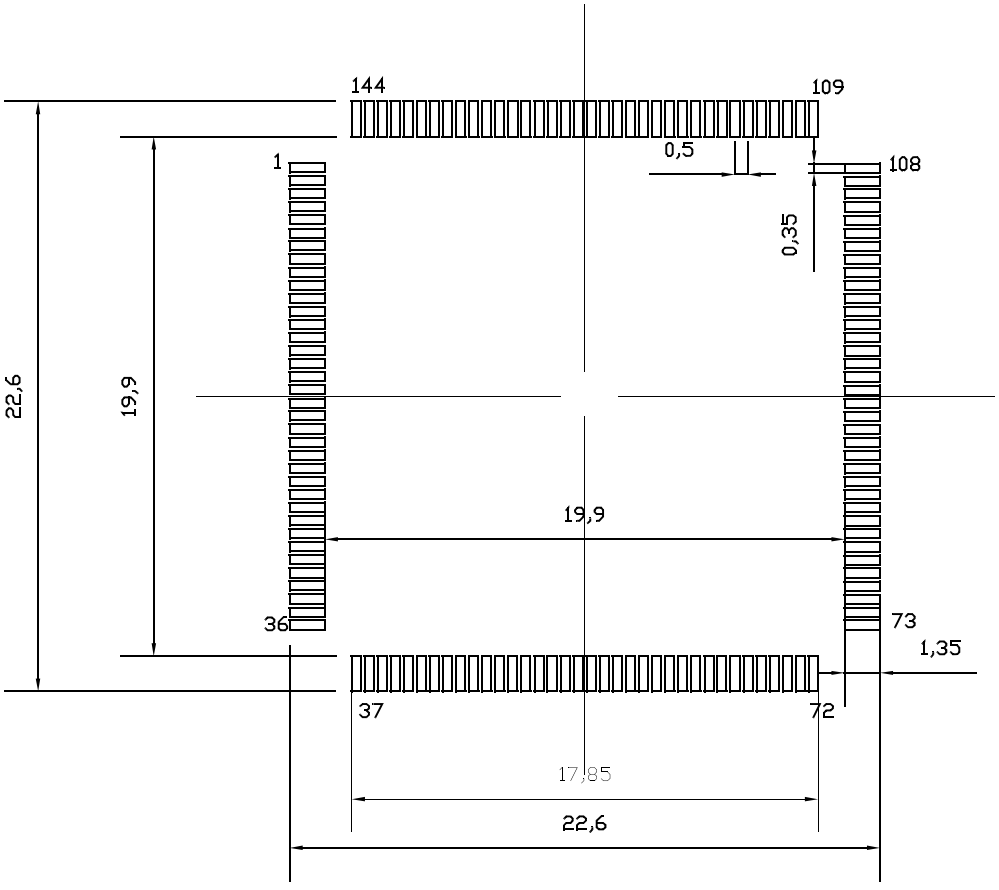
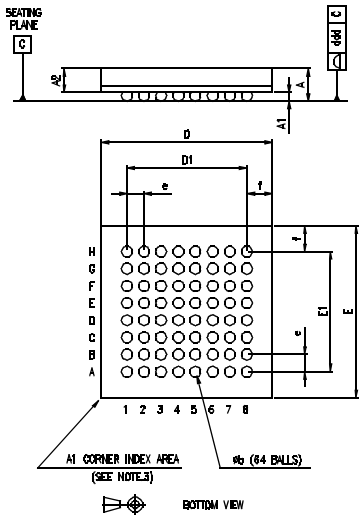
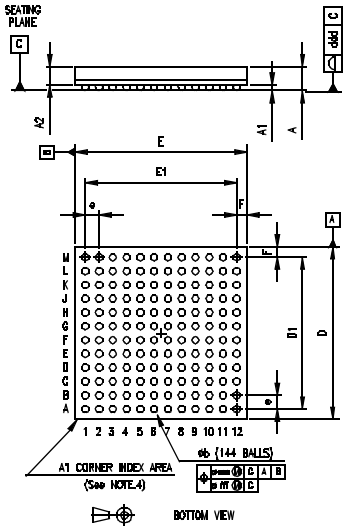


Figure 42. 64-Low profile fine pitch ball grid array package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	7.750	8.000	8.150	0.305	0.315	0.321
D1		5.600			0.220	
E	7.750	8.000	8.150	0.305	0.315	0.321
E1		5.600			0.220	
e	0.720	0.800	0.880	0.028	0.031	0.035
f	1.050	1.200	1.350	0.041	0.047	0.053
ddd			0.120			0.005
	Number of Pins					
N	64					

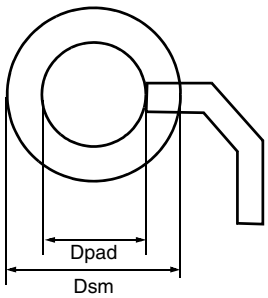
Figure 43. 144-low profile fine pitch ball grid array package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.085			0.0427	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031
	Number of Pins					
N	144					

[1]Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W

6 Product history

There are three versions of the STR710F series products. All versions are functionally identical and differ only with the points listed below.

Version "A" was the first version produced and delivered. Version "Z" was the second in production replacing version "A". Version "Z" has lower power consumption in STOP mode.

Version "X" is the latest introduced.

Marking

The difference between versions is visible on the marking of the product as shown in the four examples in *Figure 45* through *Figure 48*.

Figure 45. LQFP144 STR710 version “A”

Figure 46. LQFP64 STR712 version “Z”

Figure 47. BGA144 STR710 version “Z”

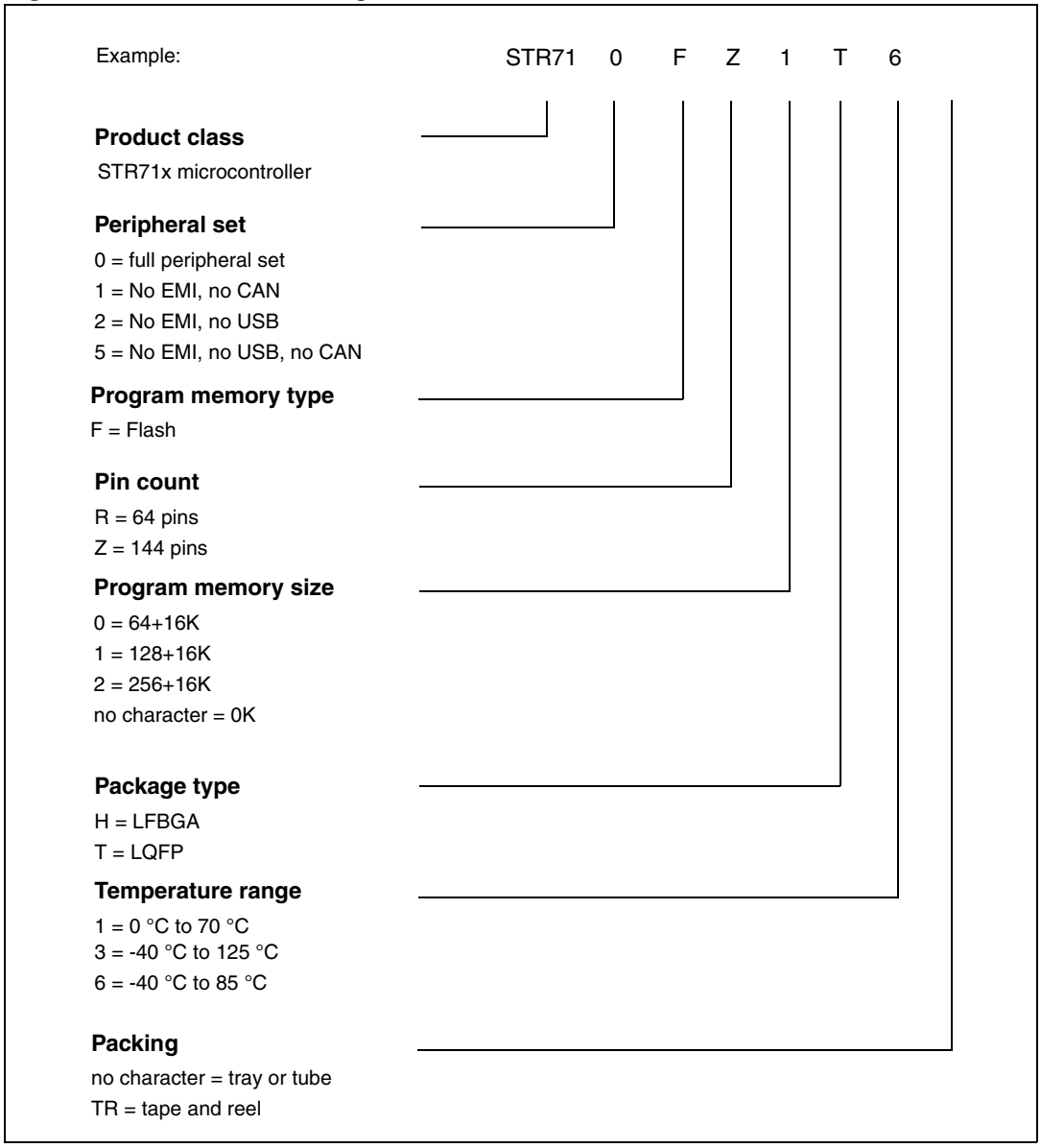
Figure 48. BGA64 STR711 version “X”

Table 43. A, Z and X version differences

Feature	A version	Z version	X version
ARM7TDMI core device Identification (ID) code register (see ARM7TDMI Technical Reference Manual)	Version bits [31:28] = 0001	Version bits [31:28] = 0010	Version bits [31:28] = 0010
Low power mode consumption in STOP mode at 25 °C	Not guaranteed Typical 49 µA	50 µA maximum at 25°C. Less than 30 µA at 25 °C for 99.730020% of parts	Same as Z.
SC.DATA pin	Not TRUE open drain When addressing 5V cards, the SCDATA Line must be connected to an open drain buffer.		Pin P0.10/U1.RX/U1.TX/SC.DATA has been modified to offer TRUE OPEN DRAIN functionality when in Smartcard mode. When addressing 5V cards, the SCDATA line can now be connected directly to the card I/O. This modification is backward compatible with previous designs, and no board modification is required.

7 Ordering information

Figure 49. STR71xF ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST Sales Office nearest to you.

8 Known limitations

Description

If an IRQ or FIQ interrupt is pending and the Interrupt vector register (EIC_IVR) is not yet read, the HALT bit in the RCCU_SMR register can not be written. Therefore a software reset can not be generated.

Workaround

To generate a software reset when an IRQ or FIQ line is pending, either:

- reset the EIC peripheral by setting bit 14 in the APB2_SWRES register, or
- read the EIC_IVR register prior to generating a software reset.

9 Revision history

Table 44. Document revision history

Date	Revision	Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “Electrical parameters” on page 34
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “EMI - external memory interface” on page 56
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31* Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25* Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in *Section 5* Updated ordering information in *Section 7*. Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45*
13-Oct-2005	7	Updated feature description on page 1 Update overview *Section 1.1* Added OD/PP to P0.12 in *Table 5* Changed name of WFI mode to WAIT mode Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption *Table 13* Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4* Update EMI Timing *Table 24* and *Figure 29*

Table 44. Document revision history (continued)

Date	Revision	Changes
22-May-2006	8	Added Flashless device. Changed reset state of pins P1.10 and P1.13 from pu to pd, P0.15 from pu to floating and removed x in interrupt column for P1.15 and P1.12 in *Table 4* and *Table 5* Added notes under *Table 4* on EMI pin reset state. Corrected inch value for d3 in *Figure 40* Added footprint diagrams in *Figure 40* and *Figure 43* Updated *Section 4: Electrical parameters*
01-Aug-2006	9	Flash data retention changed to 20 years at 85° C. Changed note 8 on page 19 Changed note 1 on page 45
06-Nov-2006	10	Added STR715FR0T1 in *Table 42: Order codes* P0.12 corrected in *Table 5 on page 25*
20-Mar-2007	11	Added characteristics of *BSPI - buffered serial peripheral interface on page 63* Updated *Table 21: Low-power mode wakeup timing on page 46*
13-Feb-2008	12	Updated ordering information Updated USB characteristics Updated external clock characteristics
03-Apr-2013	13	Updated title (to be in line with the “device summary” table) Updated ST Logo and Disclaimer Added *Section 8: Known limitations*

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