1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current[1] (8/20 µs, 1.2/50 µs)	T_j initial = T_{amb}	500	A
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Operating junction temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Thermal resistances

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction to leads	15	°C/W
$R_{th(j-a)}$	Junction to ambient on printed circuit on recommended pad layout	90	°C/W

Figure 1. Electrical characteristics - parameters

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_F	=	Forward current
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward voltage drop
R_d	=	Dynamic impedance

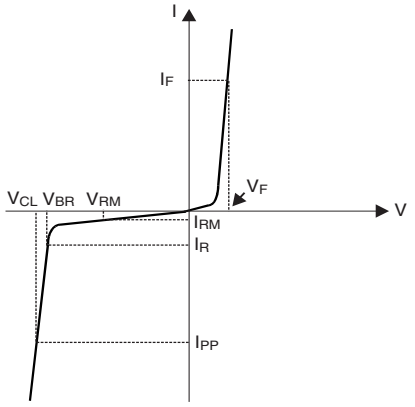


Table 3. Electrical characteristics - parameter values (T_{amb} = 25 °C)

Order code	I_{RM} @V_{RM}			V_{BR} @I_R(1)				V_{CL} @I_{PP} 8/20 µs, 1.2/50 µs		R_D(2) 8/20 µs	αT (3)
	25 °C	85 °C		Min.	Typ.	Max.		Max.		Typ.	max
	µA		V	V			mA	V	A	Ω	10^{-4}/ °C
STIEC45-24AS	0.2	1	24	26.7	28.2	29.5	1	42	500	0.025	9.6
STIEC45-26AS	0.2	1	26	28.9	30.3	31.9	1	45	500	0.026	9.7
STIEC45-27AS	0.2	1	27	30	31.6	33.2	1	47	500	0.028	9.7
STIEC45-28AS	0.2	1	28	31.1	32.6	34.3	1	49	500	0.029	9.8
STIEC45-30AS	0.2	1	30	33.3	35	36.8	1	55	500	0.036	9.9
STIEC45-33AS	0.2	1	33	36.7	38.6	40.6	1	59	500	0.036	10

1. Pulse test: t_p < 50 ms
2. To calculate maximum clamping voltage at other surge levels: $V_{CLmax} = R_D \times I_{PP} + V_{BRmax}$
3. To calculate V_{BR} versus junction temperature: V_{BR} @ $T_j = V_{BR}$ @ 25°C x (1 + αT x (T_j – 25))

Note: Surge capability given for both directions for unidirectional and bidirectional types.

Figure 2. Pulse form

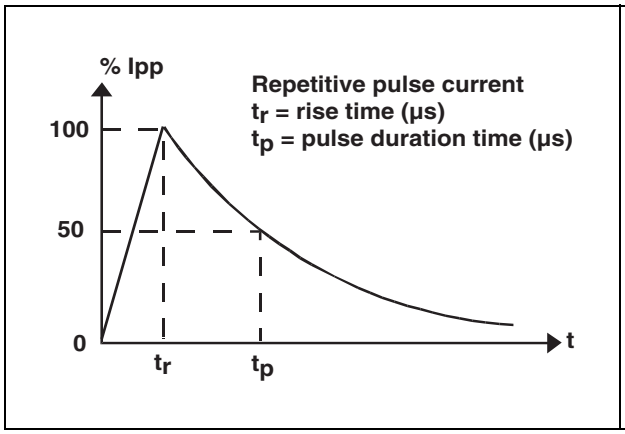


Figure 3. Peak pulse current versus initial junction temperature

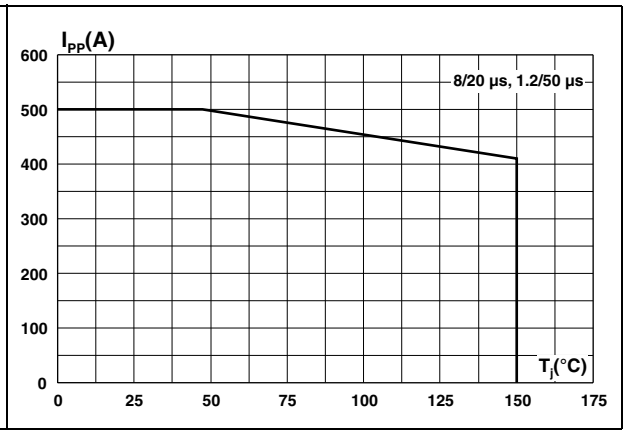


Figure 4. Clamping voltage at 500 A (1.2/50 µs - 8/20 µs)

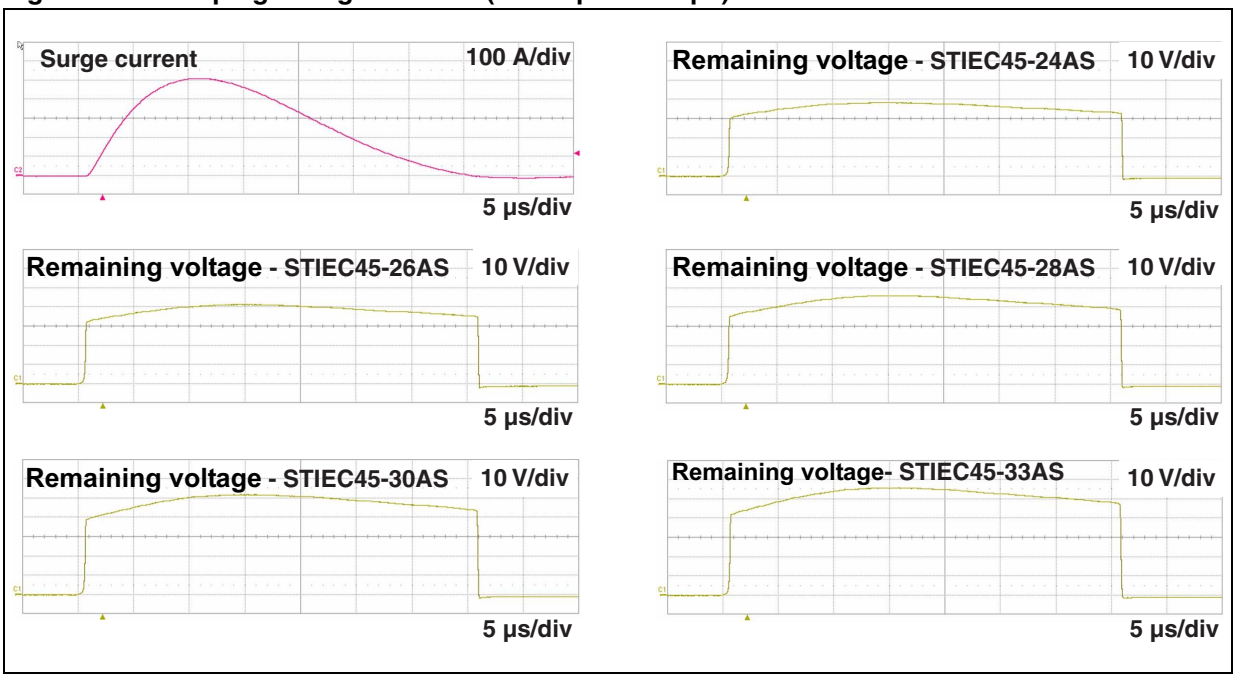


Figure 5. Junction capacitance versus reverse applied voltage (typical values)

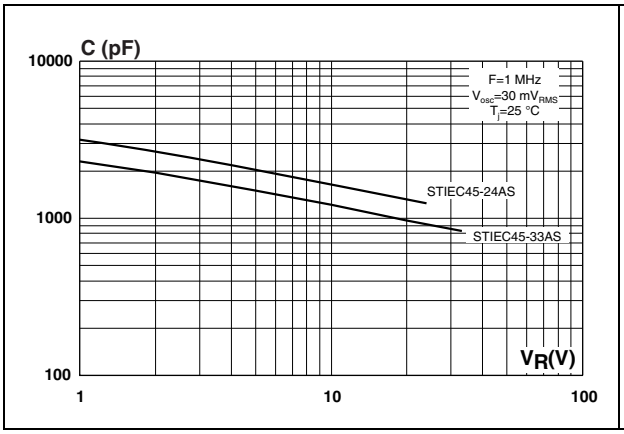


Figure 6. Peak forward voltage drop versus peak forward current (typical values)

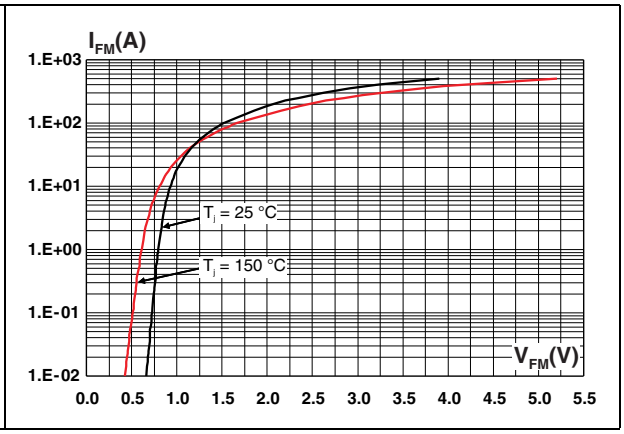


Figure 7. Relative variation of thermal impedance, junction to ambient, versus pulse duration

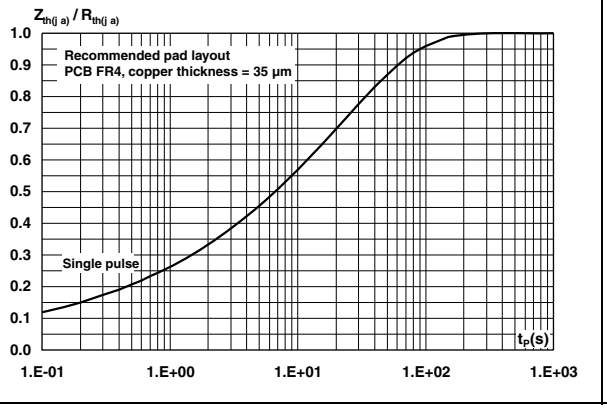


Figure 8. Thermal resistance junction to ambient versus copper surface under each lead

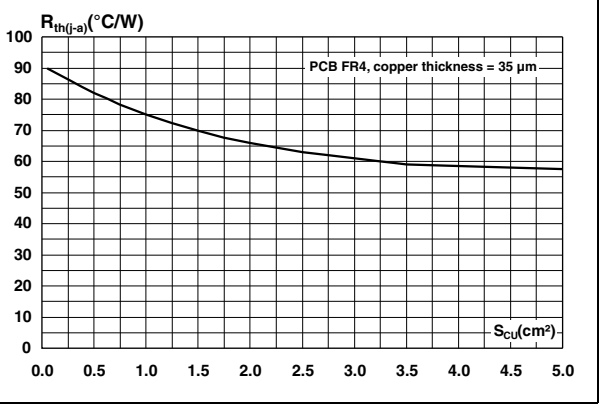
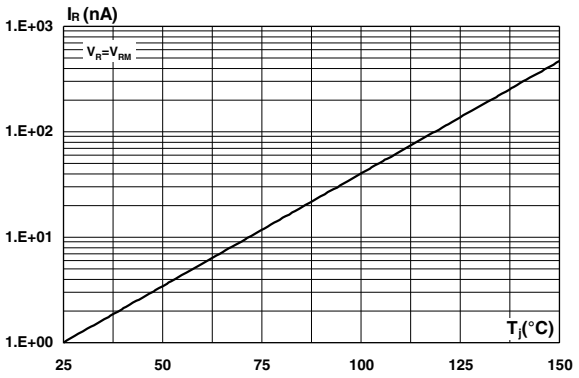
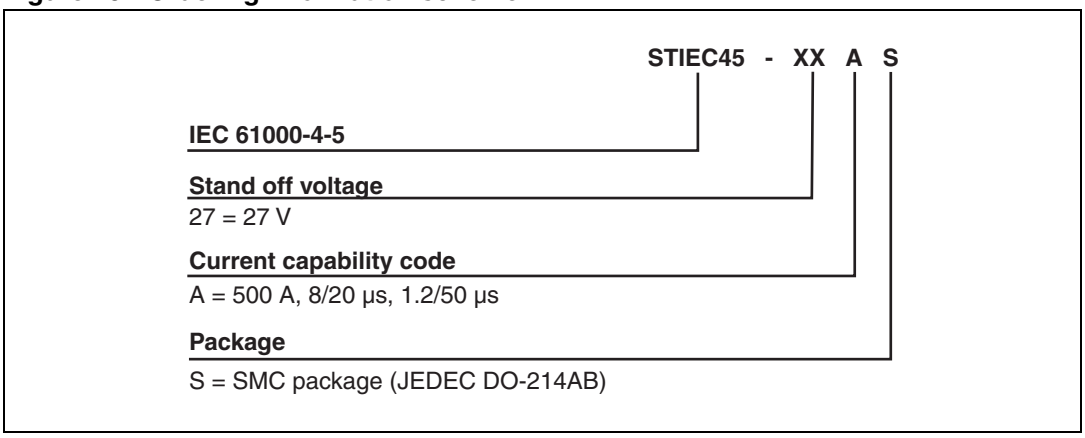


Figure 9. Leakage current versus junction temperature (typical values)



2 Ordering information scheme

Figure 10. Ordering information scheme

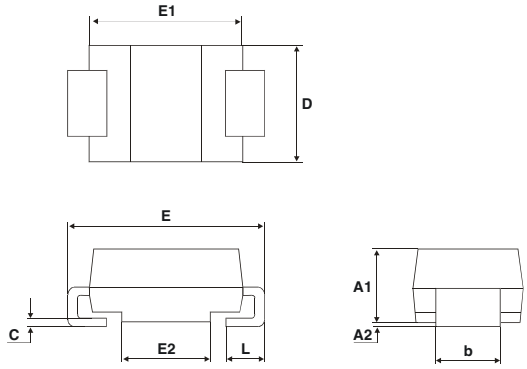


3 Package information

- Case: JEDEC DO-214AB molded plastic over planar junction
- Terminals: solder plated, solderable per MIL-STD-750, Method 2026
- Polarity: for unidirectional types the band indicates cathode
- Flammability: epoxy is rated UL94V-0
- RoHS package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 4. SMC dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A1	1.90	2.45	0.075	0.096
A2	0.05	0.20	0.002	0.008
b	2.90	3.2	0.114	0.126
c	0.15	0.41	0.006	0.016
E	7.75	8.15	0.305	0.321
E1	6.60	7.15	0.260	0.281
E2	4.40	4.70	0.173	0.185
D	5.55	6.25	0.218	0.246
L	0.75	1.60	0.030	0.063

Figure 11. Footprint dimensions in mm (inches)

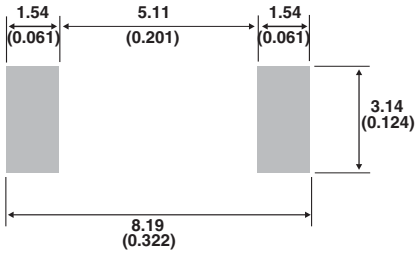
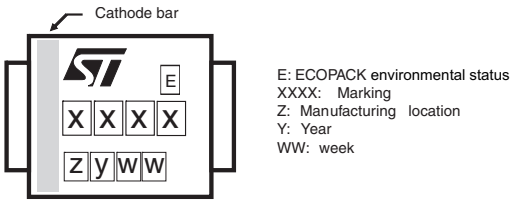


Figure 12. Marking layout



Note: Marking layout can vary according to assembly location.

4 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
STIEC45-24AS	4524A	SMC	0.25 g	2500	Tape and reel
STIEC45-26AS	4526A				
STIEC45-27AS	4527A				
STIEC45-28AS	4528A				
STIEC45-30AS	4530A				
STIEC45-33AS	4533A				

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
07-Dec-2009	1	First issue.

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