

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|------------------|
| V_{DS} | Drain-source voltage | 55 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 80 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 80 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 320 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 300 | W |
| P_1 | Long term load test ($I_D = 100\text{ A}$, $V_{DS} = 1.5\text{ V}$, $t_{pulse} = 10\text{ ms}$) ΔV_{SD} (tested) | 150 | W |
| $P_2^{(3)}$ | Short term load test ($I_D = 75\text{ A}$, $V_{DS} = 15\text{ V}$, $t_{pulse} = 700\text{ }\mu\text{s}$) ΔV_{SD} (not tested) | 1125 | W |
| $E_{AS}^{(4)}$ | Single-pulse avalanche energy | 1.3 | J |
| $dv/dt^{(5)}$ | Peak diode recovery voltage slope | 7 | V/ns |
| T_{stg} | Storage temperature range | -55 to 175 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | |

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Defined by design, not subject to production test.
4. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 30\text{ A}$, $V_{DD} = 30\text{ V}$
5. $I_{SD} \leq 80\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 0.5 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 35 | $^\circ\text{C}/\text{W}$ |

1. When mounted on an FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

$T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 3. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-----------------------------------|--|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 55 | | | V |
| V_{BR0} | | $V_{GS} = 1.5\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 40 | | | V |
| V_{BR1} | | $V_{GS} = 1.5\text{ V}$, $I_D = 10\text{ mA}$ | 40 | | | V |
| V_{BR2} | | $V_{GS} = 1.5\text{ V}$, $I_D = 100\text{ mA}$ | 40 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 55\text{ V}$ | | | 10 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 55\text{ V}$ $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾ | | | 100 | μA |
| $I_{GSS}^{(2)}$ | Gate body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2 | | 4 | V |
| | | $V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$, $T_J = 175\text{ }^{\circ}\text{C}$ ⁽¹⁾ | 1 | | | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$ | | 5.0 | 6.5 | m Ω |

1. Defined by design, not subject to production test.

2. Tested @ $V_{GS} = \pm 22\text{ V}$ at wafer level.

Table 4. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 4400 | | pF |
| C_{oss} | Output capacitance | | - | 1020 | | pF |
| C_{rss} | Reverse transfer capacitance | | - | 350 | | pF |
| Q_g | Total gate charge | $V_{DD} = 27.5\text{ V}$, $I_D = 80\text{ A}$, | - | 142 | 193 | nC |
| Q_{gs} | Gate-source charge | $V_{GS} = 0\text{ to }10\text{ V}$ | - | 29 | | nC |
| Q_{gd} | Gate-drain charge | (see Figure 13. Test circuit for gate charge behavior) | - | 60.5 | | nC |

Table 5. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 27\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 27 | - | ns |
| t_r | Rise time | | - | 155 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform) | - | 125 | - | ns |
| t_f | Fall time | | - | 65 | - | ns |

Table 6. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 80 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 320 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 35\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 100 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 325 | | nC |
| I_{RRM} | Reverse recovery current | | - | 6.5 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

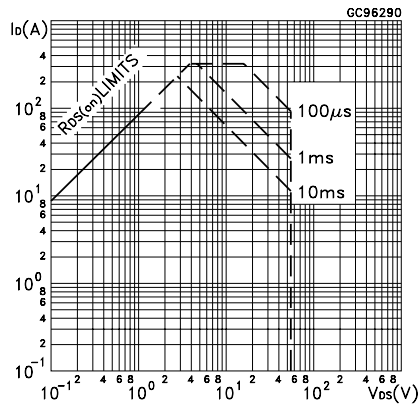


Figure 2. Thermal impedance

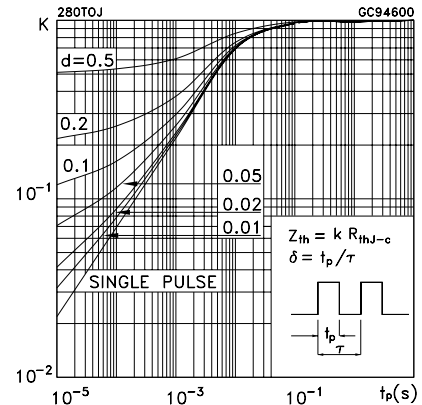


Figure 3. Output characteristics

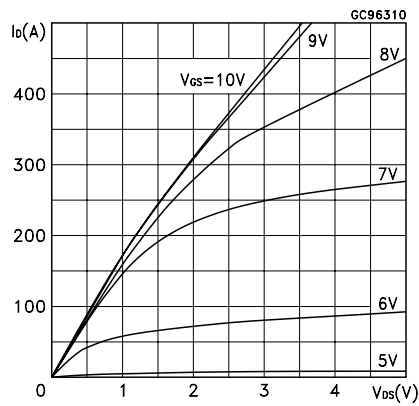


Figure 4. Transfer characteristics

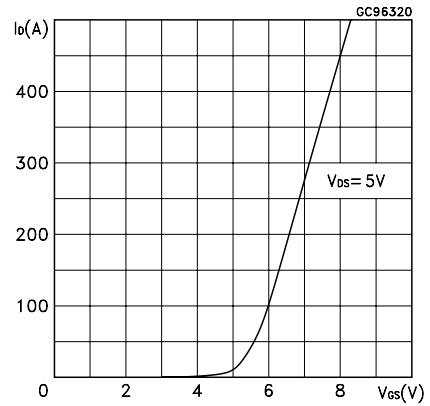


Figure 5. Static drain-source on-resistance

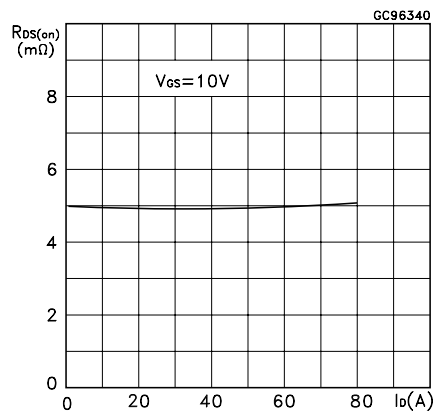


Figure 6. Gate charge vs gate-source voltage

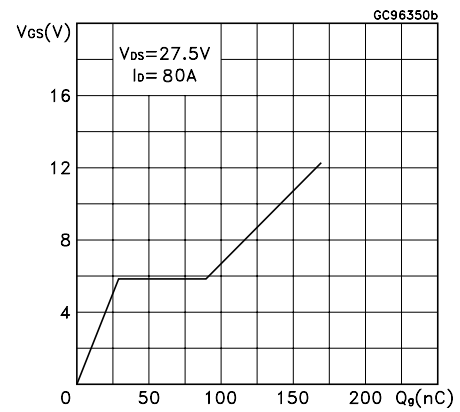


Figure 7. Capacitance variations

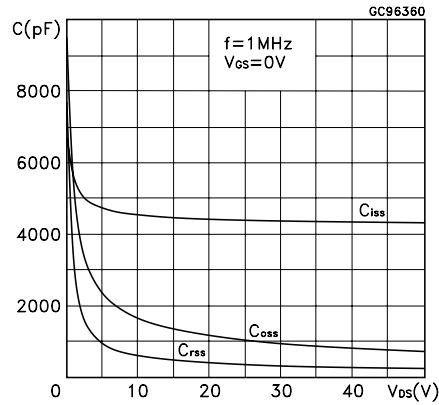


Figure 8. Normalized gate threshold voltage vs temperature

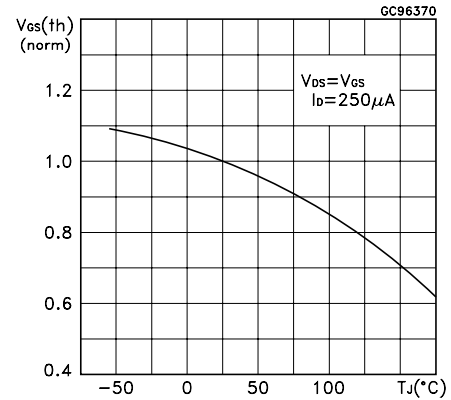


Figure 9. Normalized on-resistance vs temperature

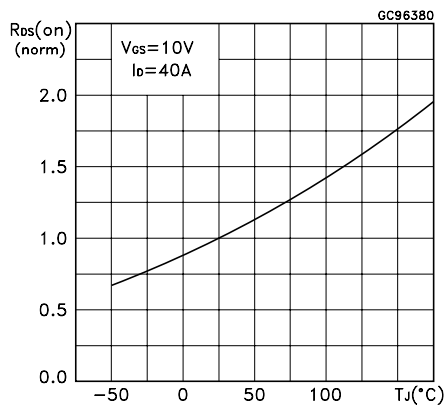


Figure 10. Source-drain diode forward characteristics

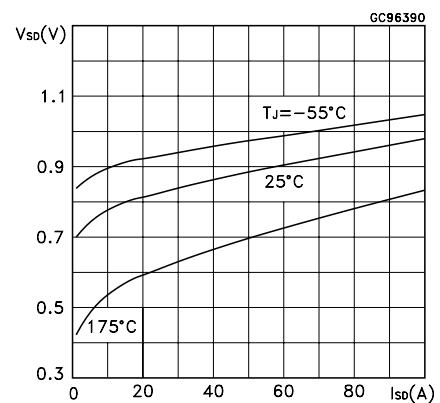
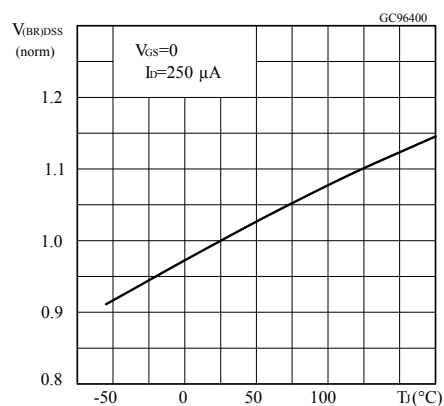
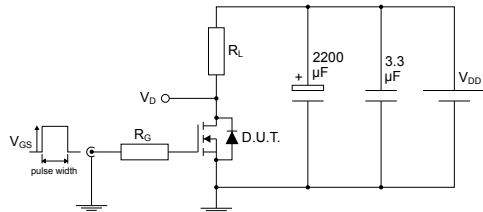


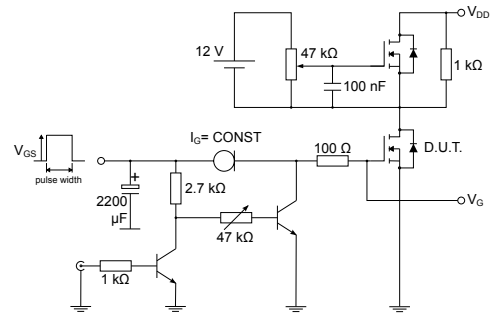
Figure 11. Normalized $V_{(BR)DSS}$ vs temperature



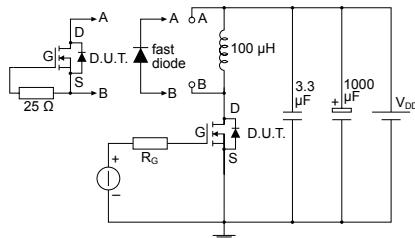
3 Test circuits

Figure 12. Test circuit for resistive load switching times


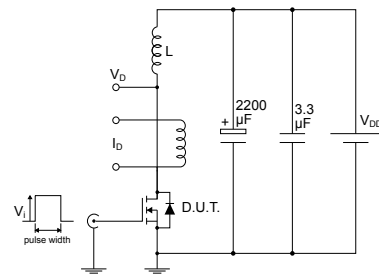
AM01468v1

Figure 13. Test circuit for gate charge behavior


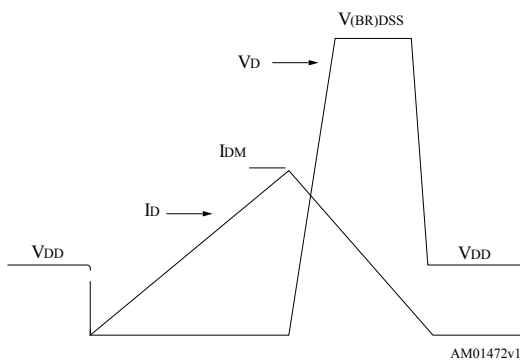
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Figure 14. Test circuit for inductive load switching and diode recovery times


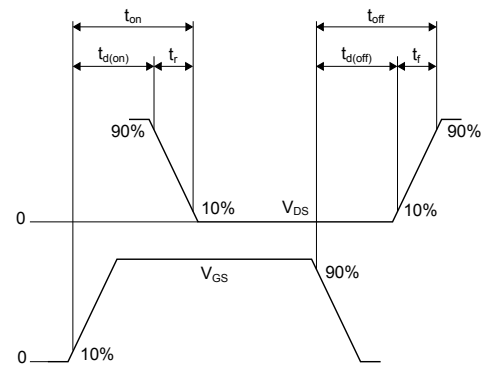
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


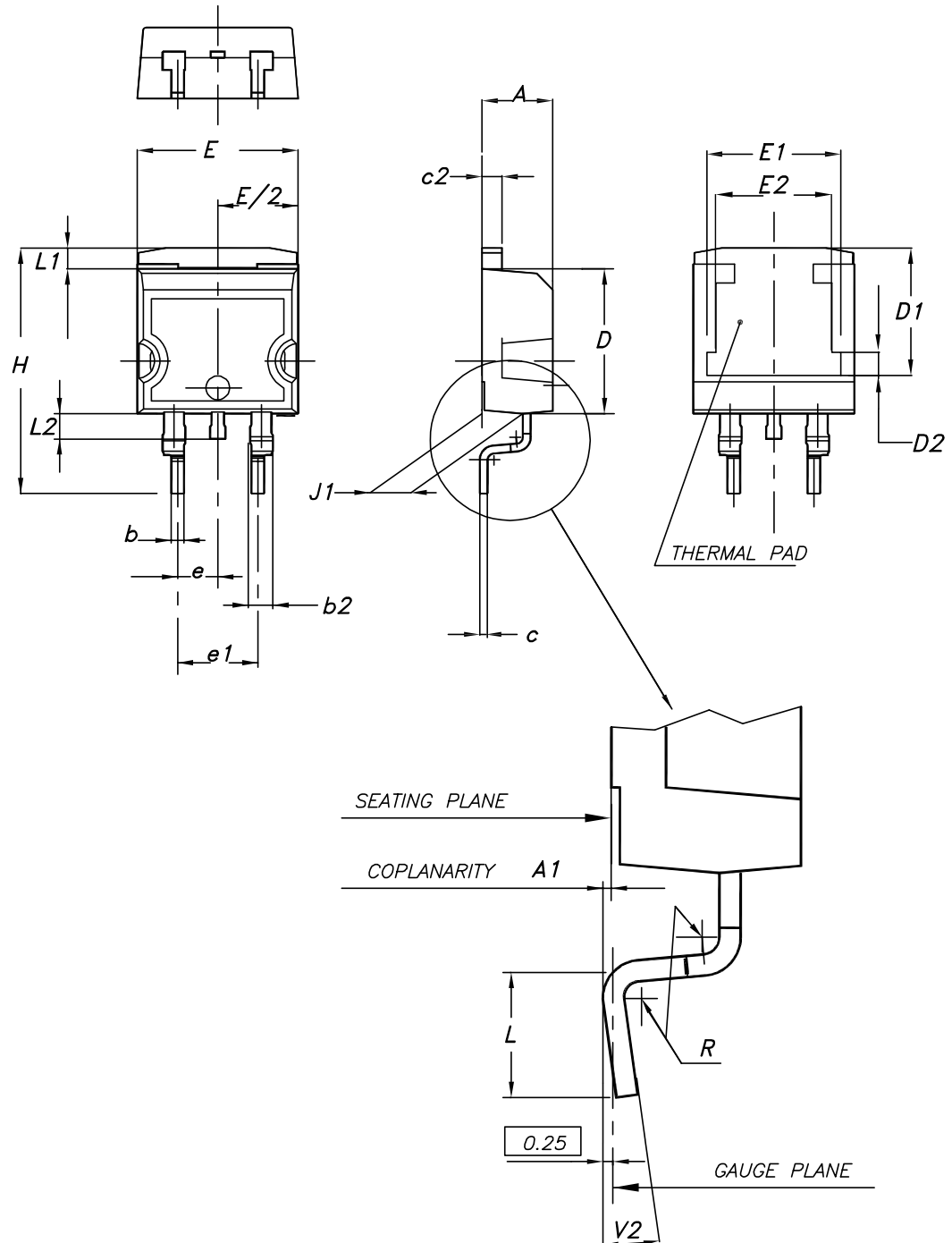
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 18. D²PAK (TO-263) type A package outline

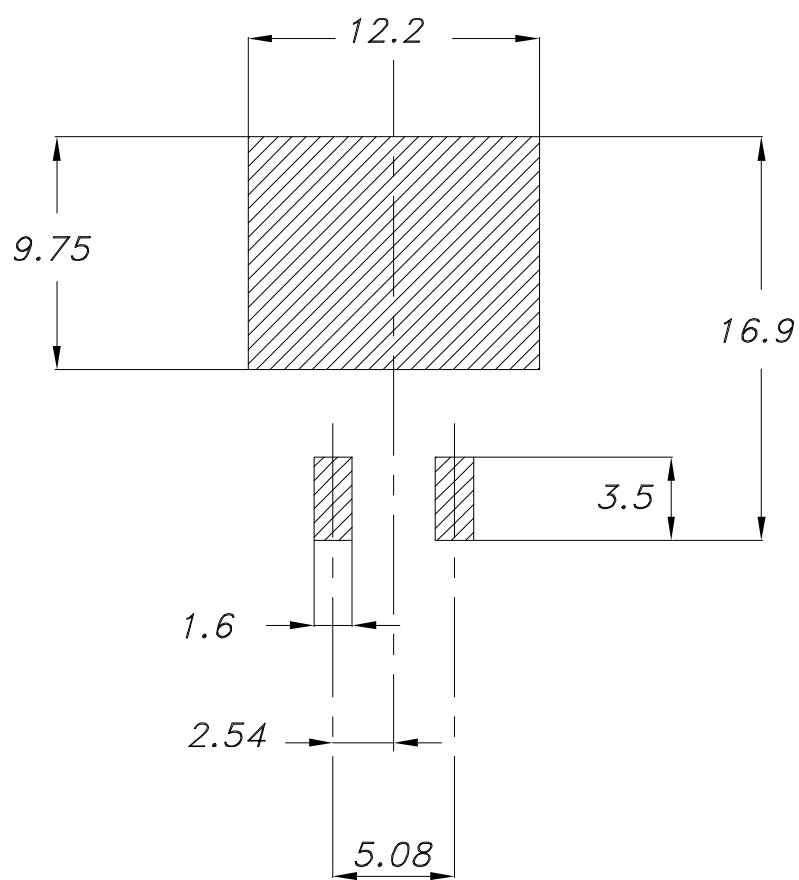


0079457_25

Table 7. D²PAK (TO-263) type A package mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10.00 | | 10.40 |
| E1 | 8.30 | 8.50 | 8.70 |
| E2 | 6.85 | 7.05 | 7.25 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15.00 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.40 | |
| V2 | 0° | | 8° |

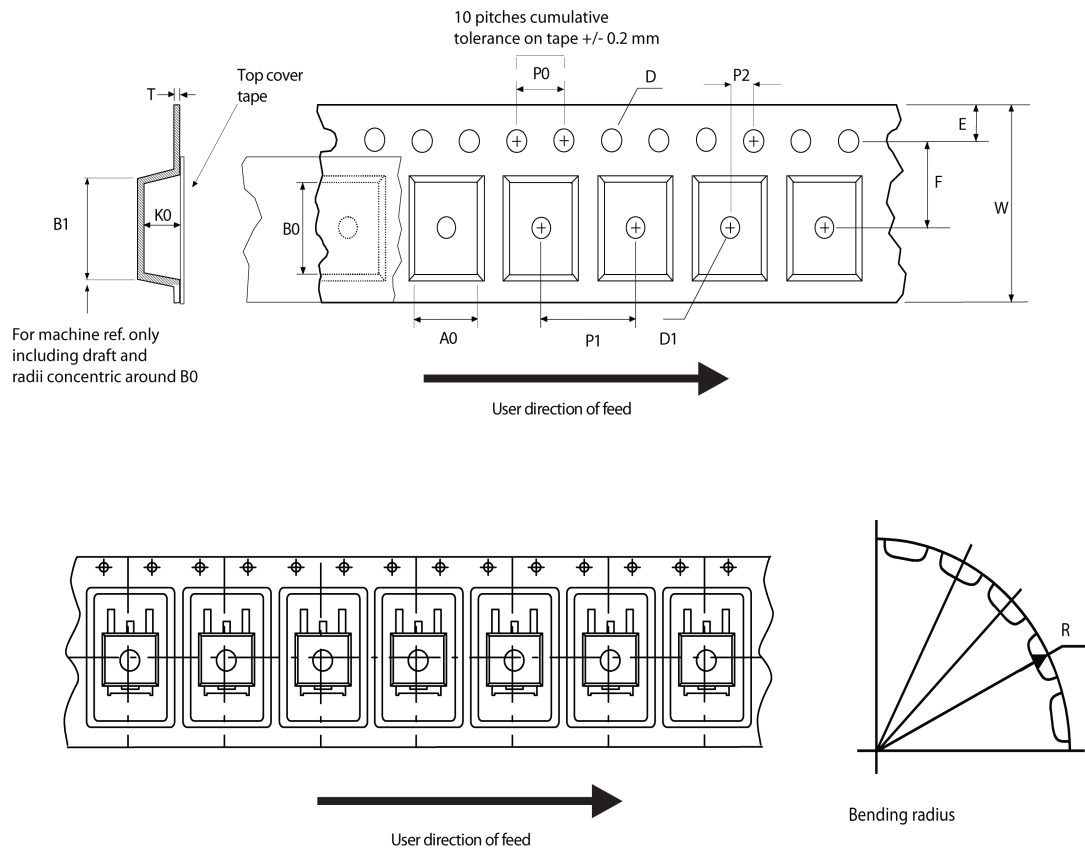
Figure 19. D²PAK (TO-263) recommended footprint (dimensions are in mm)



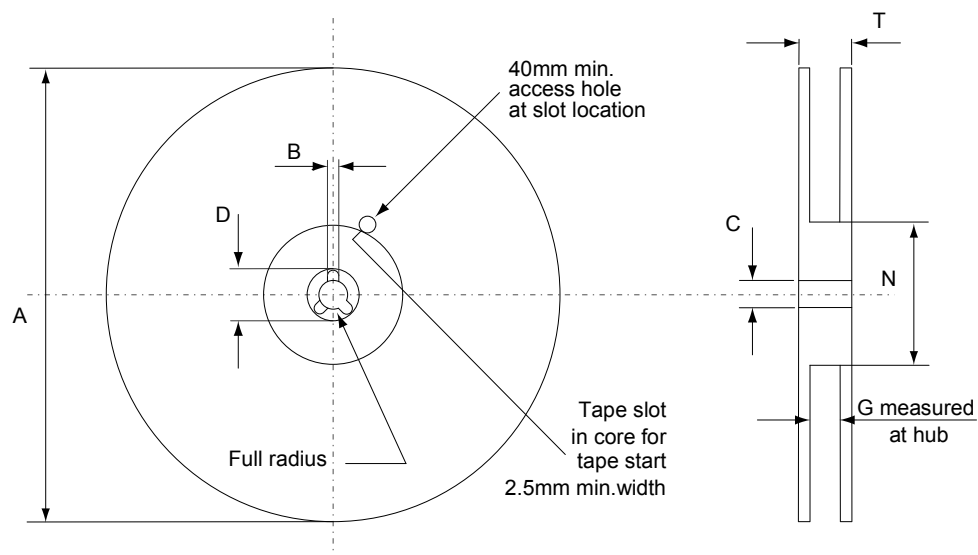
Footprint

4.2 D²PAK packing information

Figure 20. D²PAK tape outline



AM08852v1

Figure 21. D²PAK reel outline


AM06038v1

Table 8. D²PAK tape and reel mechanical data

| Tape | | | Reel | | |
|------|------|------|---------------|------|------|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base quantity | | 1000 |
| P2 | 1.9 | 2.1 | Bulk quantity | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

Revision history

Table 9. Document revision history

| Date | Version | Changes |
|-------------|---------|---|
| 19-Jan-2012 | 1 | First issue. |
| 04-Sep-2018 | 2 | Removed maturity status indication from cover page. The document status is production data. Modified Table 1. Absolute maximum ratings . Updated Section 4 Package information . Minor text changes. |

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