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1 General description

Figure 1. Logic diagram

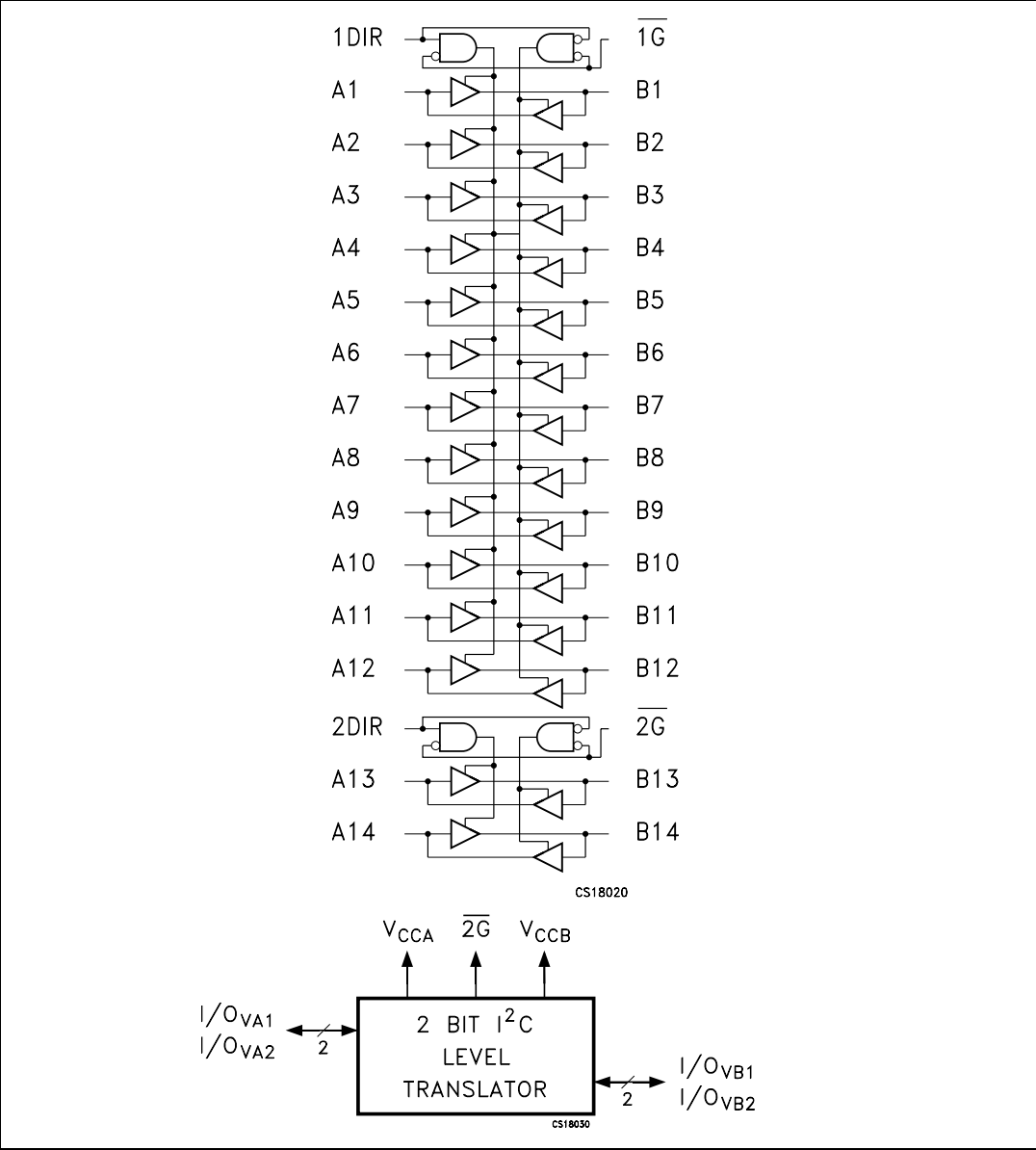
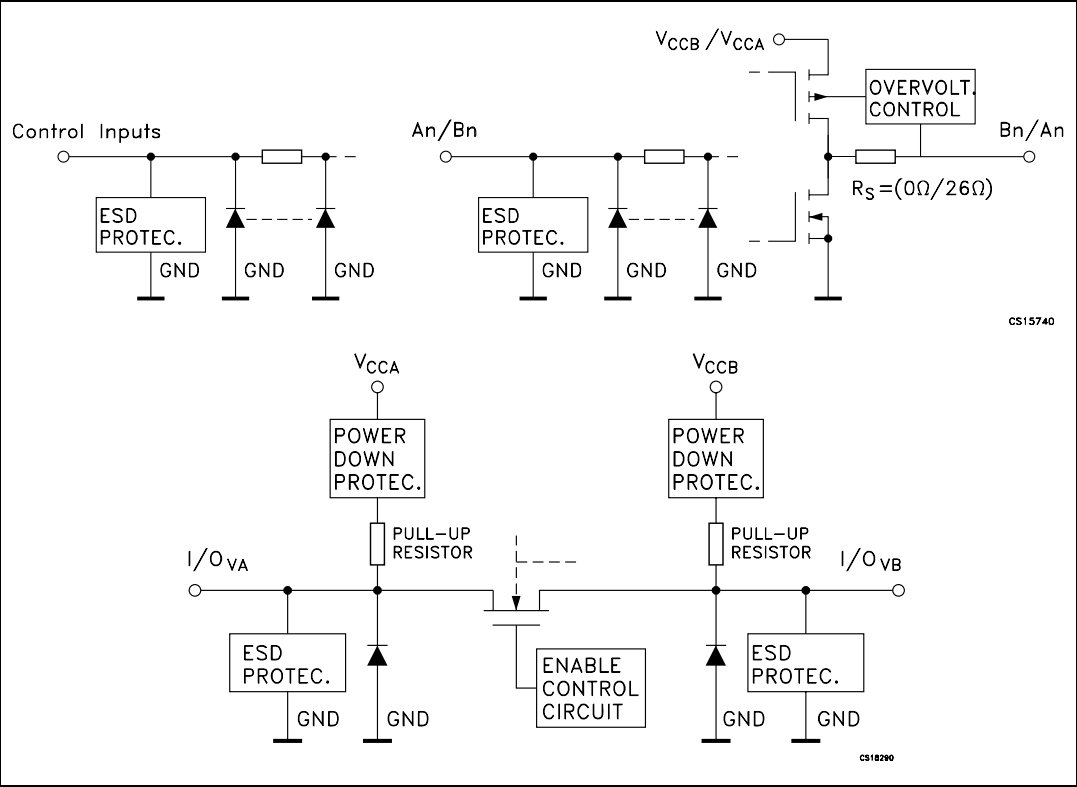


Figure 2. Input and output equivalent circuit



# 2 Pin settings

## 2.1 Pin connection

Figure 3. Pin connection (top through view)

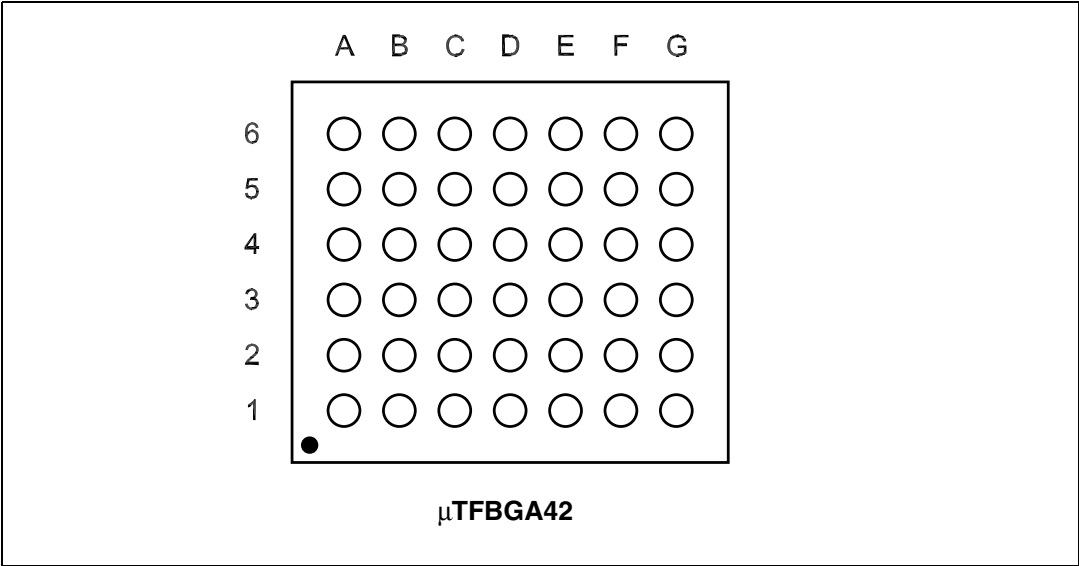


Table 2. Pin description

Pin number	Symbol	Name and function
B3	1DIR	Directional controls
F3	2DIR	Directional controls
A4, A5, A6, B5, B6, C5, C6, D5	A1, A2, A3, A4, A5, A6, A7, A8	Data Inputs/outputs
D6, E5, E6, F5, F6, G6	A9, A10, A11, A12, A13, A14	Data Inputs/outputs
A3, A2, A1, B2, B1, C2, C1, D2	B1, B2, B3, B4, B5, B6, B7, B8	Data Inputs/outputs
D1, E2, E1, F2, F1, G1	B9, B10, B11, B12, B13, B14	Data Inputs/outputs
F4	$\overline{2G}$	Output enable inputs
B4	$\overline{1G}$	Output enable inputs
C3, C4, E3, E4	GND	Ground (0V)
-	NC	No connected
D4	$V_{CCA}$	Positive supply voltage
D3	$V_{CCB}$	Positive supply voltage
G5, G4	$I/O_{VA1}, I/O_{VA2}$	I <sup>2</sup> C Line ( $V_{CCA}$ referred)
G2, G3	$I/O_{VB1}, I/O_{VB2}$	I <sup>2</sup> C Line ( $V_{CCB}$ referred)

Table 3. Truth table

Inputs		Function		Output
$\overline{G}$	DIR	A bus	B bus	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

Note: X = don't care; Z = high Impedance

## 2.2 I<sup>2</sup>C bus function

Table 4. I<sup>2</sup>C Bus function table

$\overline{2G}$	$\overline{1G}$ , 1DIR, 2DIR	I/O input		Function
		I/O <sub>VA</sub>	I/O <sub>VB</sub>	
H	X	Z	Z	I <sup>2</sup> C disabled
L	X	L	L	I <sup>2</sup> C comm.
L	X	V <sub>CCA</sub>	V <sub>CCB</sub>	I <sup>2</sup> C comm.
L	X	Open	V <sub>CCB</sub>	I <sup>2</sup> C comm.
L	X	V <sub>CCA</sub>	Open	I <sup>2</sup> C comm.

Note: Open: If I/O<sub>VA</sub> is not driven then the I/O<sub>VB</sub> goes in high level V<sub>CCB</sub> by embedded 10 kΩ pull-up resistor. If I/O<sub>VB</sub> is not driven then the I/O<sub>VA</sub> will go in high level V<sub>CCB</sub> by embedded 10 kΩ pull-up resistor.

### 3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 5. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CCA}$	Supply voltage	-0.5 to +4.6	V
$V_{CCB}$	Supply voltage	-0.5 to +4.6	V
$V_I$	DC input voltage	-0.5 to +4.6	V
$V_{I/OA}$	DC I/O voltage (Output disabled)	-0.5 to +4.6	V
$V_{I/OB}$	DC I/O voltage (Output disabled)	-0.5 to +4.6	V
$V_{I/OA}$	DC I/O voltage	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OB}$	DC I/O voltage	-0.5 to $V_{CCB} + 0.5$	V
$V_{I/OVA}$	Level input voltage ( $I/O_{VA}$ )	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OVB}$	Level input voltage ( $I/O_{VB}$ )	-0.5 to $V_{CCB} + 0.5$	V
$I_{IK}$	DC input diode current	-20	mA
$I_{OK}$	DC output diode current	-50	mA
$I_{OA}$	DC output current	$\pm 50$	mA
$I_{OB}$	DC output current	$\pm 50$	mA
$I_{CCA}$	DC $V_{CC}$ or ground current	$\pm 100$	mA
$I_{CCB}$	DC $V_{CC}$ or ground current	$\pm 100$	mA
$P_d$	Power dissipation	400	mW
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_L$	Lead temperature (10 sec)	260	°C

### 3.1 Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Value	Unit
$V_{CCA}$	Supply voltage	2.3 to 3.6	V
$V_{CCB}$	Supply voltage	1.65 to 2.7	V
$V_I$	Input voltage (Dir, $\overline{G}$ )	0 to $V_{CCB}$	V
$V_{I/OA}$	I/O voltage	0 to $V_{CCA}$	V
$V_{I/OB}$	I/O voltage	0 to $V_{CCB}$	V
$V_{I/OVA}$	Level input voltage ( $I/O_{VA}$ )	0 to $V_{CCA}$	V
$V_{I/OVB}$	Level input voltage ( $I/O_{VB}$ )	0 to $V_{CCB}$	V
$T_{op}$	Operating temperature	-40 to +85	°C
dt/dv	Input rise and fall time	0 to 10	ns/V

## 4 Electrical characteristics

Table 7. DC specification for  $V_{CCA}$

Symbol	Parameter	Test condition			Value				Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
V <sub>IHA</sub>	High level input voltage (A <sub>n</sub> ) <sup>(1)</sup>	1.8	2.5		1.6		1.6		V
		1.8	3.3		2.0		2.0		
		2.5	3.3		2.0		2.0		
V <sub>ILA</sub>	Low level input voltage (A <sub>n</sub> ) <sup>(1)</sup>	1.8	2.5			0.7		0.7	V
		1.8	3.3			0.8		0.8	
		2.5	3.3			0.8		0.8	
V <sub>OHA</sub>	High level output voltage	2.3	3.0	I <sub>O</sub> = -100 μA	2.8		2.8		V
		2.3	3.0	I <sub>O</sub> = -8 mA	2.4		2.4		
		1.65	3.0	I <sub>O</sub> = -8 mA	2.4		2.4		
		1.65	2.3	I <sub>O</sub> = -6 mA	1.8		1.8		
V <sub>OLA</sub>	Low level output voltage	2.3	3.0	I <sub>O</sub> = 100 μA		0.2		0.2	V
		2.3	3.0	I <sub>O</sub> = 8 mA		0.55		0.55	
		1.65	3.0	I <sub>O</sub> = 8 mA		0.55		0.55	
		1.65	2.3	I <sub>O</sub> = 6 mA		0.40		0.40	
I <sub>IA</sub>	Input leakage current	2.7	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		±0.5		±5	μA
I <sub>IA(HOLD)</sub>	Input hold current	1.65	2.3	V <sub>I</sub> = 0.7 V	45		45		μA
		1.65	2.3	V <sub>I</sub> = 1.6 V	-45		-45		
		1.65	3.0	V <sub>I</sub> = 0.8 V	75		75		
		1.65	3.0	V <sub>I</sub> = 2.0 V	-75		-75		
		2.3	3.0	V <sub>I</sub> = 0.8 V	75		75		
		2.3	3.0	V <sub>I</sub> = 2.0 V	-75		-75		
		2.7	3.6	V <sub>I</sub> = 0 to 3.6 V				±500	
I <sub>OZA</sub>	High impedance output leakage current	2.7	3.6	V <sub>IA</sub> = GND or 3.6 V V <sub>IB</sub> = V <sub>IHB</sub> or V <sub>ILB</sub> $\overline{G}$ = V <sub>CCB</sub>		±1.0		±10	μA
I <sub>OFF</sub>	Power off leakage current	0	0	V <sub>IA</sub> = GND to 3.6 V V <sub>IB</sub> = GND to 3.6 V $\overline{G}$ , Dir = GND to 3.6 V		±1.0		±10	μA



Table 7. DC specification for  $V_{CCA}$  (continued)

Symbol	Parameter	Test condition			Value				Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
I <sub>OFFI2C</sub>	Power Off I <sup>2</sup> C line leakage current	1.65 to 2.7	0	I/O <sub>VA1,2</sub> = GND or V <sub>CCA</sub> ; I/O <sub>VB1,2</sub> = GND or V <sub>CCB</sub> ; $\overline{2G} = V_{CCB}$		1.0		5	μA
I <sub>CCtA</sub>	Quiescent supply current	1.95	3.6	V <sub>IA</sub> = V <sub>CCA</sub> or GND		2		20	μA
		1.95	2.7	V <sub>IB</sub> = V <sub>CCB</sub> or GND					
		2.7	3.6	I/O <sub>VA1,2</sub> = V <sub>CCA</sub> or Open; Dir, $\overline{G} = \text{GND or } V_{CCB}$					
ΔI <sub>CCtA</sub>	Maximum quiescent supply current / Input (An)	2.7	3.6	V <sub>IA</sub> =V <sub>CCA</sub> - 0.6V V <sub>IB</sub> =V <sub>CCB</sub> or GND				0.75	mA
		1.95	3.6						
		1.95	2.7						

1.  $V_{CC}$  range =  $3.3 \pm 0.3$ ;  $2.5 \pm 0.2\text{V}$  and  $2.8 \pm 0.1\text{V}$ ;  $1.8 \pm 0.15\text{V}$

Table 8. DC specification for  $V_{CCB}$ 

Symbol	Parameter	Test condition			Value				Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
V <sub>IHB</sub>	High level input voltage (Bn, Dir, $\overline{G}$ ) <sup>(1)</sup>	1.8	2.5		0.65V <sub>CCB</sub>		0.65V <sub>CCB</sub>		V
		1.8	3.3		0.65V <sub>CCB</sub>		0.65V <sub>CCB</sub>		
		2.5	3.3		1.6		1.6		
V <sub>ILB</sub>	Low level input voltage (Bn, Dir, $\overline{G}$ ) <sup>(1)</sup>	1.8	2.5			0.35V <sub>CCB</sub>		0.35V <sub>CCB</sub>	V
		1.8	3.3			0.35V <sub>CCB</sub>		0.35V <sub>CCB</sub>	
		2.5	3.3			0.7		0.7	
V <sub>OHB</sub>	High level output voltage	2.3	3.0	I <sub>O</sub> =-100μA	2.1		2.1		V
		2.3	3.0	I <sub>O</sub> =-18mA	1.7		1.7		
		1.65	3.0	I <sub>O</sub> =-6mA	1.25		1.25		
		1.65	2.3	I <sub>O</sub> =-6mA	1.25		1.25		
V <sub>OLB</sub>	Low level output voltage	2.3	3.0	I <sub>O</sub> =100μA		0.2		0.2	V
		2.3	3.0	I <sub>O</sub> =18mA		0.60		0.60	
		1.65	3.0	I <sub>O</sub> =6mA		0.30		0.30	
		1.65	2.3	I <sub>O</sub> =6mA		0.30		0.30	
I <sub>IB</sub>	Input leakage current	2.7	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		±0.5		±5	μA

Table 8. DC specification for  $V_{CCB}$  (continued)

Symbol	Parameter	Test condition			Value				Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
I <sub>IB(HOLD)</sub>	Input hold current	1.65	2.3	V <sub>I</sub> = 0.57 V	25		25		μA
		1.65	2.3	V <sub>I</sub> = 1.07 V	-25		-25		
		1.65	3.0	V <sub>I</sub> = 0.57 V	25		25		
		1.65	3.0	V <sub>I</sub> = 1.07 V	-25		-25		
		2.3	3.0	V <sub>I</sub> = 0.7 V	45		45		
		2.3	3.0	V <sub>I</sub> = 1.6 V	-45		-45		
		2.7	3.6	V <sub>I</sub> = 0 to 2.7 V				±500	
I <sub>OZB</sub>	High impedance output leakage current	2.7	3.6	V <sub>IA</sub> = V <sub>IHA</sub> or V <sub>ILA</sub> V <sub>IB</sub> = GND or 2.7V $\overline{G}$ = V <sub>CCB</sub>		±1.0		±10	μA
I <sub>CCtB</sub>	Quiescent supply current	1.95	3.6	V <sub>IA</sub> =V <sub>CCA</sub> or GND		2		20	μA
		1.95	2.7	V <sub>IB</sub> =V <sub>CCB</sub> or GND					
		2.7	3.6	Dir or $\overline{G}$ =V <sub>CCB</sub> or GND I/O <sub>VA1,2</sub> =V <sub>CCA</sub> or Open					
ΔI <sub>CCtB</sub>	Maximum quiescent supply current / Input (Bn, DIR, $\overline{G}$ )	2.7	3.6	V <sub>IB</sub> =V <sub>CCB</sub> - 0.6V V <sub>IA</sub> =V <sub>CCA</sub> or GND				0.75	mA
		1.95	3.6						
		1.95	2.7						

1.  $V_{CC}$  range =  $3.3\pm 0.3$ ;  $2.5\pm 0.2\text{ V}$  and  $2.8\pm 0.1\text{ V}$ ;  $1.8\pm 0.15\text{ V}$

Table 9. Dynamic switching characteristics

Symbol	Parameter	Test condition			Value					Unit
		V <sub>C<sub>CB</sub></sub> (V)	V <sub>C<sub>CA</sub></sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max.	
V <sub>OLPA</sub>	Dynamic low level quiet An output	1.8	2.5	C <sub>L</sub> = 30 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = V <sub>CC</sub>		0.25				V
		1.8	3.3			0.35				
		2.5	3.3			0.35				
V <sub>OLPB</sub>	Dynamic low level quiet Bn output	1.8	2.5	C <sub>L</sub> = 30 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = V <sub>CC</sub>		0.25				V
		1.8	3.3			0.25				
		2.5	3.3			0.6				
V <sub>OLVA</sub>	Dynamic low level quiet An output	1.8	2.5	C <sub>L</sub> = 30 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = V <sub>CC</sub>		-0.25				V
		1.8	3.3			-0.35				
		2.5	3.3			-0.35				
V <sub>OLVB</sub>	Dynamic low level quiet Bn output	1.8	2.5	C <sub>L</sub> = 30 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = V <sub>CC</sub>		-0.25				V
		1.8	3.3			-0.25				
		2.5	3.3			-0.6				
V <sub>OHVA</sub>	Dynamic high level quiet An output	1.8	2.5	C <sub>L</sub> = 30 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = V <sub>CC</sub>		2.1				V
		1.8	3.3			2.6				
		2.5	3.3			2.6				
V <sub>OHVB</sub>	Dynamic high level quiet Bn output	1.8	2.5	C <sub>L</sub> = 30 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = V <sub>CC</sub>		1.7				V
		1.8	3.3			1.7				
		2.5	3.3			2.0				

Table 10. DC specification I<sup>2</sup>C lines

Symbol	Parameter	Test condition			Value				Unit
		V <sub>CCB</sub> (V) (1)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C		-40 to 85 °C		
					Min.	Max.	Min.	Max.	
V <sub>IH2</sub>	High level input voltage (I/O <sub>VB1</sub> , I/O <sub>VB2</sub> )	1.8	2.65 to 3.6		0.7 V <sub>CCB</sub>	V <sub>CCB</sub>	0.7 V <sub>CCB</sub>	V <sub>CCB</sub>	V
		1.8	2.65 to 3.6		0.7 V <sub>CCB</sub>	V <sub>CCB</sub>	0.7 V <sub>CCB</sub>	V <sub>CCB</sub>	
	High level input voltage (I/O <sub>VA1</sub> , I/O <sub>VA2</sub> )	1.8	2.65 to 3.6		0.7 V <sub>CCA</sub>	V <sub>CCA</sub>	0.7 V <sub>CCA</sub>	V <sub>CCA</sub>	
		1.8	2.65 to 3.6		0.7 V <sub>CCA</sub>	V <sub>CCA</sub>	0.7 V <sub>CCA</sub>	V <sub>CCA</sub>	
V <sub>IL2</sub>	Low level input voltage (I/O <sub>VB1</sub> , I/O <sub>VB2</sub> )	1.8	2.65 to 3.6		0	0.25	0	0.25	V
		1.8	2.65 to 3.6		0	0.25	0	0.25	
	Low level input voltage (I/O <sub>VA1</sub> , I/O <sub>VA2</sub> )	1.8	2.65 to 3.6		0	0.25	0	0.25	
		1.8	2.65 to 3.6		0	0.25	0	0.25	
V <sub>OH2</sub>	High level output voltage (I/O <sub>VB1</sub> , I/O <sub>VB2</sub> )	1.65	2.3	I <sub>OH</sub> = -20 μA; V <sub>I/OVA</sub> =V <sub>CCA</sub>	V <sub>CCB</sub> -0.4		V <sub>CCB</sub> -0.4		V
	High level output voltage (I/O <sub>VA1</sub> , I/O <sub>VA2</sub> )	1.65	2.3	I <sub>OH</sub> = -20 μA; V <sub>I/OVB</sub> =V <sub>CCB</sub>	V <sub>CCA</sub> -0.4		V <sub>CCA</sub> -0.4		
V <sub>OL2</sub>	Low level output voltage (I/O <sub>VB1</sub> , I/O <sub>VB2</sub> ), (I/O <sub>VA1</sub> , I/O <sub>VA2</sub> )	1.65	2.3	I <sub>OL</sub> = 1 mA; V <sub>I/OVB</sub> or V <sub>I/OVA</sub> =GND		0.35		0.35	V

1. V<sub>CC</sub> range = 1.8±0.15 V

Table 11. AC electrical characteristics

Symbol	Parameter	Test condition			Value		Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		-40 to 85 °C		
					Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time An to Bn	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.8	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	6.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time Bn to An <sup>(1)</sup>	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.5	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output enable time G̅ to An	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output enable time G̅ to Bn	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	8.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	8.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.6	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output disable time G̅ to An	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	5.2	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.6	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.8	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output disable time G̅ to Bn	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω	1.0	4.6	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	4.5	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to output skew time <sup>(2)</sup> <sup>(3)</sup>	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 30 pF R <sub>L</sub> = 500 Ω		0.5	ns
		1.8 ± 0.15	3.3 ± 0.3			0.5	
		2.5 ± 0.2	3.3 ± 0.3			0.75	

1. To add 2.5 ns at t<sub>PLH</sub>, t<sub>PHL</sub> max propagation delay time Bn to An at V<sub>CCB</sub> = 1.8 ± 0.15 V; V<sub>CCA</sub> = 2.8 ± 0.1 V; R<sub>L</sub> = 500 Ω when C<sub>L</sub> = 60 pF.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|).
3. Parameter guaranteed by design.

Table 12. AC I<sup>2</sup>C electrical characteristics

Symbol	Parameter	Test condition			Value		Unit
		V <sub>CCB</sub> (V) <sup>(1)</sup>	V <sub>CCA</sub> (V) <sup>(1)</sup>		-40 to 85 °C		
					Min.	Max.	
t <sub>rl/O</sub>	Rise time I <sup>2</sup> C input/output voltage (20% to 80%)	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 15 pF t <sub>rl/O</sub> = 15 ns		250	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
t <sub>fl/O</sub>	Fall time I <sup>2</sup> C input/output voltage (80% to 20%)	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 15 pF t <sub>fl/O</sub> = 15 ns		250	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
t <sub>PLH</sub>	Propagation delay time I <sup>2</sup> C I/O voltage (20% to 80%) (low to high)	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 15 pF t <sub>rl/O</sub> = 15 ns		100	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
t <sub>PHL</sub>	Propagation delay time I <sup>2</sup> C I/O voltage (20% to 80%) high to low)	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 15 pF t <sub>rl/O</sub> = 15 ns		100	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
f <sub>I/OVA</sub> , f <sub>I/OVB</sub>	I <sup>2</sup> C lines data rate	1.8 ± 0.15	2.5 ± 0.2	C <sub>L</sub> = 15 pF t <sub>rl/O</sub> = 15 ns	400		KHz
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				

1. V<sub>CC</sub> range = 3.3±0.3; 2.5±0.2 V and 2.8 ±0.1 V; 1.8 ±0.15 V

Table 13. Capacitance characteristics

Symbol	Parameter	Test condition			Value					Unit
		V <sub>CCB</sub> (V)	V <sub>CCA</sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
C <sub>INB</sub>	Input capacitance	open	open			5				pF
C <sub>I/O</sub>	Input/Output capacitance	2.5	3.3			6				pF
C <sub>PD</sub> <sup>(1)</sup>	Power dissipation capacitance	2.5	3.3	f = 10MHz		28				pF
		1.8	3.3			28				pF

1. C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average current can be obtained by the following equation.  
 $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/14$  (per circuit)

# 5 Test circuit

Figure 4. Test circuit

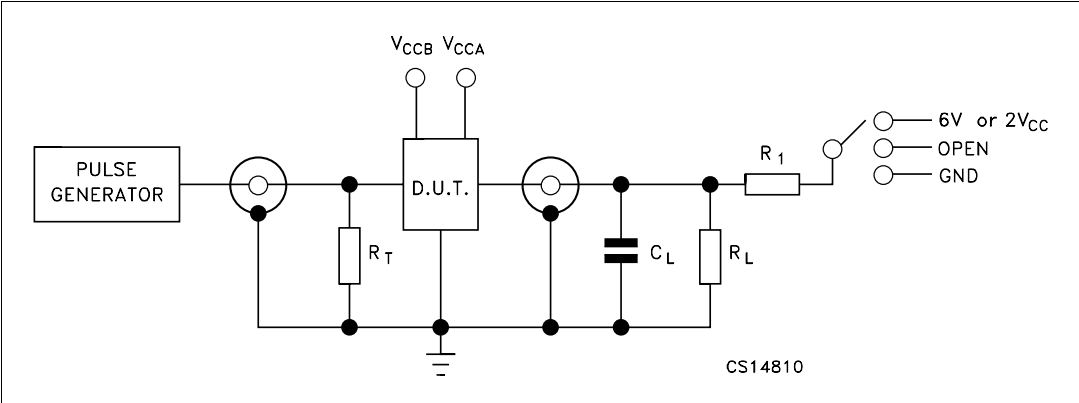


Table 14. Test circuit

Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 3.0$ to $3.6$ V)	6 V
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 2.3$ to $2.7$ V or $V_{CC} = 1.65$ to $1.95$ V)	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 10/30$  pF or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$  or equivalent

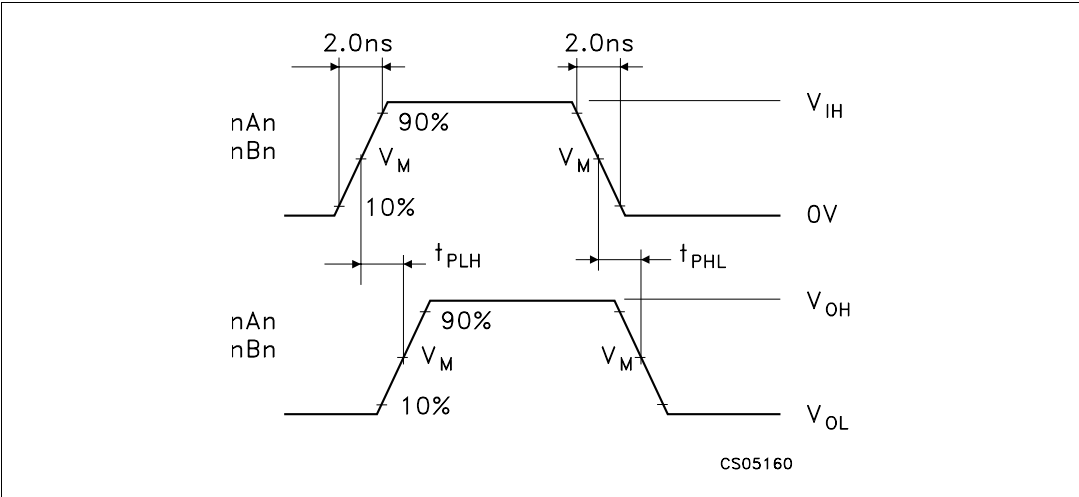
$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

6 Waveforms

Table 15. Waveform symbol value

Symbol	V <sub>CC</sub>		
	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V
V <sub>IH</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>M</sub>	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>X</sub>	V <sub>OL</sub> +0.3V	V <sub>OL</sub> +0.15V	V <sub>OL</sub> +0.15V
V <sub>Y</sub>	V <sub>OL</sub> -0.3V	V <sub>OL</sub> -0.15V	V <sub>OL</sub> -0.15V

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)





The diagram illustrates the timing characteristics of the SC13231. It features three main signal traces:  $\overline{nG}$  (input),  $nAn$  and  $nBn$  (output), and  $nAn$  and  $nBn$  (load). The input  $\overline{nG}$  is a square wave with a period of 2.0ns, switching between  $V_{IH}$  and GND. The output  $nAn$  and  $nBn$  is a square wave that switches between  $V_{OH}$  and GND. The load  $nAn$  and  $nBn$  is a square wave that switches between 3.0V or  $V_{CC}$  and  $V_{OL}$ . The timing parameters are defined as follows:

- $t_{PZH}$ : Propagation delay from input  $\overline{nG}$  to output  $nAn$  and  $nBn$  when the input transitions from high to low.
- $t_{PHZ}$ : Propagation delay from input  $\overline{nG}$  to output  $nAn$  and  $nBn$  when the input transitions from low to high.
- $t_{PZL}$ : Propagation delay from input  $\overline{nG}$  to load  $nAn$  and  $nBn$  when the input transitions from high to low.
- $t_{PLZ}$ : Propagation delay from input  $\overline{nG}$  to load  $nAn$  and  $nBn$  when the input transitions from low to high.

The voltage levels are defined as  $V_M$  (mid-level),  $V_{OH}$  (output high),  $V_Y$  (output low),  $V_{IH}$  (input high),  $V_{OL}$  (output low), and  $V_{CC}$  (supply voltage).

The diagram illustrates the timing characteristics of the CS18070. It shows two signal transitions: a rising edge (left) and a falling edge (right). The top signal, labeled  $I/O_{VA}, I/O_{VB}$ , transitions between  $V_{CCA}, V_{CCB}$  and  $0V$ . The bottom signal, labeled  $I/O_{VB}, I/O_{VA}$ , transitions between  $V_{OH}$  and  $V_{OL}$ . Key timing parameters are indicated:  $t_{r1/o}$  and  $t_{f1/o}$  for the input signals,  $t_{PLH}$  and  $t_{PHZ}$  for the propagation delays, and  $t_{r1/o}$  and  $t_{f1/o}$  for the output signals. The signal levels are marked at 20%, 50%, and 80% of the full swing.

## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

$\mu$ TFBGA42 MECHANICAL DATA						
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	0.30	0.35	9.8	11.8	13.8
D	3.9	4.0	4.1	153.5	157.5	161.4
D1		3			118.1	
E	3.4	3.5	3.6	133.9	137.8	141.7
E1		2.5			98.4	
e		0.5			19.7	
SE		0.25			9.8	

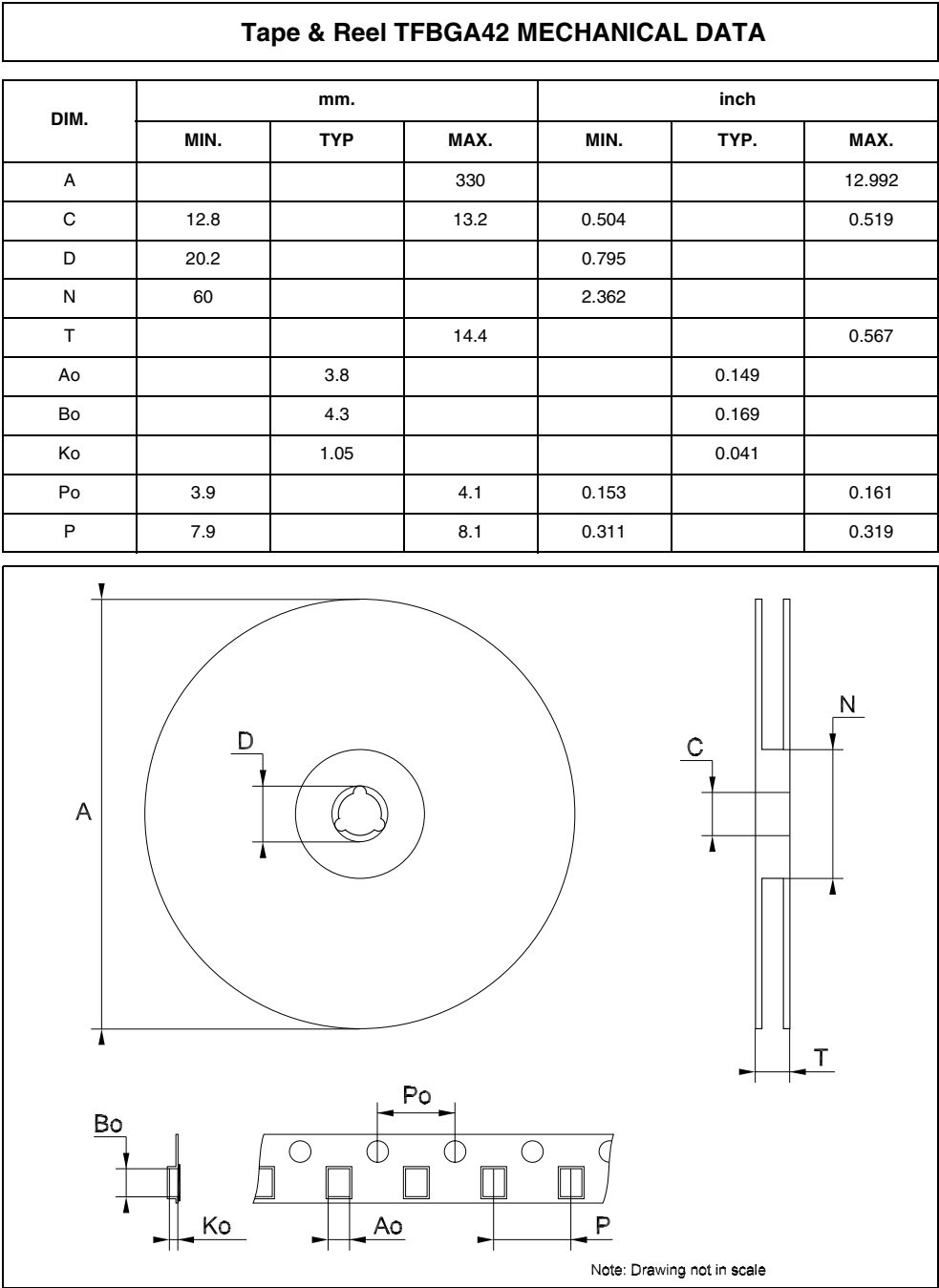
The drawing illustrates the mechanical specifications of the  $\mu$ TFBGA42 package. The top view shows a rectangular array of 42 pins (6 columns by 7 rows). Key dimensions include:
 

- E**: Total width of the pin array.
- E1**: Width of the central pin columns.
- SE**: Stagger between columns.
- e**: Pin pitch.
- D**: Total height of the package.
- D1**: Height of the pin array.
- A**: Total thickness of the package.
- A1**: Thickness of the base.
- A2**: Thickness of the top layer.
- b**: Pin diameter.

 A 'DISTINGUISH FEATURE' is indicated at the bottom-left corner of the pin array. The side view shows the package profile with a 'SEATING PLANE' and a 'COPLANARITY' specification of 0.10 [C]. A note  $\phi b \ 42x$  refers to the pin diameter.

7513237/A

Figure 9.  $\mu$ TFBGA42 tape and reel



## 8 Revision history

**Table 16. Document revision history**

Date	Revision	Changes
01-Oct-2004	1	Initial release.
31-Mar-2005	2	Document status promoted from preliminary data to datasheet.
04-Mar-2009	3	Document reformatted. TSSOP and TFBGA54 packages removed.

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