FUNCTIONAL BLOCKS

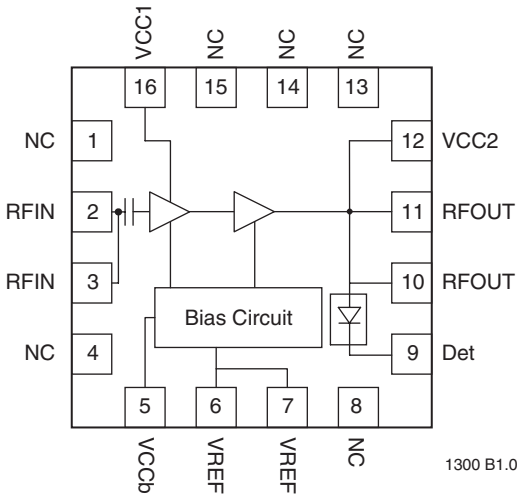


FIGURE 1: Functional Block Diagram

PIN ASSIGNMENTS

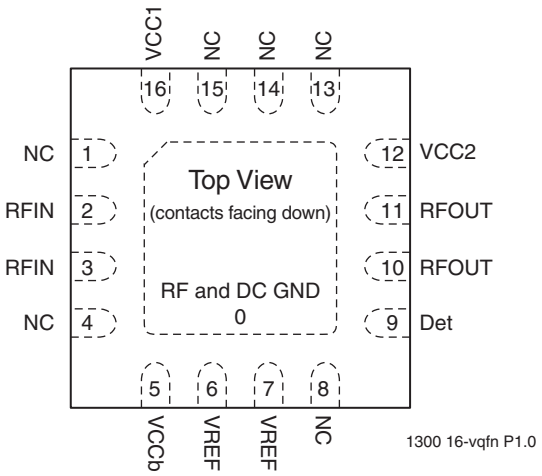


FIGURE 2: Pin Assignments for 16-contact VQFN

PIN DESCRIPTIONS

TABLE 1: Pin Description

Symbol	Pin No.	Pin Name	Type[1]	Function
GND	0	Ground		The center pad should be connected to RF ground with several low inductance, low resistance vias
NC	1	No Connection		Unconnected pin
RFIN	2		I	RF input, DC decoupled
RFIN	3		I	RF input, DC decoupled
NC	4	No Connection		Unconnected pin
VCCb	5	Power Supply	PWR	Supply voltage for bias circuit
VREF	6		PWR	1st and 2nd stage idle current control
VREF	7		PWR	1st and 2nd stage idle current control
NC	8	No Connection		Unconnected pin
Det	9		O	On-chip power detector
RFOUT	10		O	RF output
RFOUT	11		O	RF output
VCC2	12	Power Supply	PWR	Power supply, 2nd stage
NC	13	No Connection		Unconnected pin
NC	14	No Connection		Unconnected pin
NC	15	No Connection		Unconnected pin
VCC1	16	Power Supply	PWR	Power supply, 1st stage

T1.0 1300

1. I=Input, O=Output

ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the power amplifier interface signals. Refer to Table 2 for the DC voltage and current specifications. Refer to Figures 3 through 18 for the RF performance.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pins 2 and 3 (P_{IN}) . . . . . +5 dBm
Average output power (P_{OUT})[1] . . . . . +26 dBm
Supply Voltage at pins 5, 12, and 16 (V_{CC}) . . . . . -0.3V to +4.0V
Reference voltage to pins 6 and 7 (V_{REF}) . . . . . -0.3V to +3.3V
DC supply current (I_{CC}) . . . . . 400 mA
Operating Temperature (T_A) . . . . . -40ºC to +85ºC
Storage Temperature (T_{STG}) . . . . . -40ºC to +120ºC
Maximum Junction Temperature (T_J) . . . . . +150ºC
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds

1. Never measure with CW source. Pulsed single-tone source with <50% duty cycle is recommended. Exceeding the maximum rating of average output power could cause permanent damage to the device.

Operating Range

Range	Ambient Temp	V_{CC}
Industrial	-40°C to +85°C	3.3V

TABLE 2: DC Electrical Characteristics

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Conditions
V_{CC}	Supply Voltage at pins 5, 12, 16	3.0	3.3	3.6	V	
I_{CC}	Supply Current					
	for 802.11g, 22 dBm		210		mA	
	for 802.11b, 23 dBm		230		mA	
I_{CQ}	Idle current for 802.11g to meet EVM<4% @ 21dBm		70		mA	
I_{OFF}	Shut down current			0.1	µA	
V_{REG}	Reference Voltage for, with 110Ω resistor	2.75	2.85	2.95	V	

T2.1 1300

TABLE 3: AC Electrical Characteristics for Configuration

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range	2400		2485	MHz
P_{OUT}	Output power				
	@ PIN = -6 dBm 11b signals	22			dBm
	@ PIN = -7 dBm 11g signals	21			dBm
G	Small signal gain	28	29		dB
G_{VAR1}	Gain variation over band (2400~2485 MHz)			±0.5	dB
G_{VAR2}	Gain ripple over channel (20 MHz)		0.2		dB
ACPR	Meet 11b spectrum mask	22	23		dBm
	Meet 11g OFDM 54 Mbps spectrum mask	22	23		dBm
Added EVM	@ 21 dBm output with 11g OFDM 54 Mbps signal		4		%
2f, 3f, 4f, 5f	Harmonics at 22 dBm, without external filters			-40	dBc

T3.2 1300

TYPICAL PERFORMANCE CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 3.3V, T_A = 25°C, UNLESS OTHERWISE SPECIFIED

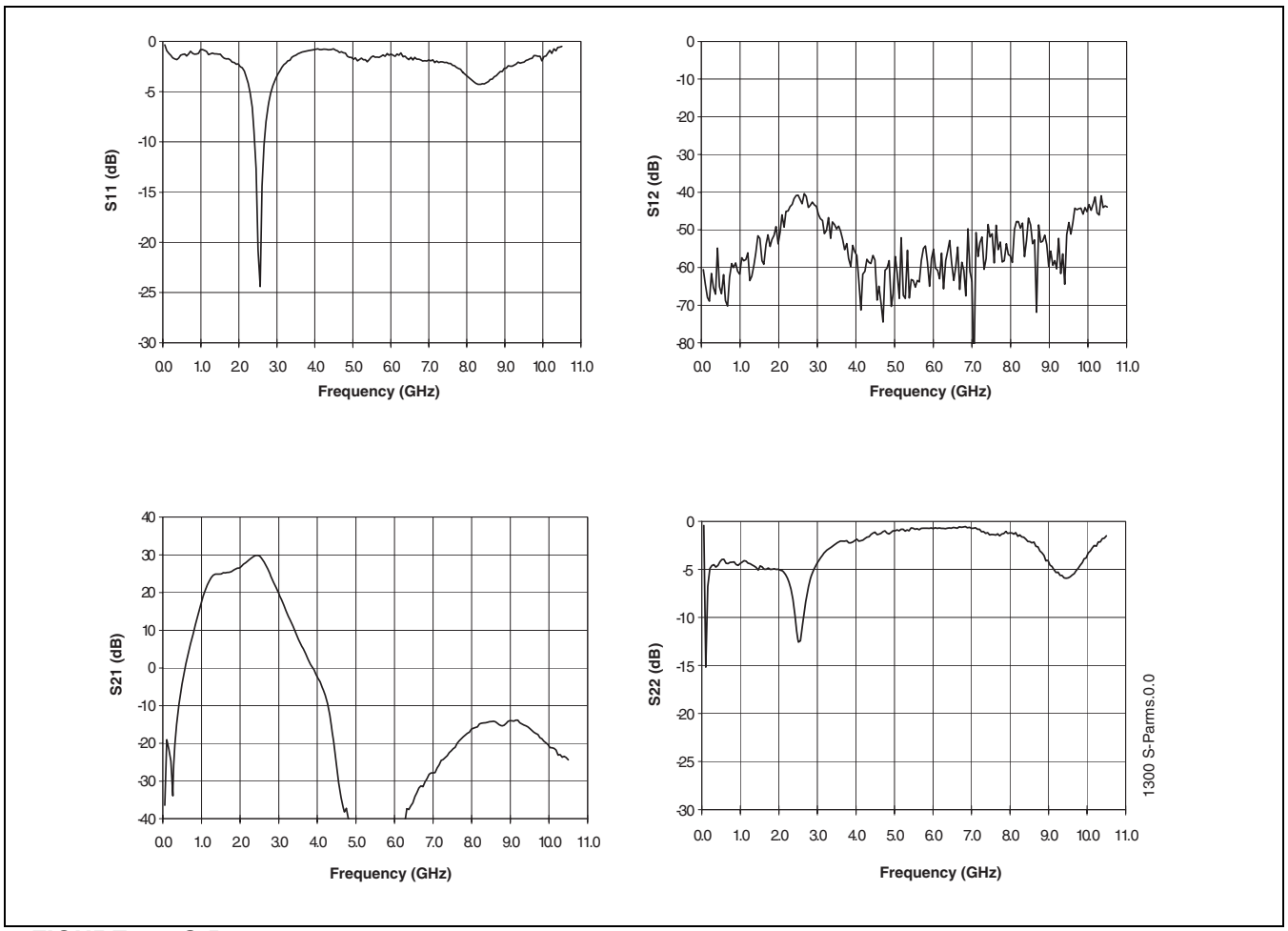


FIGURE 3: S-Parameters

TYPICAL PERFORMANCE CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 3.3V, T_A = 25°C, 54 MBPS 802.11G OFDM SIGNAL

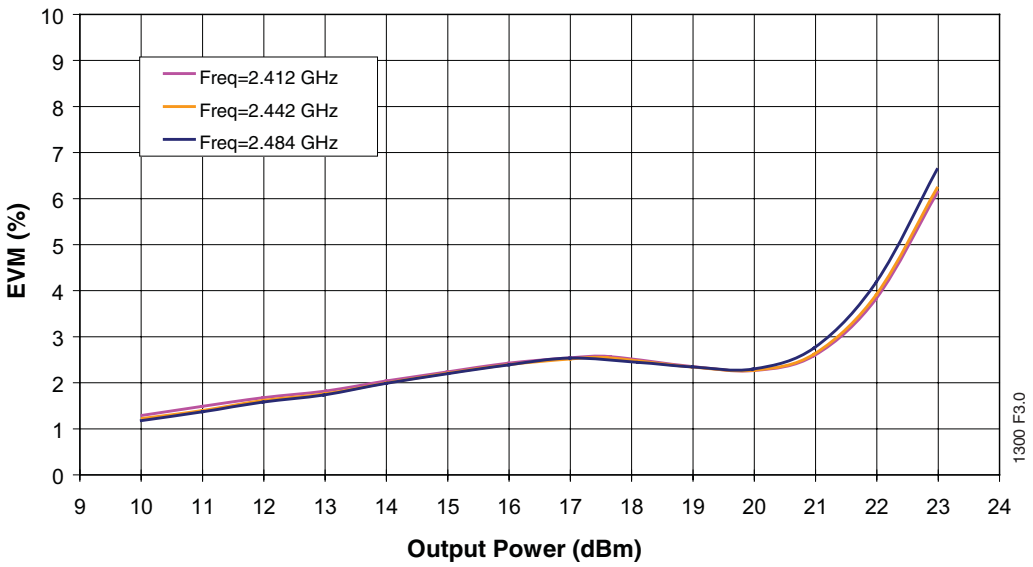


FIGURE 4: EMV versus Output Power

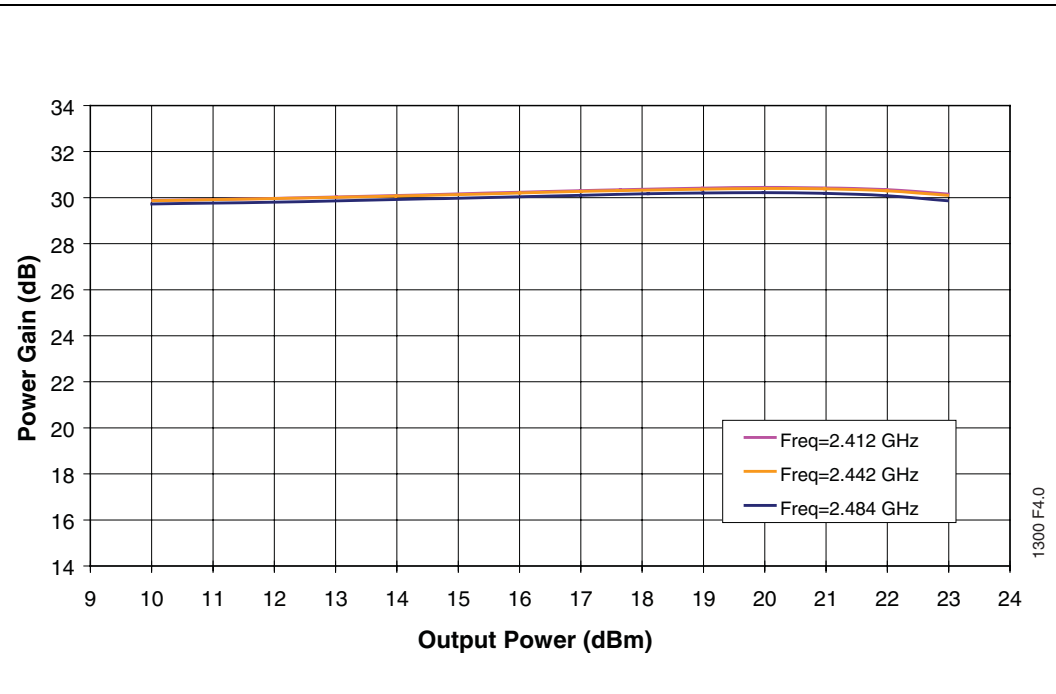


FIGURE 5: Power Gain versus Output Power

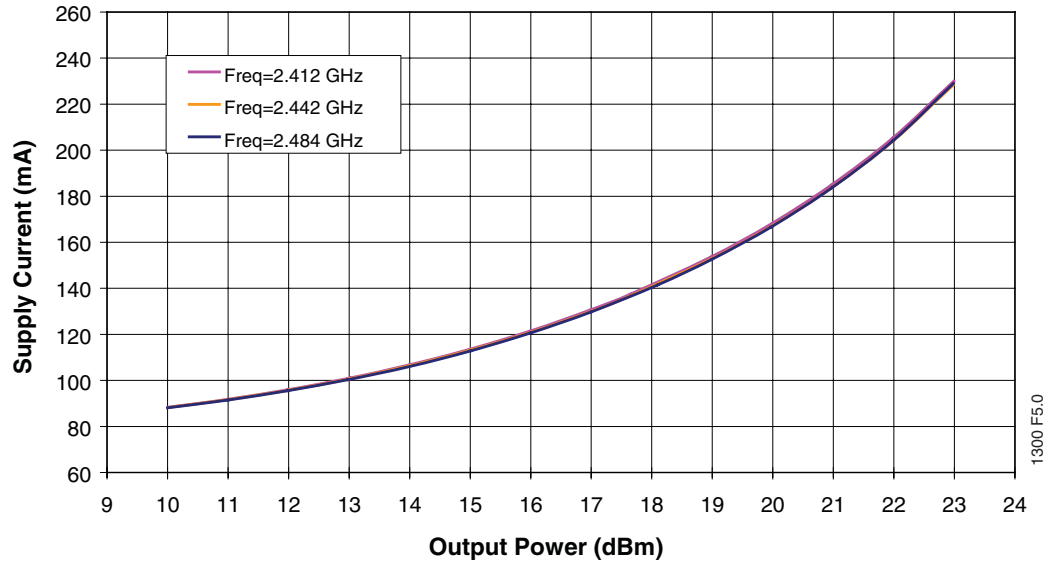


FIGURE 6: Total Current Consumption for 802.11g operation versus Output Power

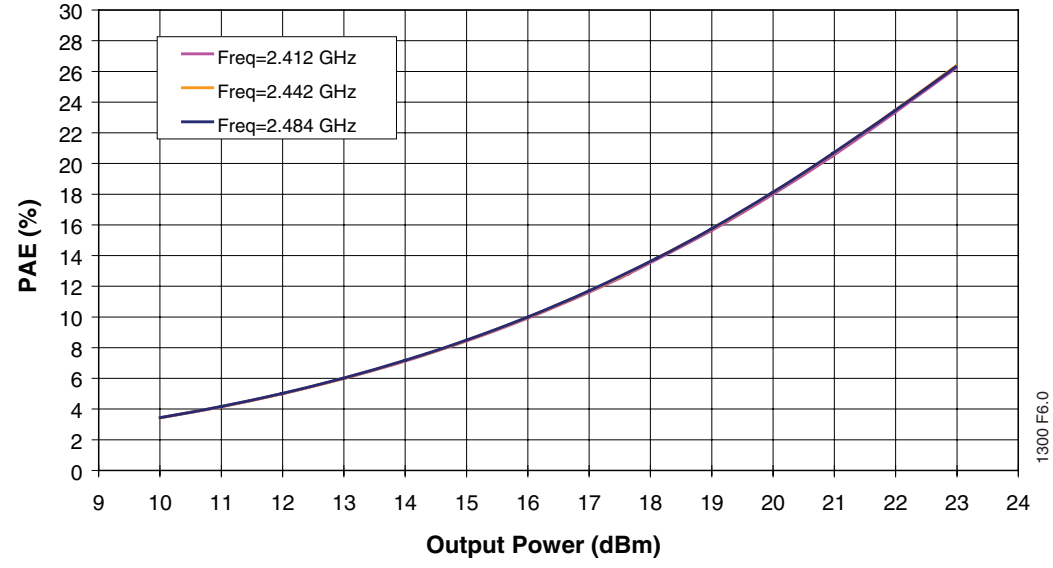


FIGURE 7: PAE versus Output Power

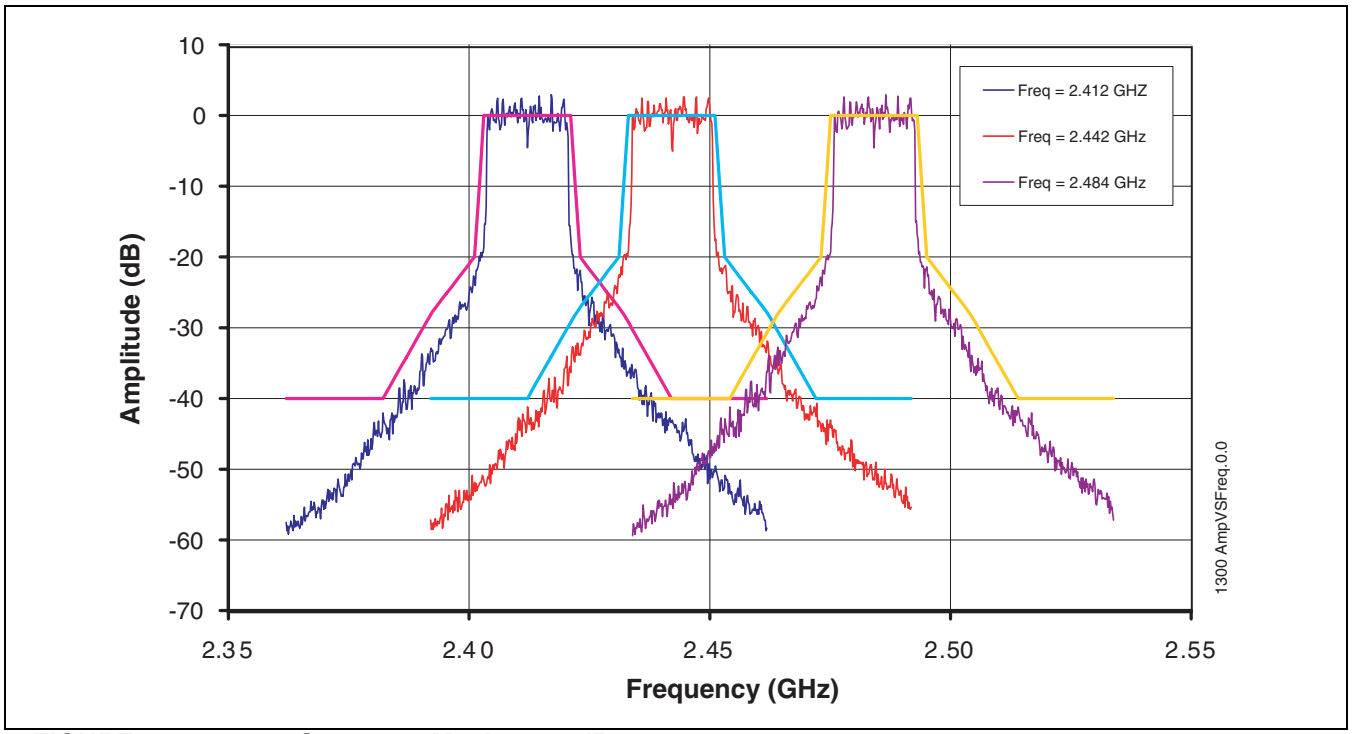


FIGURE 8: 802.11g Spectrum Mask at 23 dBm

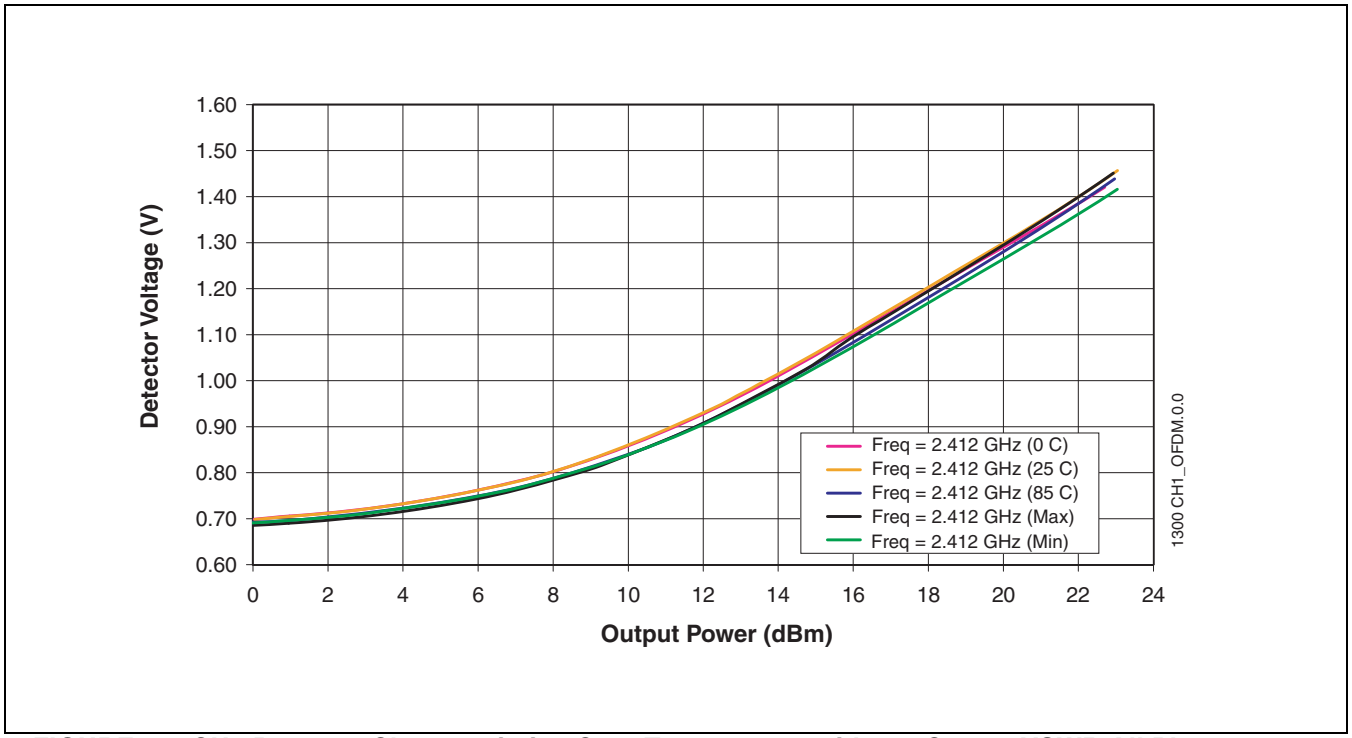


FIGURE 9: CH1 Detector Characteristics Over Temperature with 2:1 Output VSWR All Phases

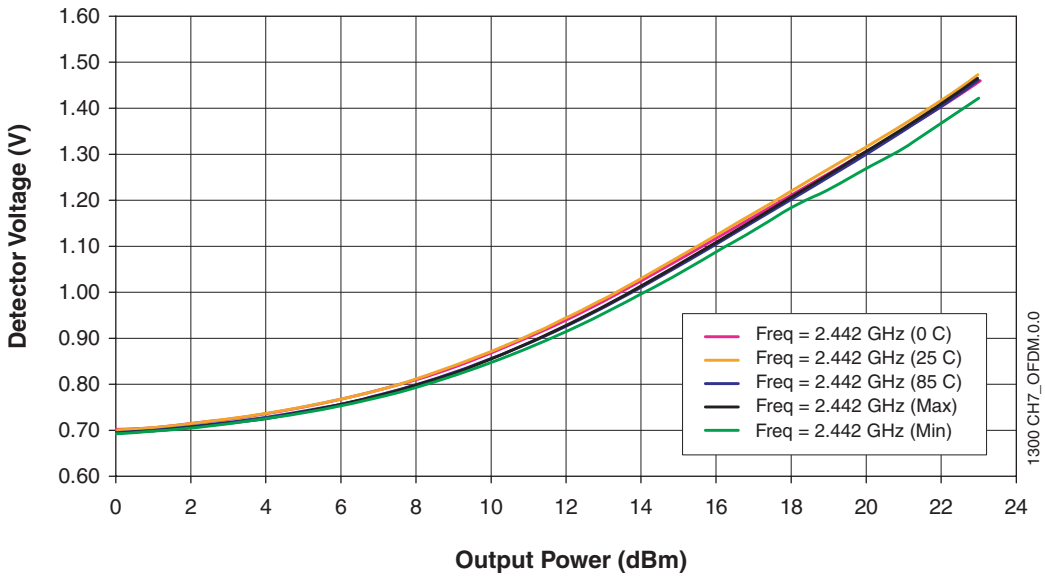


FIGURE 10: CH7 Detector Characteristics Over Temperature with 2:1 Output VSWR All Phases

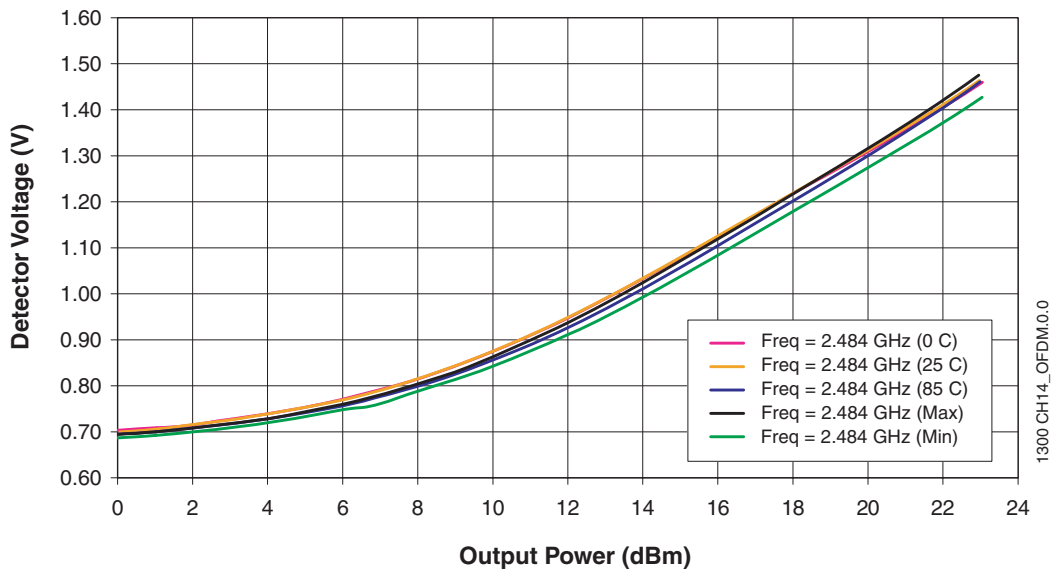


FIGURE 11: CH14 Detector Characteristics Over Temperature with 2:1 Output VSWR All Phases

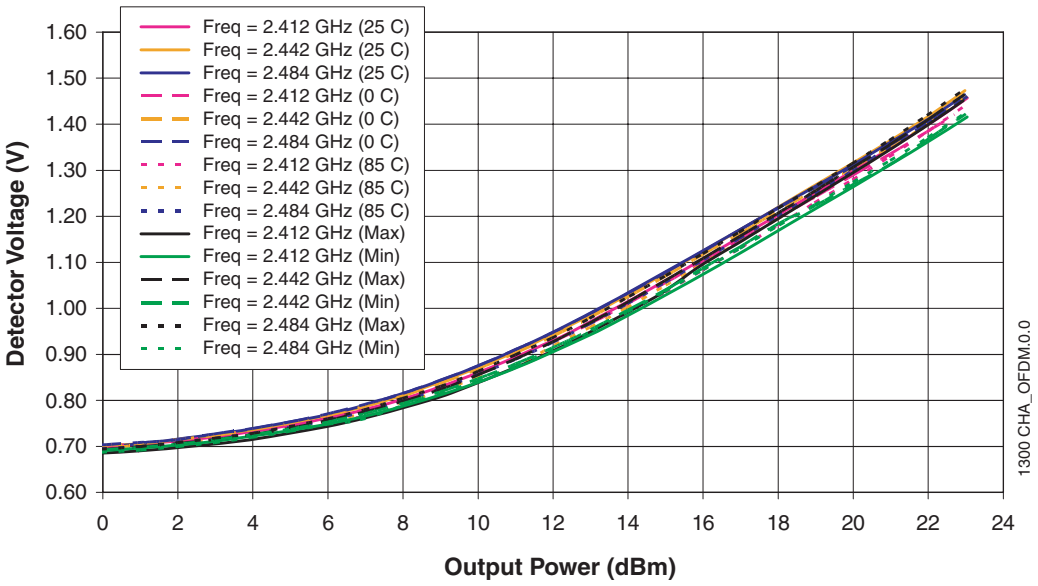


FIGURE 12: Detector Characteristics Over Temperature and Over Frequency with 2:1 Output VSWR All Phases

TYPICAL PERFORMANCE CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 3.3V, T_A = 25°C, 1 MBPS 802.11B CCK SIGNAL

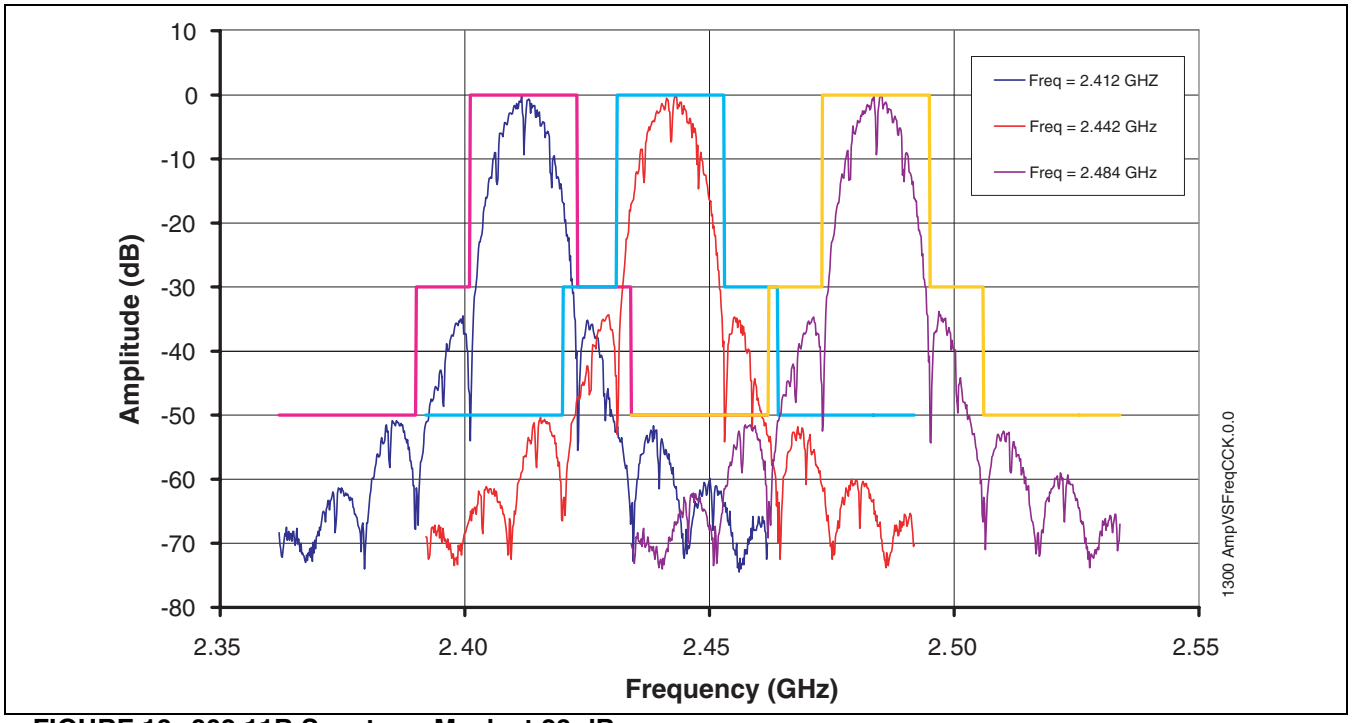


FIGURE 13: 802.11B Spectrum Mask at 23 dBm

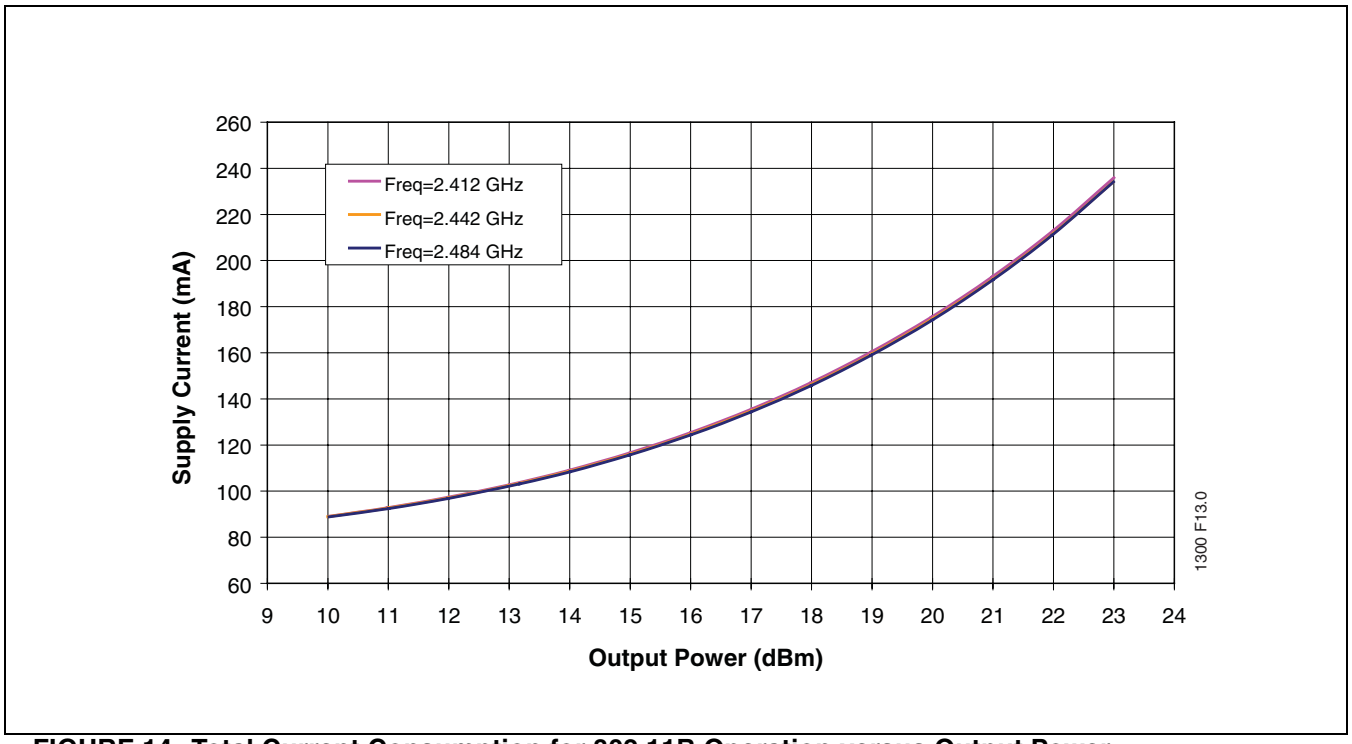


FIGURE 14: Total Current Consumption for 802.11B Operation versus Output Power

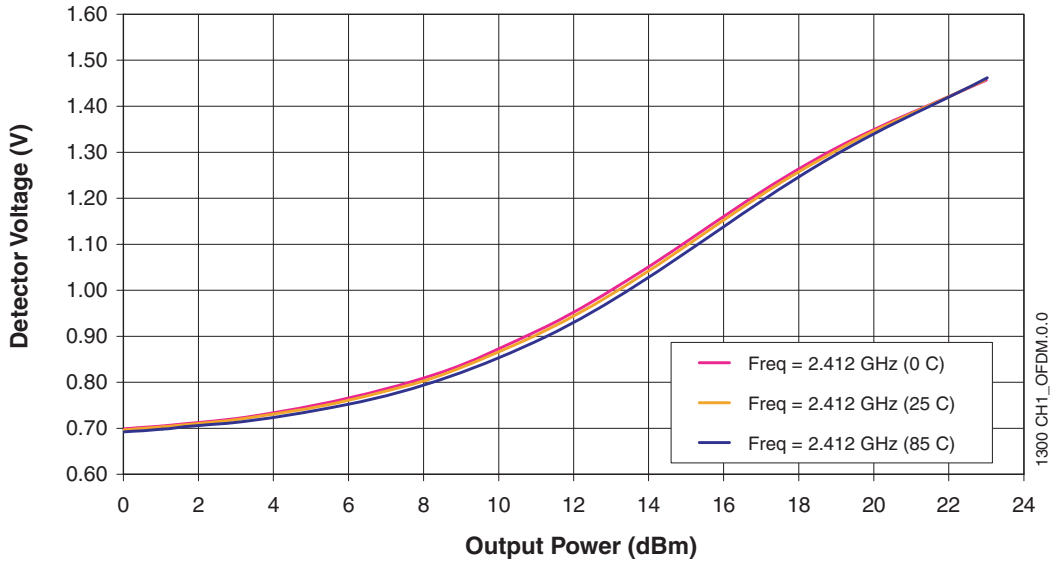


FIGURE 15: CH1 Detector Characteristics Over Temperature

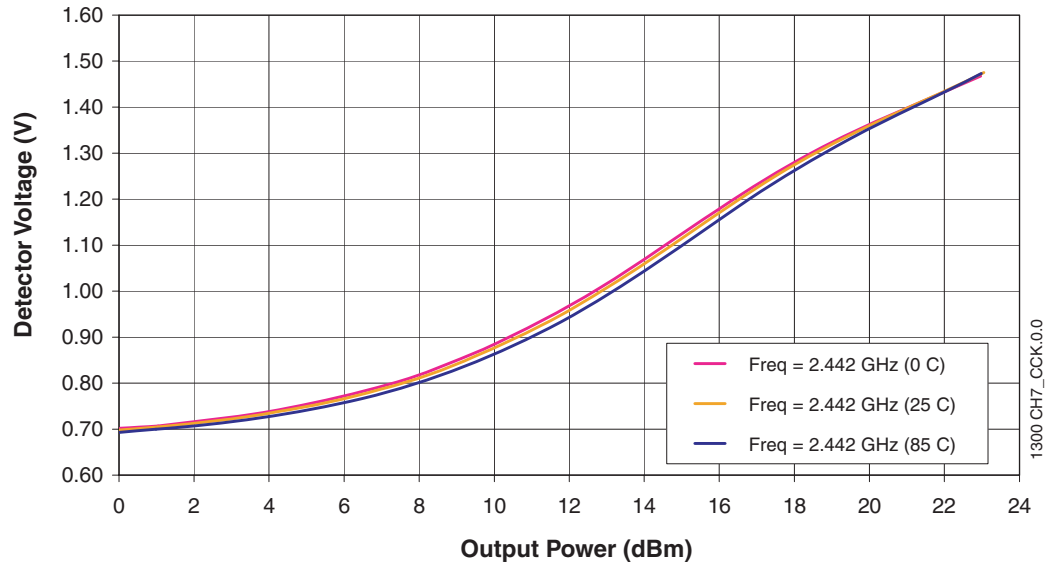


FIGURE 16: CH7 Detector Characteristics Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS
TEST CONDITIONS: V_{CC} = 3.3V, T_A=25°C, 1 MBPS 802.11B CCK SIGNAL

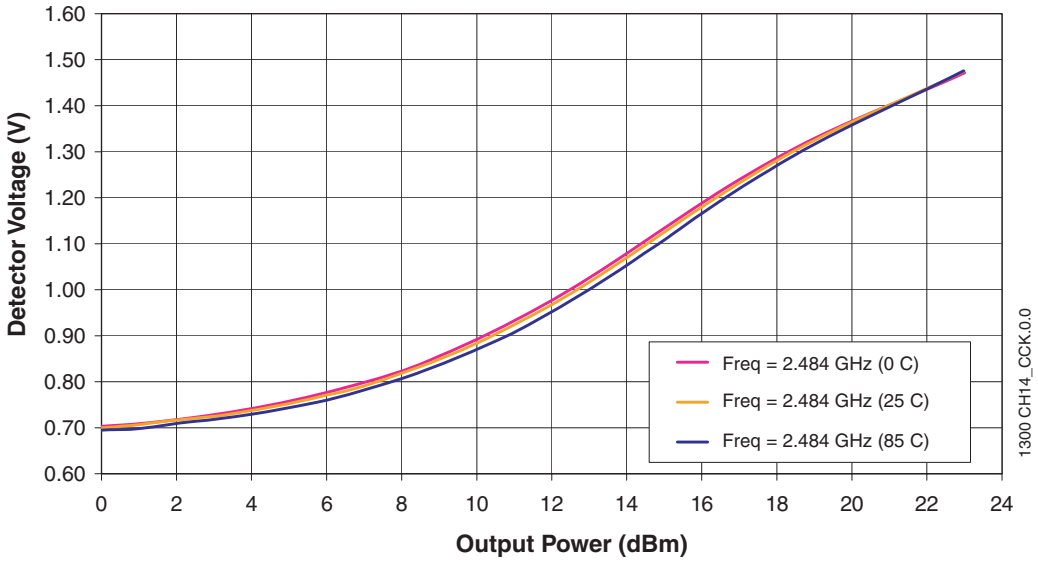


FIGURE 17: CH14 Detector Characteristics Over Temperature

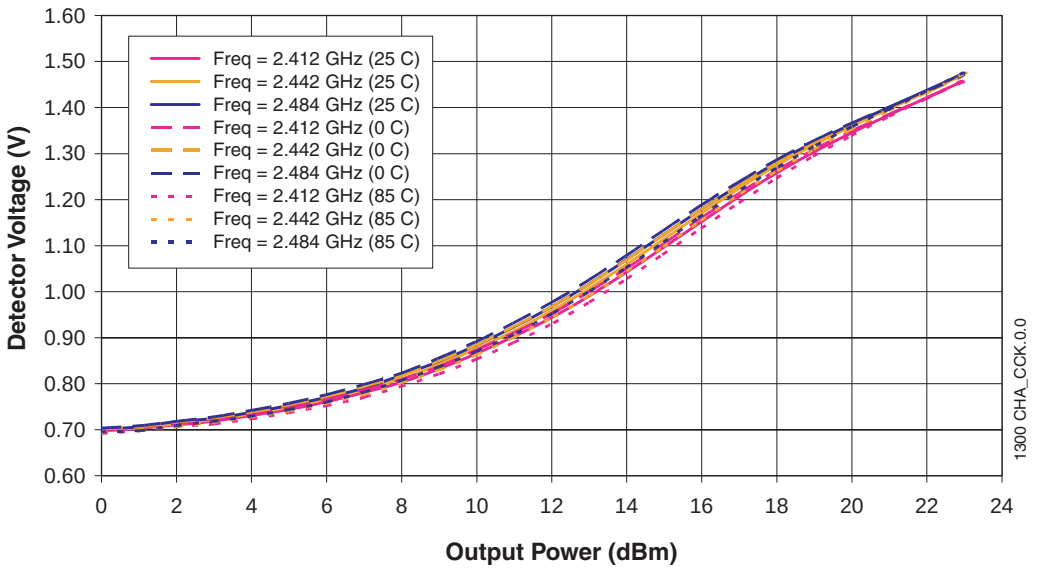


FIGURE 18: Detector Characteristics Over Temperature and Frequency

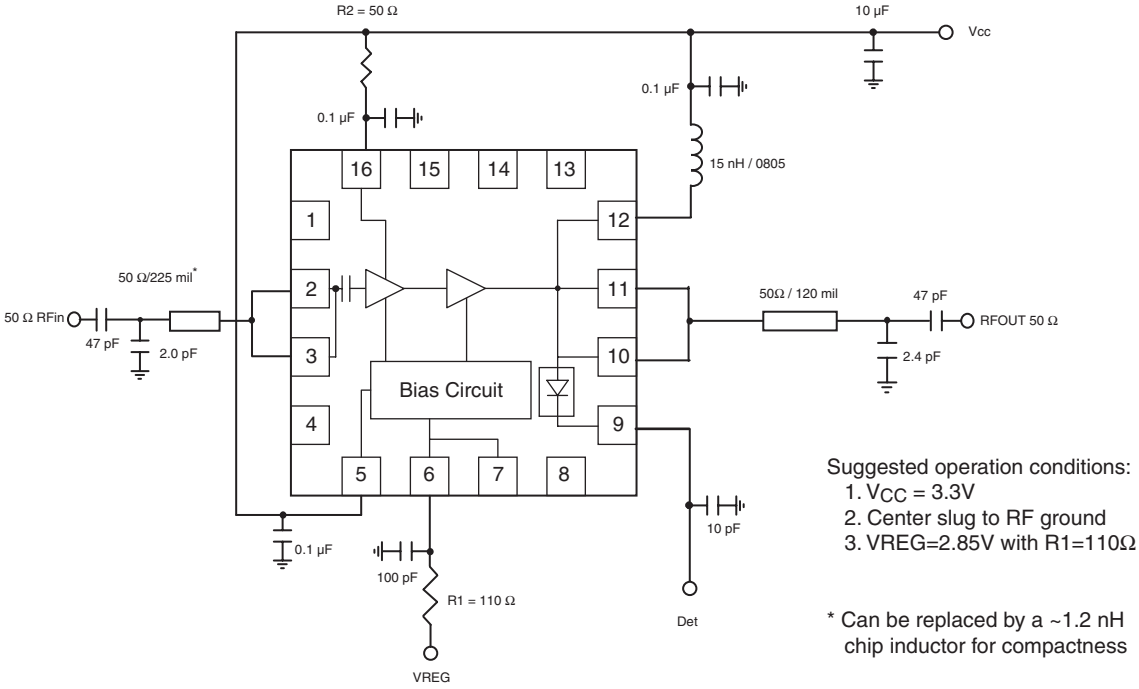
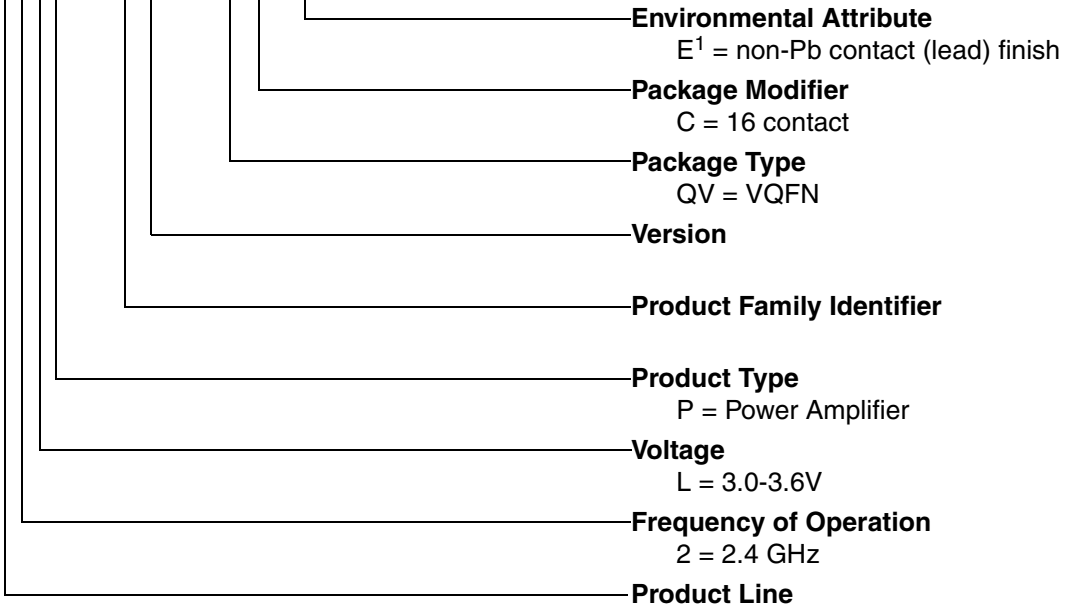


FIGURE 19: Typical Schematic for High-Power/High-Efficiency 802.11b/g Applications

PRODUCT ORDERING INFORMATION

SST12LP 14A - QVC E
SSTXXLP XXX - XXX X



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST12LP14A

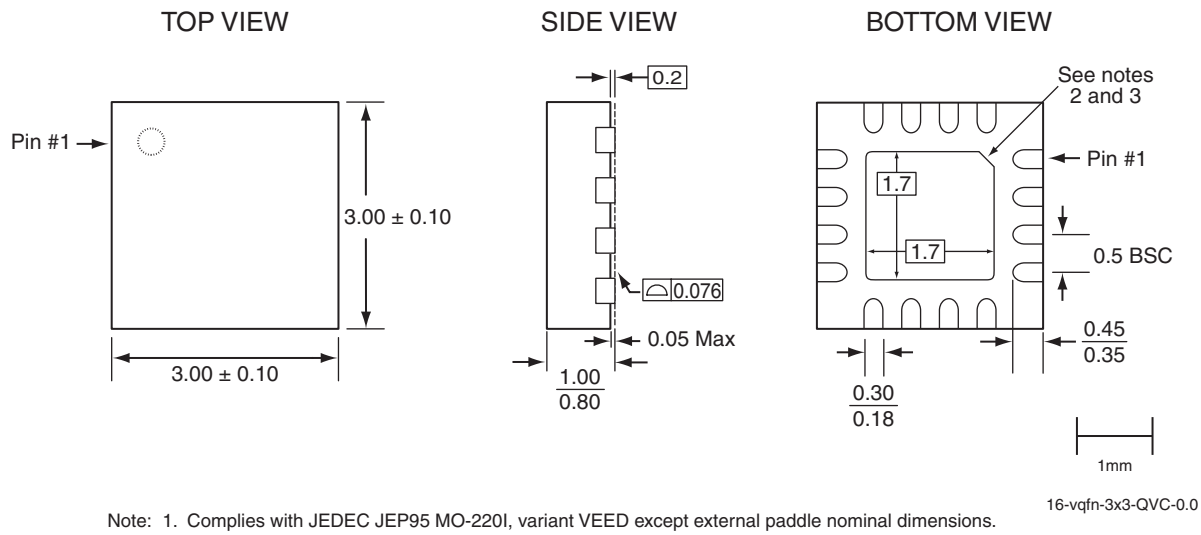
SST12LP14A-QVCE

SST12LP14A Evaluation Kits

SST12LP14A-QVCE-K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC JEP95 MO-220I, variant VEED except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain V_{SS} leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the V_{SS} of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

FIGURE 20: 16-Contact Very-thin Quad Flat No-lead (VQFN)
SST Package Code: QVC

TABLE 4: Revision History

Revision	Description	Date
00	• Initial release of data sheet	Jun 2005
01	• Removed Stability and Ruggedness parms from Table 3 on page 5 • Updated the schematic in Figure 19 on page 15	Sep 2005
02	• Updated the schematic in Figure 19 on page 15 • Updated Figures 4, 5, 6, 7, and 14 • Made minor updates to the “Features:” section • Made minor updates to the “Electrical Specifications” section • Applied new format.	Mar 2006
03	• Updated document status from Preliminary Specification to Data Sheet	Apr 2008
04	• Updated “Contact Information” on page 18.	Feb 2009

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