TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Voltage	V_A		2.7[2]	—	5.5	V
Digital and I/O Supply Voltage	V_D		1.62	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Notes:
1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at V_A = 3.3 V and 25 °C unless otherwise stated.
2. SSOP devices operate down to 2 V at 25 °C. See Section “4.20. 2 V Operation (SSOP Only)” for details.

Table 2. DC Characteristics

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
V_{AQFN} Supply Current	I_{FMVA}	Digital Output Mode[1]	—	8.2	9.5	mA
V_{DQFN} Supply Current	I_{FMVD}		—	10.5	13.5	
V_{ASSOP} Supply Current	I_{FMVA}		—	18.5	21.5	
V_{DSSOP} Supply Current	I_{FMVD}		—	0.15	0.6	
V_{AQFN} Supply Current	I_{FMVA}	Analog Output Mode[2]	—	9.1	10.3	
V_{DQFN} Supply Current	I_{FMVD}		—	9.9	12.8	
V_{ASSOP} Supply Current	I_{FMVA}		—	19.1	21.3	
V_{DSSOP} Supply Current	I_{FMVD}			0.1	0.6	
Powerdown						
V_{AQFN} Powerdown Current	I_{APD}		—	4	15	µA
V_{ASSOP} Powerdown Current			—	9.5	15	
V_{DQFN} Powerdown Current	I_{DPD}	SCLK, RCLK inactive	—	3	10	µA
V_{DSSOP} Powerdown Current		SCLK, RCLK inactive	—	3	10	
High Level Input Voltage[3]	V_{IH}		0.7 x V_D	—	V_D + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_D	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_D = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_D = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_D	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_D	V

Notes:

1. Guaranteed by characterization.
2. Backwards compatible mode to rev B and rev C. Additional features on this device may increase typical supply current.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.

Table 3. Reset Timing Characteristics[1,2,3]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}\uparrow$[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns
$\overline{RST}$ Pulse Release Time Before VDD/VIO Turn Off	t_{RRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.
5. $\overline{RST}$ must be held low for at least 100 µs after all voltage supplies have been ramped up.
6. $\overline{RST}$ needs to be asserted (pulled low) prior to any supply voltage is ramped down.

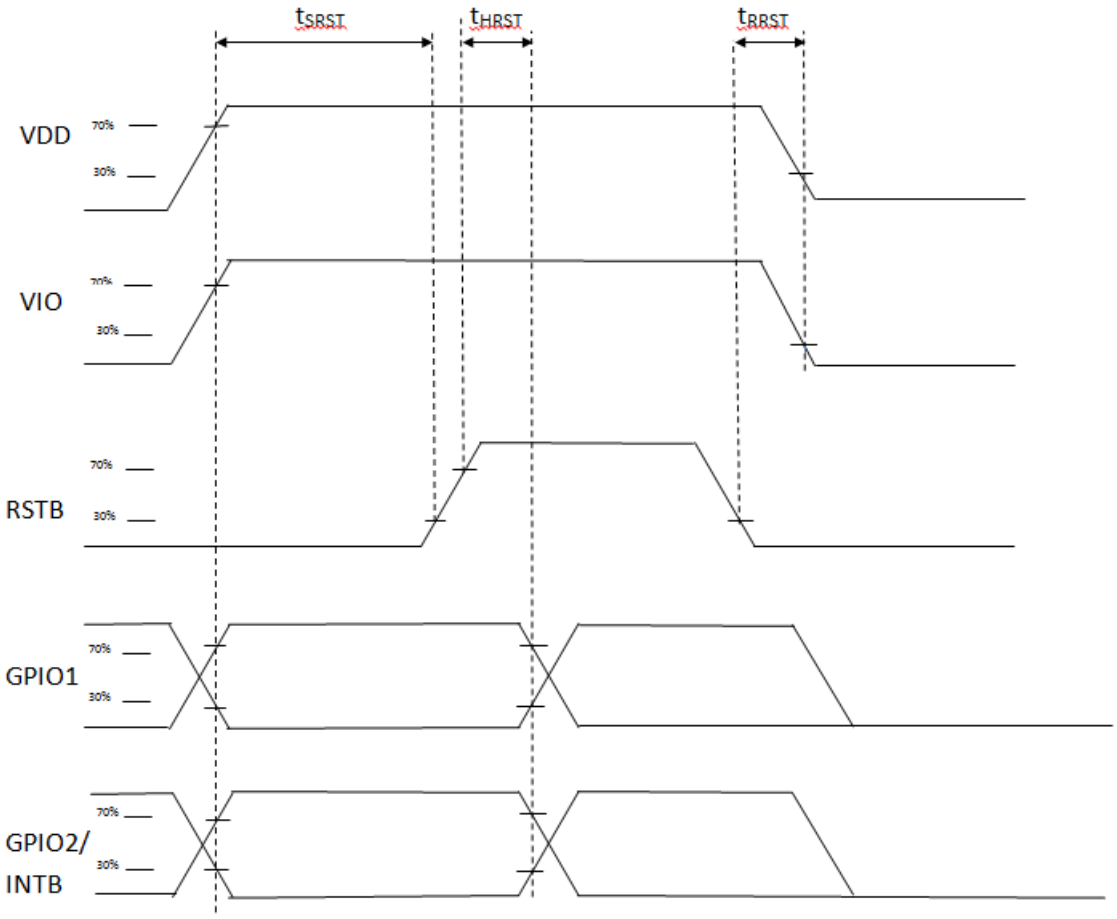


Figure 1. Reset Timing Parameters for Busmode Select

Table 4. 2-Wire Control Interface Characteristics[1,2,3]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_D = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4704/05-D60 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

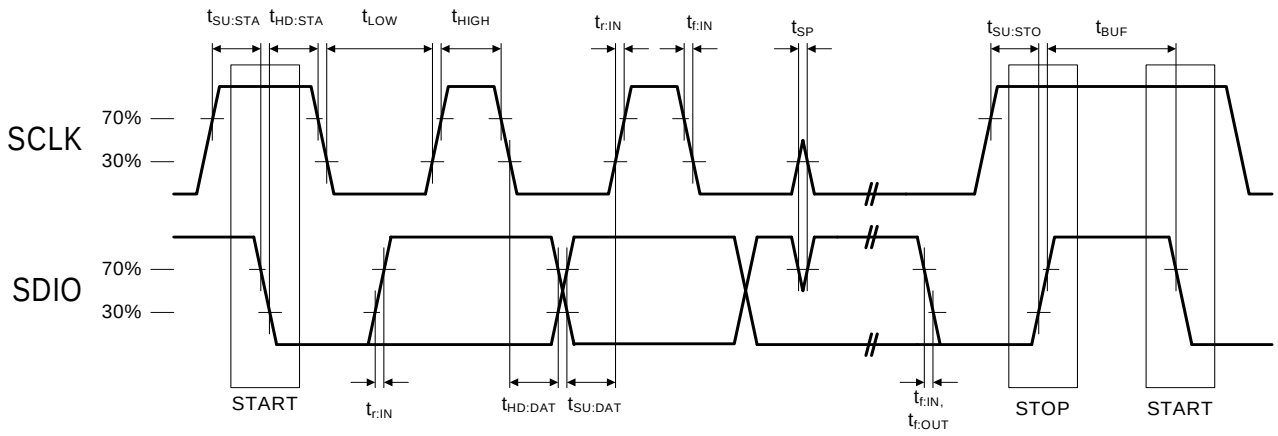


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

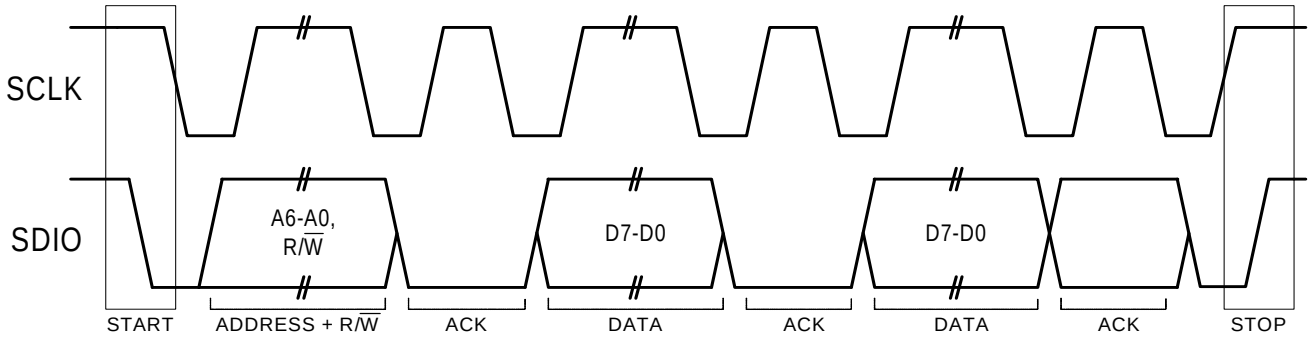


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 5. 3-Wire Control Interface Characteristics
(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

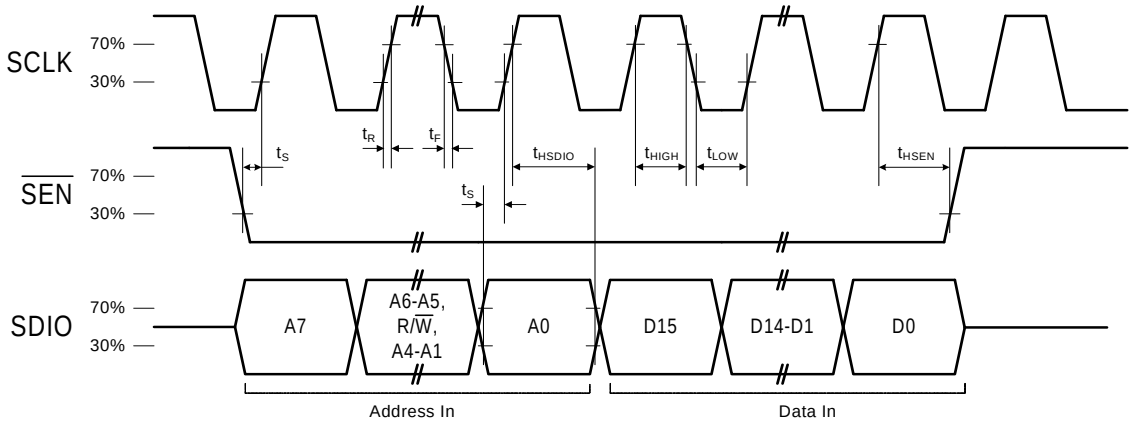


Figure 4. 3-Wire Control Interface Write Timing Parameters

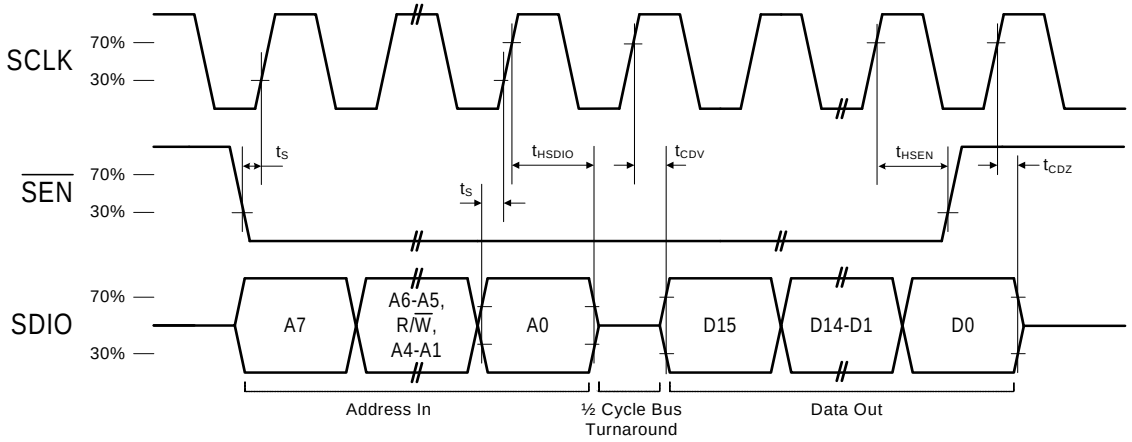


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 6. Digital Audio Interface Characteristics
(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	50	ns

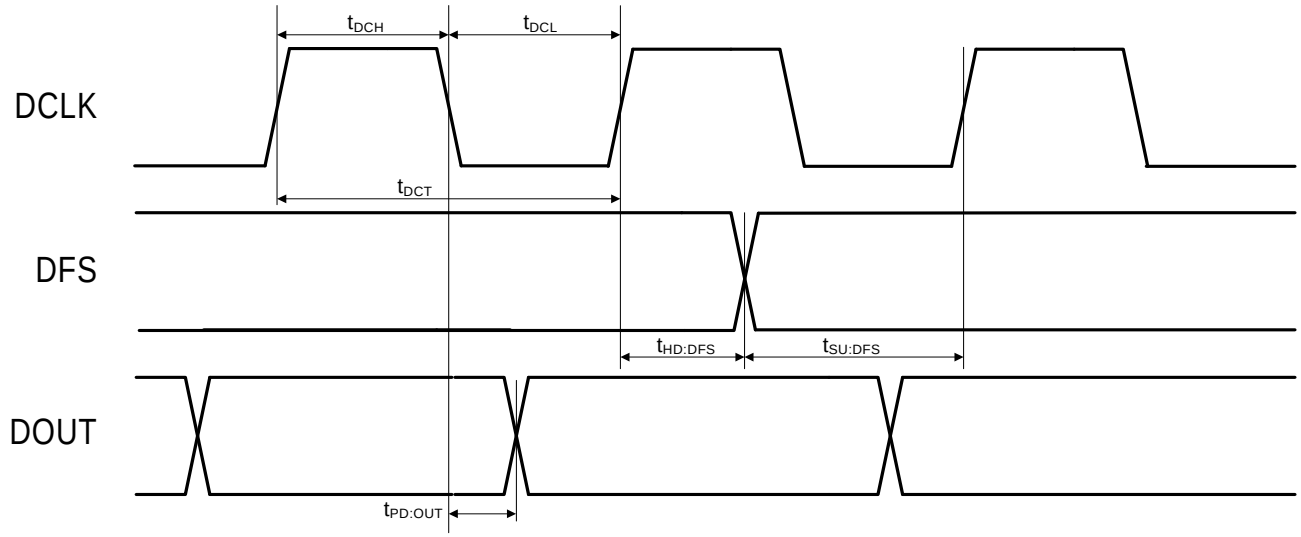


Figure 6. Digital Audio Interface Timing Parameters, I^2S Mode

Table 7. FM Receiver Characteristics[1,2]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity[3,4,5,6]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
RDS Sensitivity[6,7]		Δf = 2 kHz, RDS BLER < 5%	—	10	—	µV EMF
LNA Input Resistance[7,8]			3	4	5	kΩ
LNA Input Capacitance[7,8]			4	5	6	pF
Input IP3[7,9]			100	105	—	dBµV EMF
AM Suppression[3,4,7,8]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[7]		In-band	35	—	—	dB
Audio Output Voltage[3,4,8]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,8,10]			—	—	1	dB
Audio Frequency Response Low[7]		–3 dB	—	—	30	Hz
Audio Frequency Response High[7]		–3 dB	15	—	—	kHz
Audio Stereo Separation[8,10]			35	42	—	dB
Audio Mono S/N[3,4,5,8]			55	63	—	dB
Audio Stereo S/N[4,5,7,8]			—	58	—	dB
Audio THD[3,8,10]			—	0.1	0.5	%
De-emphasis Time Constant[7]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Blocking Sensitivity[3,4,5,6,7,11, 12]		Δf = ±400 kHz	—	34	—	dBµV
		Δf = ±4 MHz	—	30	—	dBµV

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Analog audio output mode.
7. Guaranteed by characterization.
8. V_{EMF} = 1 mV.
9. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled.
10. Δf = 75 kHz.
11. Sensitivity measured at (S+N)/N = 26 dB.
12. Blocker Amplitude = 100 dBµV.
13. At temperature (25 °C).
14. At LOUT and ROUT pins.

Table 7. FM Receiver Characteristics[1,2] (Continued)

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermod Sensitivity[3,4,5,6,7,11,12]		Δf = ±400 kHz, ±800 kHz	—	40	—	dBµV
		Δf = ±4 MHz, ±8 MHz	—	35	—	dBµV
Audio Output Load Resistance[7,14]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[7,14]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[7]		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time[7]		From powerdown	—	—	110	ms
RSSI Offset[13]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Analog audio output mode.
7. Guaranteed by characterization.
8. V_{EMF} = 1 mV.
9. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
10. Δf = 75 kHz.
11. Sensitivity measured at (S+N)/N = 26 dB.
12. Blocker Amplitude = 100 dBµV.
13. At temperature (25 °C).
14. At LOUT and ROUT pins.

Table 8. 64–75.9 MHz Input Frequency FM Receiver Characteristics[1,2,3]

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		64	—	75.9	MHz
Sensitivity[4,5,6,8]		(S+N)/N = 26 dB	—	3.5	—	µV EMF
LNA Input Resistance[3,7]			3	4	5	kΩ
LNA Input Capacitance[3,7]			4	5	6	pF
Input IP3[9]			—	105	—	dBµV EMF
AM Suppression[3,4,5,7]		m = 0.3	—	50	—	dB
Adjacent Channel Selectivity		±200 kHz	—	50	—	dB
Alternate Channel Selectivity		±400 kHz	—	70	—	dB
Audio Output Voltage[4,5,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[4,7,10]			—	—	1	dB
Audio Frequency Response Low[3]		–3 dB	—	—	30	Hz
Audio Frequency Response High[3]		–3 dB	15	—	—	kHz
Audio Mono S/N[4,3,5,7]			—	63	—	dB
Audio THD[4,7,10]			—	0.1	—	%
De-emphasis Time Constant[3]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Output Load Resistance[3,11]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[3,11]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[3]		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time[3]		From powerdown	—	—	110	ms
RSSI Offset[12]		Input levels of 8 and 60 dBµV EMF	–3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. Guaranteed by characterization.
4. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. V_{EMF} = 1 mV.
8. Analog output mode.
9. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled.
10. Δf = 75 kHz.
11. At LOUT and ROUT pins.
12. At temperature (25 °C).

Table 9. Reference Clock and Crystal Characteristics

(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[2]			–100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance[2]			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF
ESR			—	—	50	kΩ
CL[3]			7	12	22	pF
CL–single ended[3]			14	24	44	pF

Notes:

1. The Si473x-D60 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. For more details, see Table 6 of “AN332: Si47xx Programming Guide”.
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.
3. Guaranteed by characterization.

Table 10. Thermal Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	—	80	—	°C/W
Ambient Temperature	T_A	–20	25	85	°C
Junction Temperature	T_J	—	—	92	°C

***Note:** Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.

Table 11. Absolute Maximum Ratings[1,2]

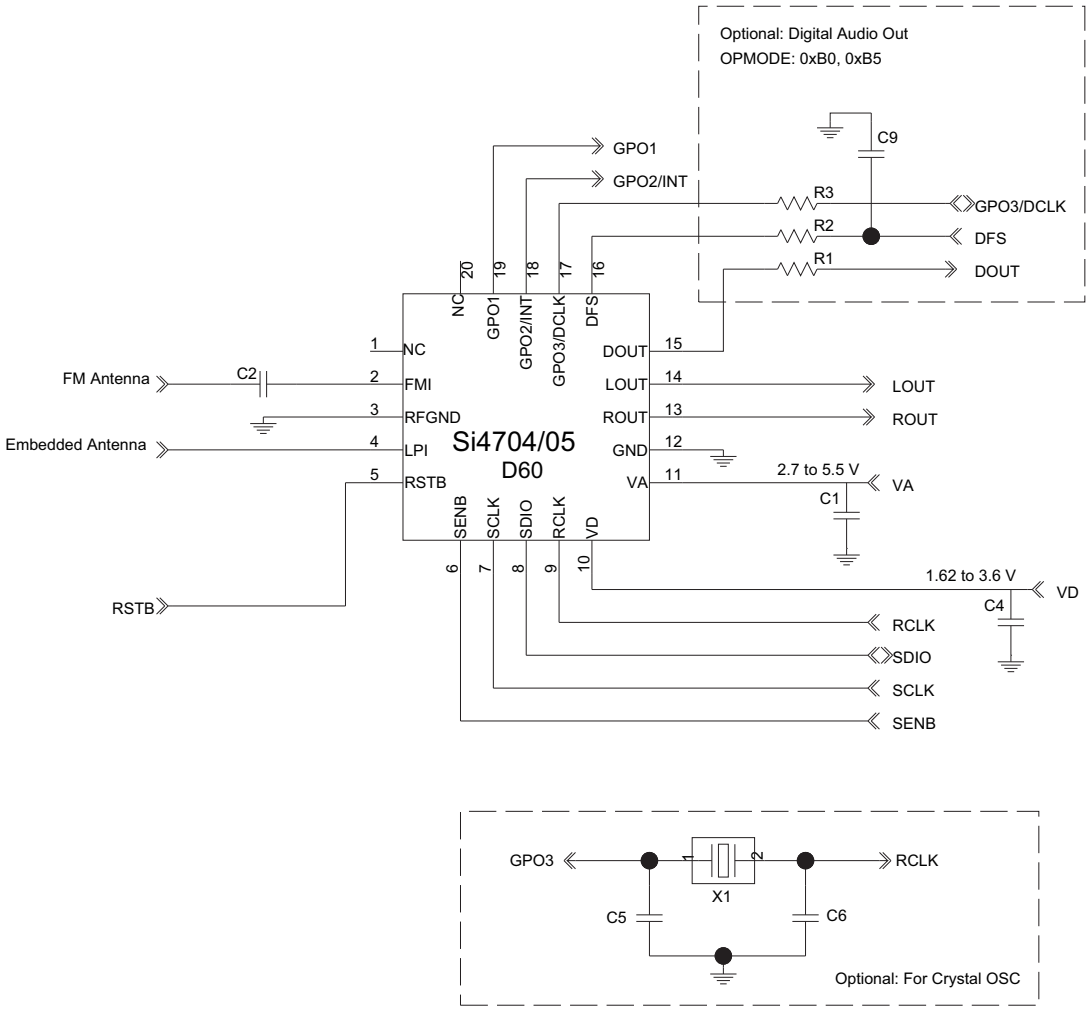
Parameter	Symbol	Value	Unit
Analog Supply Voltage	V_A	–0.5 to 5.8	V
Digital and I/O Supply Voltage	V_D	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pk}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4704/05-D60 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins DFS, SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2, GPO3, and DCLK.
4. At RF input pin FMI and LPI.

2. Typical Application Schematic

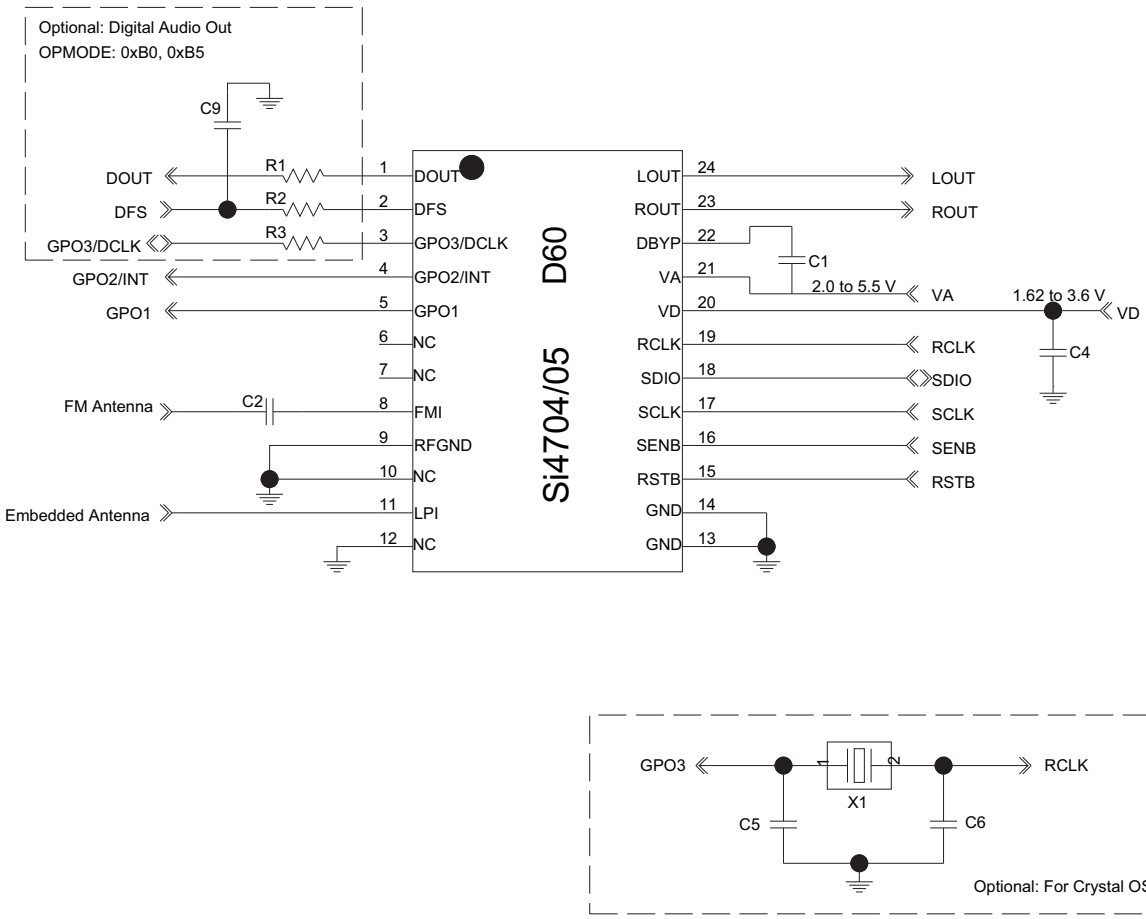
2.1. QFN Typical Application Schematic



Notes:

1. Place C1 close to VA pin and C4 close to VD pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the FM antenna interface.
6. Place Si4704/05-D60 as close as possible to antenna and keep the FMI traces as short as possible.

2.2. SSOP Typical Application Schematic



Notes:

1. Place C1 close to VA and C4 close to VD pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 6 and 7 are no connects, leave floating.
4. Pin 10 is unused. Tie this pin to GND.
5. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
6. Pin 8 connects to the FM antenna interface.
7. Place Si4704/05-D60 as close as possible to antenna and keep the FMI traces as short as possible.

3. QFN/SSOP Bill of Materials

Table 12. Si4704/05-D60 QFN/SSOP Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
C2	Coupling capacitor, 1 nF, ±20%, Z5U/X7R	Murata
C4	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R	Murata
U1	Si4704/05-D60 FM Radio Tuner	Silicon Laboratories
Optional Components		
C5, C6	Crystal load capacitors, 22 pF, ±5%, COG (Optional for crystal oscillator)	Venkel
C9	Noise mitigating capacitor, 2~5 pF (Optional for digital audio)	Murata
R1	Resistor, 600 Ω (Optional for digital audio)	Venkel
R2	Resistor, 2 kΩ (Optional for digital audio)	Venkel
R3	Resistor, 2 kΩ (Optional for digital audio)	Venkel
X1	32.768 kHz crystal (Optional for crystal oscillator)	Epson

4. Functional Description

4.1. Overview

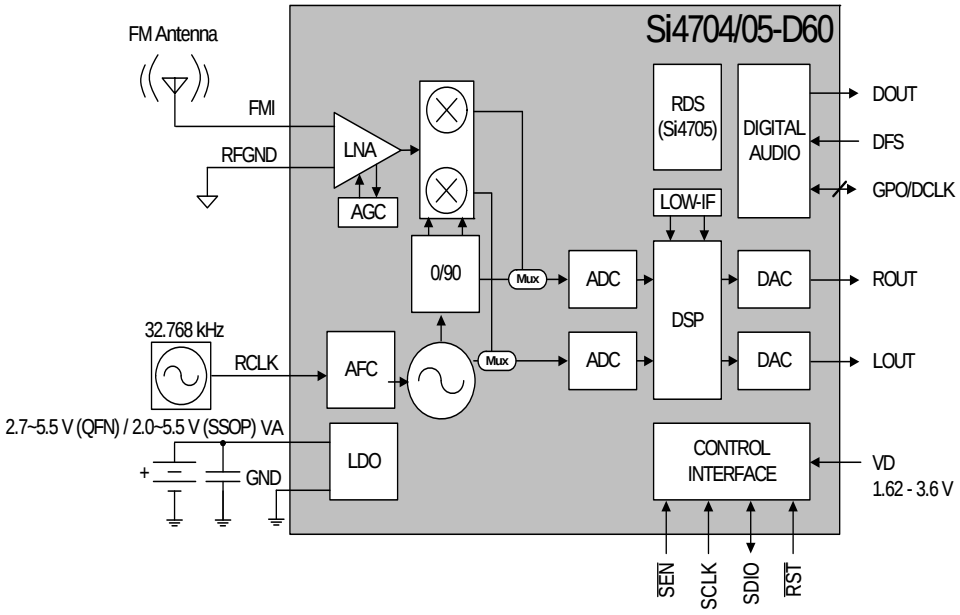


Figure 7. Functional Block Diagram

The Si4704/05-D60 CMOS FM radio receiver IC integrates the complete tuner function from antenna input to audio output. This feature enables a cost-efficient digital audio platform for consumer electronics applications with high TDMA noise immunity, superior radio performance, and high fidelity audio power amplification. Offering unmatched integration and PCB space savings, the Si4704/05-D60 requires only few external components and less than 15 mm^2 of board area, excluding the antenna inputs. The Si4704/05-D60 FM radio provides the space savings and low power consumption necessary for portable devices while delivering the high performance and design simplicity desired for all FM solutions.

Leveraging Silicon Laboratories' proven and patented Si4700/01 FM tuner's digital low intermediate frequency (low-IF) receiver architecture, the Si4704/05-D60 delivers superior RF performance and interference rejection in the FM bands. The high level of integration and complete system production test simplifies design-in, increases system quality, and improves reliability and manufacturability.

The Si4704/05-D60 is a feature-rich solution that includes advanced seek algorithms, soft mute, auto-calibrated digital tuning, FM stereo processing and advanced audio processing.

In addition, the Si4704/05-D60 provides analog and digital audio outputs and a programmable reference clock. The device supports I^2C-compatible 2-wire control interface, and a Si4700/01 backwards-compatible 3-wire control interface.

The Si4704/05-D60 utilizes digital signal processing to achieve high fidelity, optimal performance, and design flexibility. The chip provides excellent pilot rejection, selectivity, and unmatched audio performance, and offers both the manufacturer and the end-user extensive programmability and a better listening experience.

The Si4705-D60 incorporates a digital signal processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions. Using this feature, the Si4705-D60 enables broadcast data such as station identification and song name to be displayed to the user.

4.2. Operating Modes

The Si4704/05-D60 operates in FM receive mode. In FM mode, radio signals are received on FMI and processed by the FM front-end circuitry. In addition to the receiver mode, there is a clocking mode to choose to clock the Si4704/05-D60 from a reference clock or crystal. On the Si4704/05-D60, there is an audio output mode to choose between an analog and/or digital audio output. In the analog audio output mode, ROUT and LOUT are used for the audio output pins. In the digital audio mode, DOUT, DFS, and DCLK pins are used. Concurrent analog/digital audio output mode is also available requiring all five pins.

4.3. FM Receiver

The Si4704/05-D60 FM receiver is based on the proven Si4700/01 FM tuner. The receiver uses a digital low-IF architecture allowing the elimination of external components and factory adjustments. The Si4704/05-D60 integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (64 to 108 MHz). An AGC circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the Si4704/05-D60 to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

4.4. Digital Audio Interface

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4704/05-D60 supports a number of industry-standard sampling rates including 32, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

4.4.1. Audio Data Formats

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In left-justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties. The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.4.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

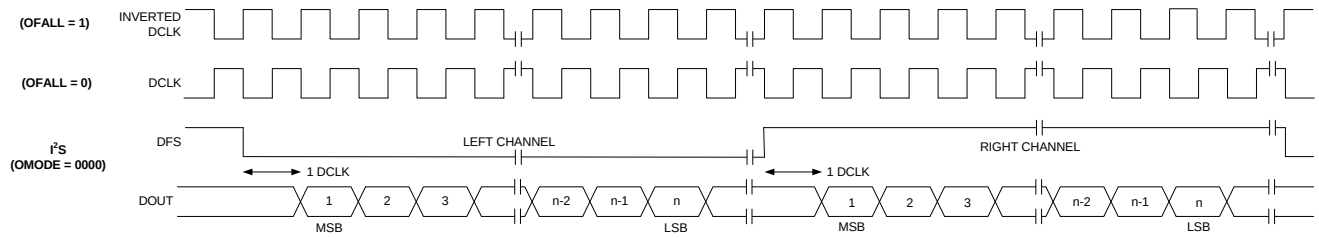


Figure 8. I²S Digital Audio Format

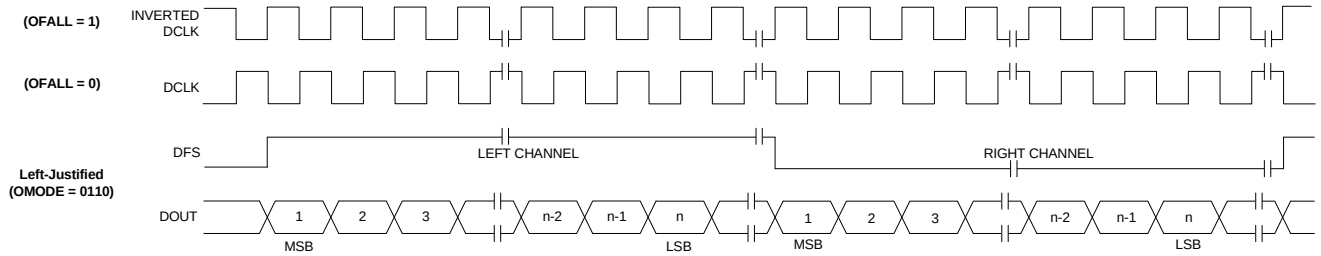


Figure 9. Left-Justified Digital Audio Format

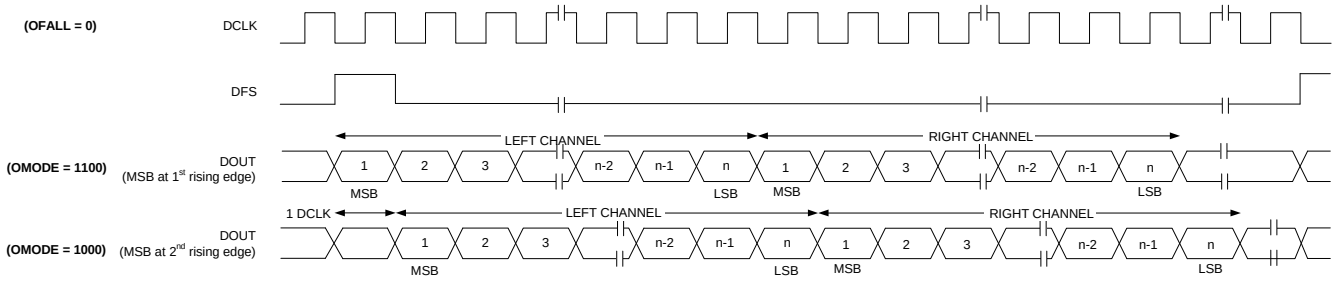


Figure 10. DSP Digital Audio Format

4.5. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 11 below.

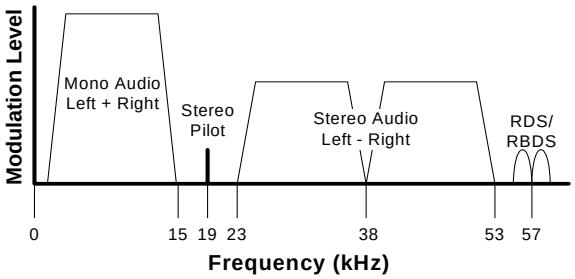


Figure 11. MPX Signal Spectrum

4.5.1. Stereo Decoder

The Si4704/05-D60's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

4.5.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Three metrics, received signal strength indicator (RSSI), signal-to-noise ratio (SNR), and multipath interference, are monitored simultaneously in forcing a blend from stereo to mono. The metric which reflects the minimum signal quality takes precedence and the signal is blended appropriately.

All three metrics have programmable stereo/mono thresholds and attack/release rates. If a metric falls below its mono threshold, the signal is blended from stereo to full mono. If all metrics are above their respective stereo thresholds, then no action is taken to blend the signal. If a metric falls between its mono and stereo thresholds, then the signal is blended to the level proportional to the metric's value between its mono and stereo thresholds, with an associated attack and release rate.

4.6. Received Signal Qualifiers

The quality of a tuned signal can vary depending on many factors including environmental conditions, time of day, and position of the antenna. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si4704/05-D60 monitors and provides indicators of the signal quality, allowing the host processor to perform additional processing if required by the customer. The Si4704/05-D60 monitors signal quality metrics including RSSI, SNR, and multipath interference on FM signals. These metrics are used to optimize signal processing and are also reported to the host processor. The signal processing algorithms can use either Silicon Labs' optimized settings (recommended) or be customized to modify performance.

4.7. Volume Control

The audio output may be muted. Volume is adjusted digitally by the RX_VOLUME property.

4.8. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted.

4.9. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The soft mute feature is triggered by the SNR metric. The SNR threshold for activating soft mute is programmable, as are soft mute attenuation levels and attack and release rates.

4.10. FM Hi-Cut Control

Hi-cut control is employed on audio outputs with degradation of the signal due to low SNR and/or multipath interference. Two metrics, SNR and multipath interference, are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for both metrics. The transition frequency for hi-cut is also programmable with up to seven hi-cut filter settings. A single set of attack and release rates for hi-cut are programmable for both metrics from a range of 2 ms to 64 s. The level of hi-cut applied can be monitored with the FM_RSQ_STATUS command. Hi-cut can be disabled by setting the hi-cut filter to audio bandwidth of 15 kHz.

4.11. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4704/05-D60 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

4.12. RDS/RBDS Processor (Si4705-D60 Only)

The Si4705-D60 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4705-D60 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4705-D60 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors or that the block checkword contains errors. The pilot does not have to be present to decode RDS/RBDS.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

4.13. Tuning

The tuning frequency is directly programmed using the FM_TUNE_FREQ command. The Si4704/05-D60 supports channel spacing steps of 10 kHz in FM mode.

4.14. Seek

The Si4704/05-D60 seek functionality is performed completely on-chip and will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds. The seek function can be made to stop at the band edge and provide an interrupt, or wrap the band and continue seeking until arriving at the original departure frequency. The device sets interrupts with found valid stations or, if the seek results in zero found valid stations, the device indicates failure and again sets an interrupt. Refer to “AN332: Si47xx Programming Guide”.

The Si4704/05-D60 uses RSSI, SNR, and AFC to qualify stations. Most of these variables have programmable thresholds for modifying the seek function according to customer needs.

RSSI is employed first to screen all possible candidate stations. SNR and AFC are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations. The Si4704/05-D60 defaults set RSSI to a mid-level threshold and add an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations while keeping the seek time to acceptable levels. Generally, the time to auto-scan and store valid channels for an entire FM band with all thresholds engaged is very short depending on the band content. Seek is initiated using the FM_SEEK_START command. The RSSI, SNR, and AFC threshold settings are adjustable using properties.

4.15. Reference Clock

The Si4704/05-D60 reference clock is programmable, supporting RCLK frequencies listed in Table 9, “Reference Clock and Crystal Characteristics,” on page 15. Refer to Table 2, “DC Characteristics,” on page 6 for switching voltage levels and Table 9 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic" on page 17. This mode is enabled using the POWER_UP command. Refer to “AN332: Si47xx Programming Guide”.

The Si4704/05-D60 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4704/05-D60 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4704/05-D60 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

4.16. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4704/05-D60 and receive responses from the device. The serial port can operate in two bus modes: 2-wire mode and 3-wire mode. The Si4704/05-D60 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor, which is connected while RST is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while RST is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 13.

Table 13. Bus Mode Select on Rising Edge of RST

Bus Mode	GPO1	GPO2
2-Wire	1	0
3-Wire	0 (must drive)	0

After the rising edge of RST, the pins GPO1 and GPO2 are used as general purpose output (O) pins, as described in Section “4.17. GPO Outputs”. In any bus mode, commands may only be sent after VD and VA supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.16.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4704/05-D60 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4704/05-D60 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). Refer to “AN332: Si47xx Programming Guide”

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4704/05-D60 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4704/05-D60 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4704/05-D60.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 4, “2-Wire Control Interface Characteristics” on page 8; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 9, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 9.

4.16.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 9-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4704/05-D60 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 5, “3-Wire Control Interface Characteristics,” on page 10, Figure 4, and Figure 5.

4.17. GPO Outputs

The Si4704/05-D60 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-impedance. The GPO pins can be reconfigured as specialized functions.

4.18. Firmware Upgrades

The Si4704/05-D60 contains on-chip program RAM to accommodate minor changes to the firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new radio designs and those already deployed in the field.

4.19. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

The Si4704/05-D60 contains an on-board non-volatile memory for storing its operational firmware. Proper timing as specified in this data sheet, particularly with respect to keeping RST pin low during any power supply transitions, must be honored to avoid the risk of corrupting the contents of this memory, which can render the device permanently non-functional.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

4.20. 2 V Operation (SSOP Only)

The Si4704/05-D60 is capable of operating down to 2 V as the battery drains in an application. Any power-up or reset is not guaranteed to work below the dc characteristics defined in Table 2. This capability enables a much longer run time in battery operated devices.

4.21. Programming with Commands

To ease development time and offer maximum customization, the Si4704/05-D60 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control an action such as powerup the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command.

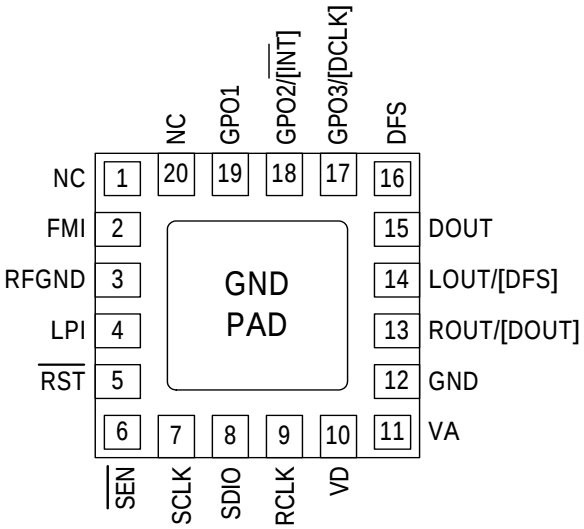
Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a 1-byte status update, indicating interrupt and clear-to-send status information.

For a detailed description of the commands and properties for the Si4704/05-D60, see “AN332: Si47xx Programming Guide.”

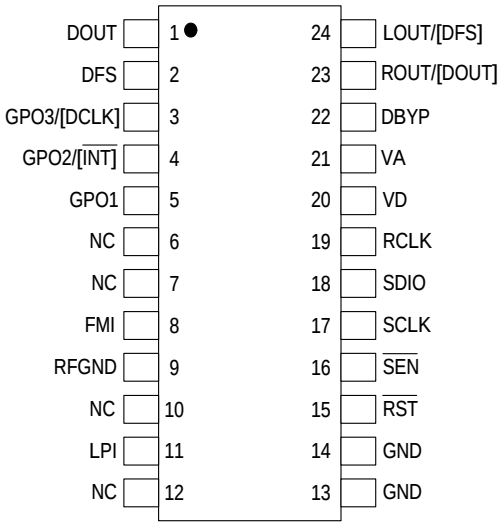
5. Pin Descriptions

5.1. Si4704/05-D60-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM RF inputs. FMI should be connected to the antenna trace.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	LPI	Embedded antenna input.
5	$\overline{\text{RST}}$	Device reset input (active low).
6	$\overline{\text{SEN}}$	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	V_D	Digital and I/O supply voltage.
11	V_A	Analog supply voltage. May be connected directly to battery.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.
13	ROUT/[DOUT]	Right audio line output for analog output mode.
14	LOUT/[DFS]	Left audio line output for analog output mode.
15	DOUT	Digital output data for digital output mode.
16	DFS	Digital frame synchronization input for digital output mode.
17	GPO3/[DCLK]	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
18	GPO2/[$\overline{\text{INT}}$]	General purpose output or interrupt pin.
19	GPO1	General purpose output.

5.2. Si4704/05-D60-GU



Pin Number(s)	Name	Description
1	DOUT	Digital output data for digital output mode.
2	DFS	Digital frame synchronization input for digital output mode.
3	GPO3/[DCLK]	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
4	GPO2/[$\overline{\text{INT}}$]	General purpose output or interrupt pin.
5	GPO1	General purpose output.
6,7	NC	No connect. Leave floating.
8	FMI	FM RF inputs. FMI should be connected to the antenna trace.
9	RFGND	RF ground. Connect to ground plane on PCB.
10	NC	Unused. Tie these pins to GND.
11	LPI	Embedded antenna input.
12	NC	Unused. Tie these pins to GND.
13,14	GND	Ground. Connect to ground plane on PCB.
15	$\overline{\text{RST}}$	Device reset input (active low).
16	$\overline{\text{SEN}}$	Serial enable input (active low).
17	SCLK	Serial clock input.
18	SDIO	Serial data input/output.
19	RCLK	External reference oscillator input.
20	V_D	Digital and I/O supply voltage.
21	V_A	Analog supply voltage. May be connected directly to battery.
22	DBYP	Bypass capacitor.
23	ROUT/[DOUT]	Right audio line output in analog output mode.
24	LOUT/[DFS]	Left audio line output in analog output mode.

6. Ordering Guide

Part Number[1]	Description	Package Type	Operating Temperature/Voltage
Si4704-D60-GM	FM Broadcast Radio Receiver	QFN Pb-free	–20 to 85 °C 2.7 to 5.5 V
Si4704-D60-GU[2]		SSOP Pb-free	
Si4705-D60-GM	FM Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	–20 to 85 °C 2.7 to 5.5 V
Si4705-D60-GU[2]		SSOP Pb-free	

Notes:
1. Add an "(R)" at the end of the device part number to denote tape and reel option.
2. SSOP devices operate down to V_A = 2 V at 25 °C.

7. Package Outline

7.1. Si4704/05-D60 QFN

Figure 12 illustrates the package details for the Si4704/05-D60. Table 14 lists the values for the dimensions shown in the illustration.

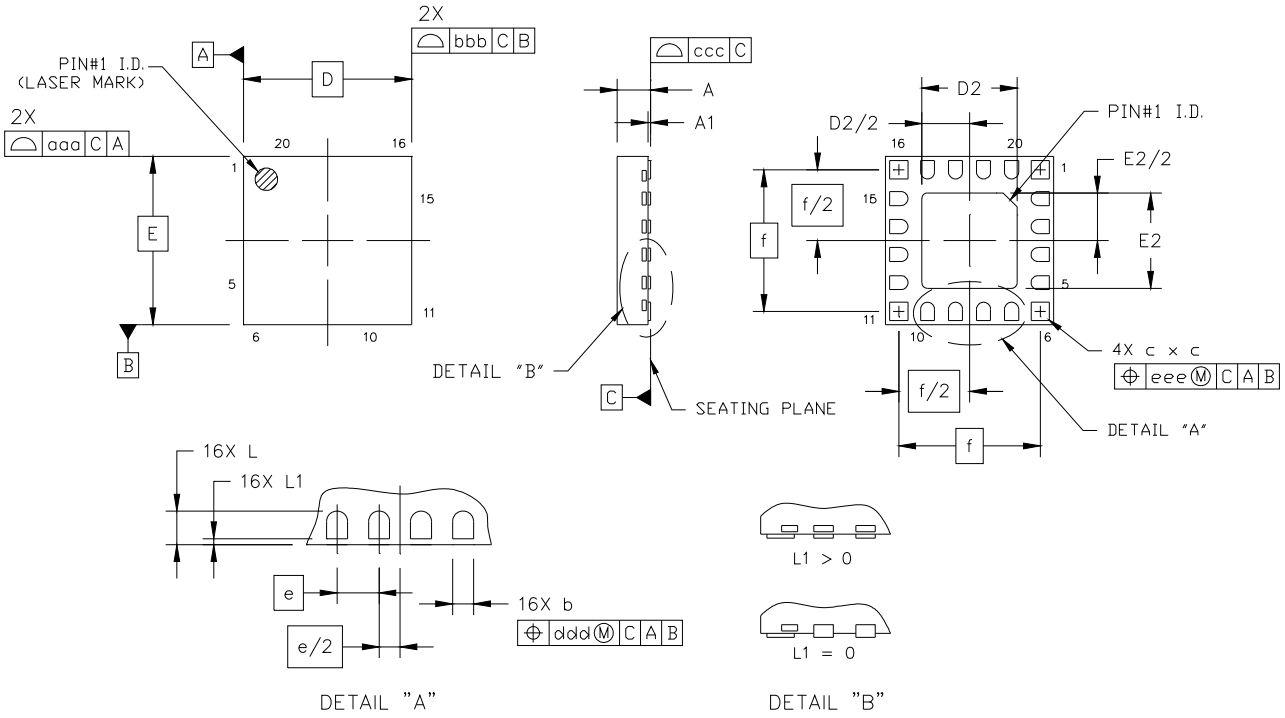


Figure 12. 20-Pin Quad Flat No-Lead (QFN)

Table 14. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:
1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

7.2. Si4704/05-D60 SSOP

Figure 13 illustrates the package details for the Si4704/05-D60. Table 15 lists the values for the dimensions shown in the illustration.

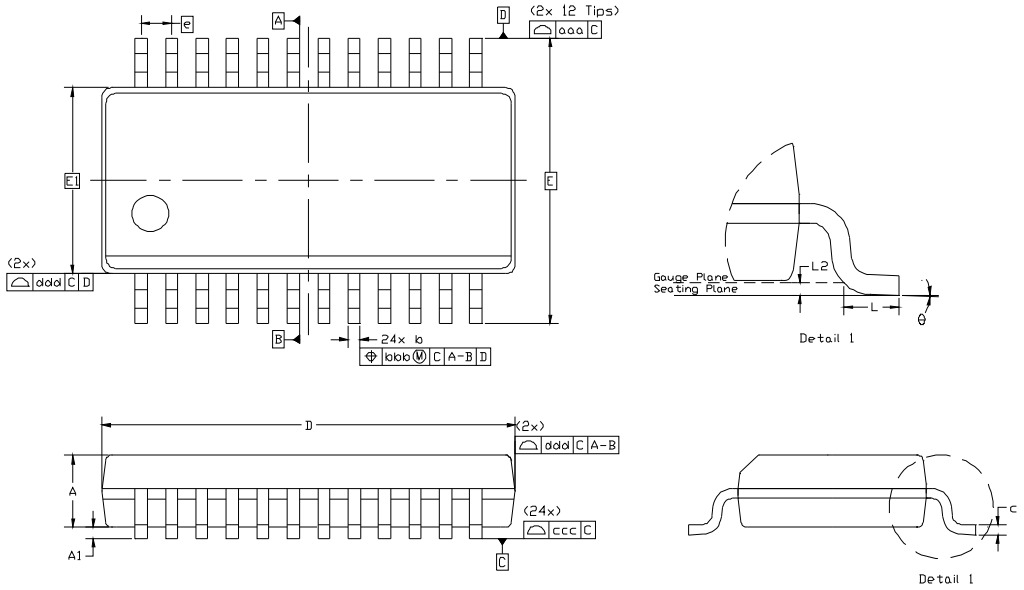


Figure 13. 24-Pin SSOP

Table 15. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.20		
bbb	0.18		
ccc	0.10		
ddd	0.10		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

8.1. Si4704/05-D60 QFN

Figure 14 illustrates the PCB land pattern details for the Si4704/05-D60-GM QFN. Table 16 lists the values for the dimensions shown in the illustration.

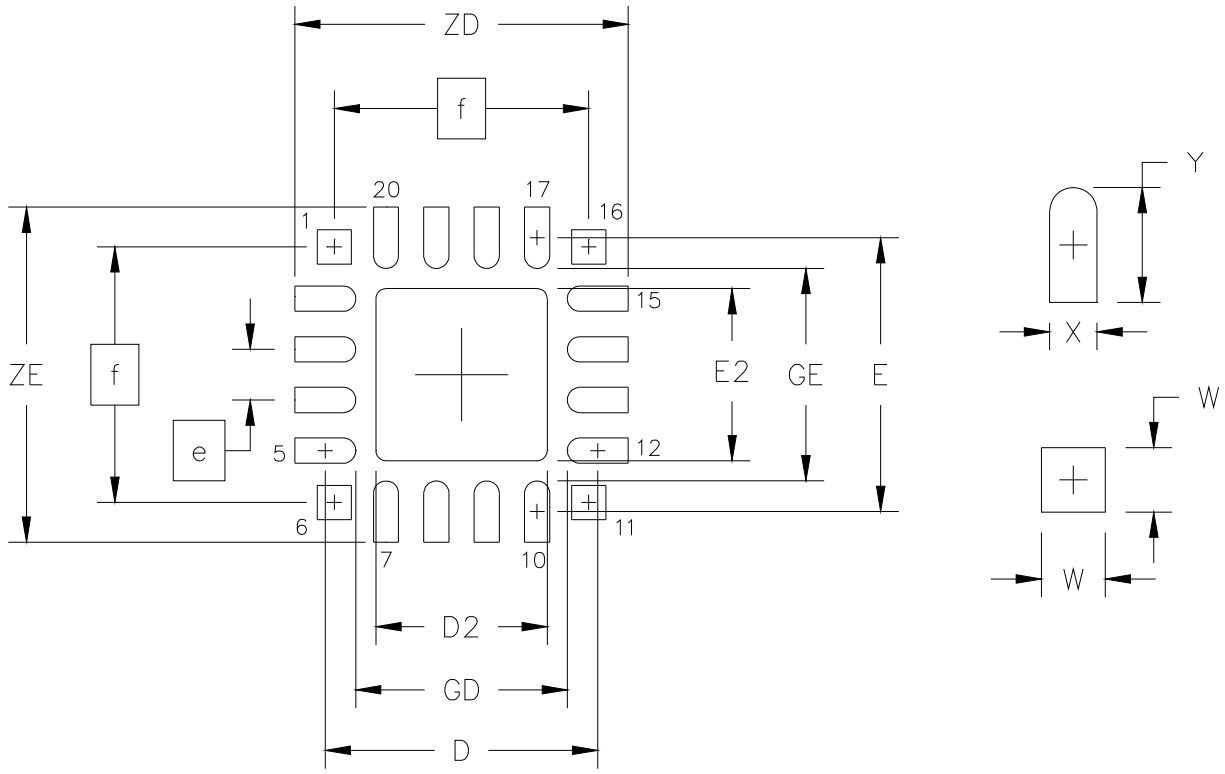


Figure 14. PCB Land Pattern

Table 16. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2. Si4704/05-D60 SSOP

Figure 15 illustrates the PCB land pattern details for the Si4704/05-D60-GU SSOP. Table 17 lists the values for the dimensions shown in the illustration.

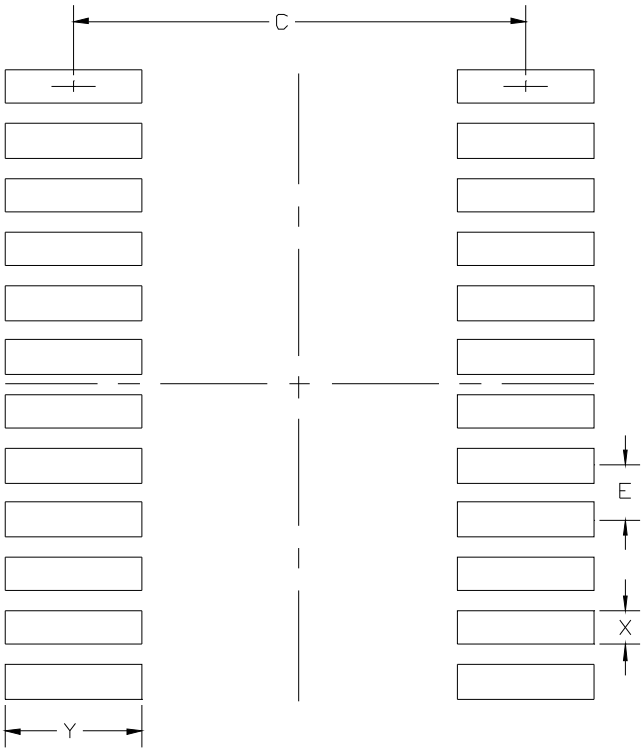


Figure 15. PCB Land Pattern

Table 17. PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y1	1.50	1.60

General:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

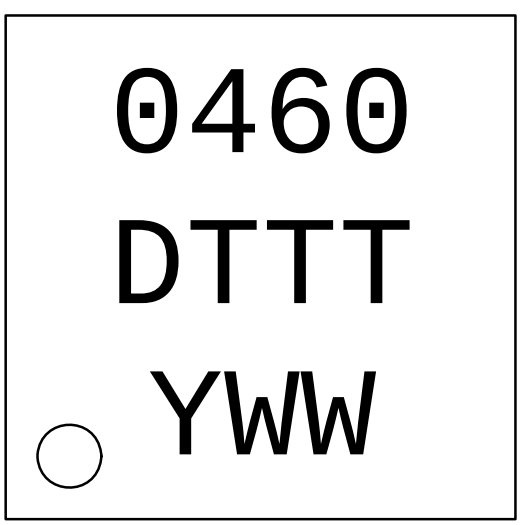
Solder Mask Design:
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

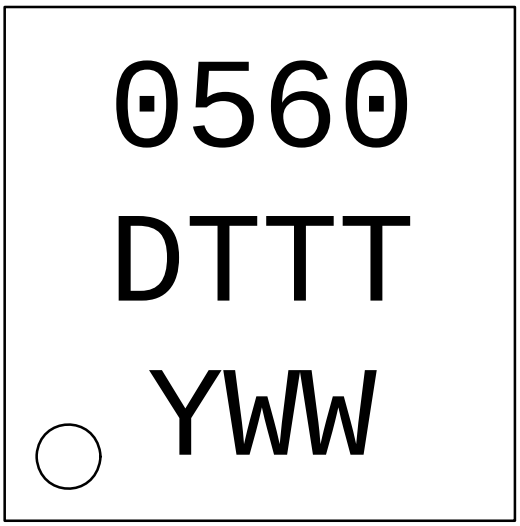
Stencil Design:
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly:
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Markings

9.1. Si4704/05-D60 Top Marking (QFN)

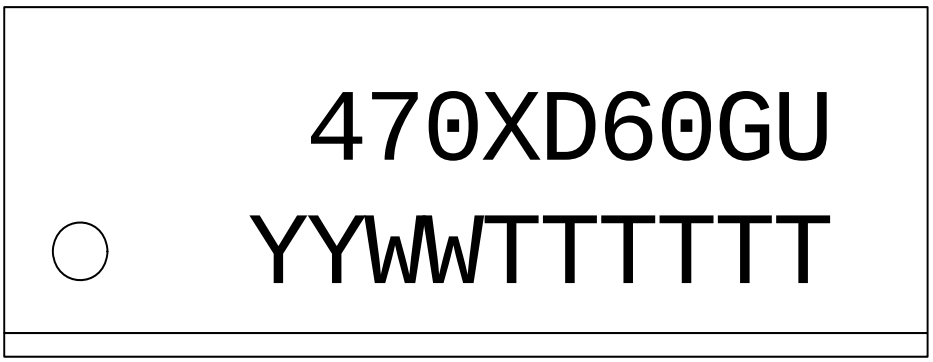




9.2. Top Marking Explanation (QFN)

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	04 = Si4704, 05 = Si4705-D60.
	Firmware Revision	60 = Firmware Revision 6.0.
Line 2 Marking:	Die Revision	D = Revision D Die.
	TTT = Internal Code	Internal tracking code.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier.
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and work week of the mold date.

9.3. Si4704/05-D60 Top Marking (SSOP)



9.4. Top Marking Explanation (SSOP)

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	4704 = Si4704; 4705 = Si4705-D60.
	Die Revision	D = Revision D die.
	Firmware Revision	60 = Firmware Revision 6.0.
	Package Type	GU = 24-pin SSOP Pb-free package
Line 2 Marking:	YY = Year WW = Work week TTTTTT = Manufacturing code	Assigned by the Assembly House.

10. Additional Reference Resources

Contact your local sales representatives for more information or to obtain copies of the following references:

- EN55020 Compliance Test Certificate
- AN332: Si47xx Programming Guide
- AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines
- AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure
- Si47xx EVB User's Guide
- Customer Support Site: www.silabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for complete access. Please visit the Silicon Labs Technical Support web page: https://www.silabs.com/support/pages/contacttechnicalsupport.aspx and register to submit a technical support request.

Document Change List:

Revision 0.4 to Revision 1.0

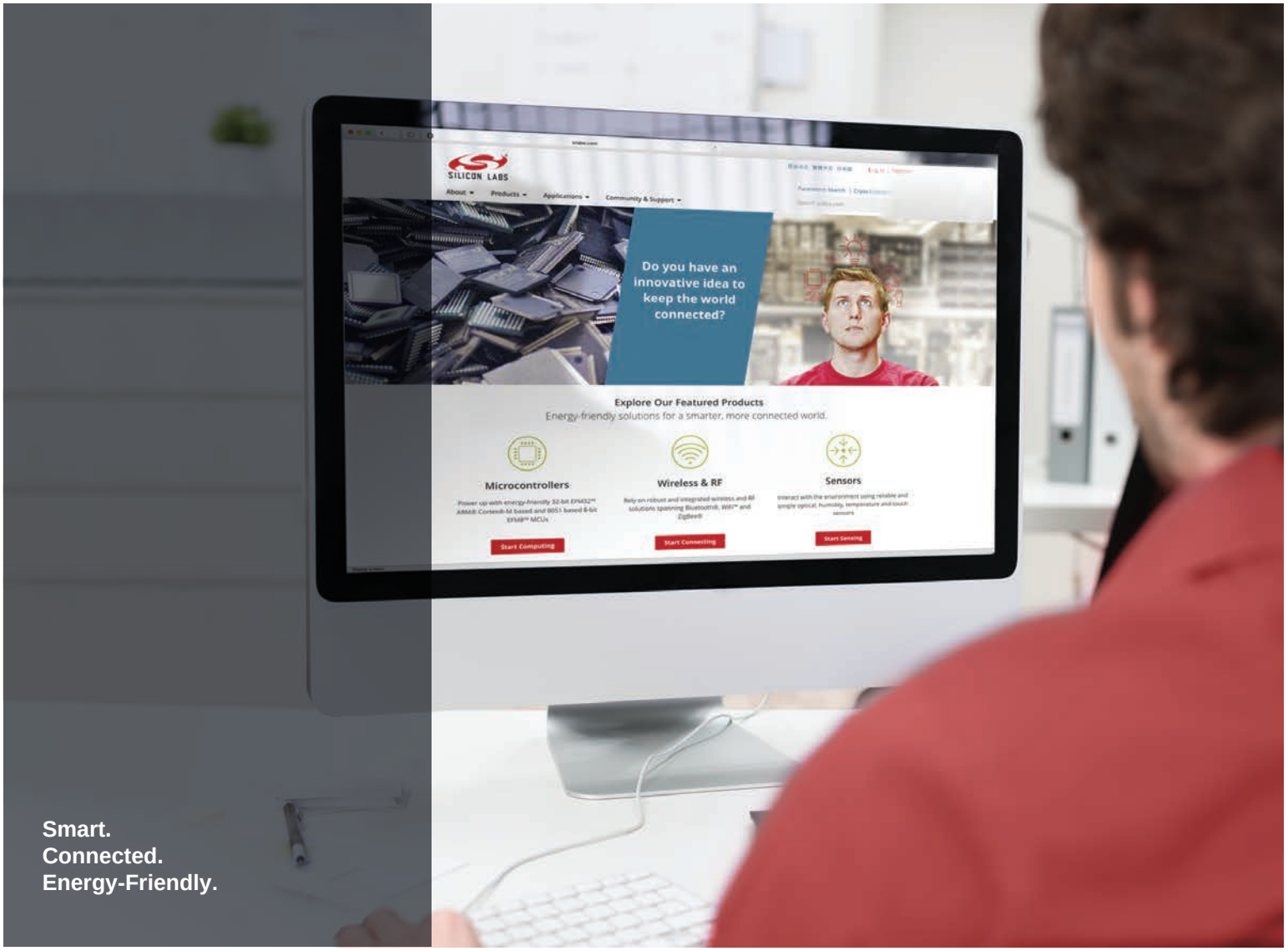
- Updated application schematic.
- Updated pin descriptions.

Revision 1.0 to Revision 1.1

- Updated front page pin assignments.
- Updated Table 6, “Digital Audio Interface Characteristics,” on page 11.
- Updated Table 9, “Reference Clock and Crystal Characteristics,” on page 15.
- Added Table 10, “Thermal Conditions,” on page 15.
- Updated Section "5. Pin Descriptions" on page 27.
- Updated Section "5.1. Si4704/05-D60-GM" on page 27.
- Updated Section "5.2. Si4704/05-D60-GU" on page 28.

Revision 1.1 to Revision 1.2

- Deleted the AUXIN feature.
- Updated Table 3, “Reset Timing Characteristics.”
- Updated Table 10, “Thermal Conditions.”
- Updated Section 4.19, “Reset, Powerup, and Powerdown.”



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com