TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)			
		B2	B3	B4	B6
PIC32MX440F256H	0x0952053	0x3	0x4	0x5	0x5
PIC32MX440F512H	0x0956053				
PIC32MX440F128H	0x094D053				
PIC32MX420F032H	0x0942053				

Note 1: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				B2	B3	B4	B6
Device Reset	$\overline{\text{MCLR}}$	1.	A Reset ($\overline{\text{MCLR}}$) Pulse that is shorter than 2 SYSCLK will not reset the device properly.	X	X	X	X
Device Reset	—	2.	All Resets, except Power-on Reset (POR), can cause a Fail-Safe Clock Monitor event (if enabled) when the duration of the Reset pulse exceeds the clock period of the internal fail-safe clock reference clock (31 kHz).	X	X	X	X
Device Reset	Software Reset	3.	Attempting to perform a software device Reset with PBDIV set to 1:1, and SYSCLK less than 1 MHz will not reset the device properly.	X	X	X	X
External Voltage Regulator	—	4.	A VDDCORE voltage less than 1.75V will cause the CPU to reset when using an external core voltage supply.	X	X	X	X
ADC	Gain and Offset Errors	5.	When running the Analog-to-Digital Converter (ADC) module in Internal Reference mode, the gain error is 3-4 LSb and the offset error is 1-2 LSb across voltage and speed.	X	X	X	X
Bus Matrix	Configuration	6.	The BMXDUDBA, BMXDUPBA and BMXPUPBA registers can be set to values that are outside the device's actual memory size limit.	X	X	X	X
Oscillator	Clock Fail Detect	7.	After a clock failure event, any write to the OSCCON register erroneously clears the fail-safe condition and attempts to switch to a new clock source that is specified by the NOSC bits in the OSCCON register.	X	X	X	X
DMA	Pattern Match Mode	8.	In Pattern Match mode, the DMA will generate up to three additional byte writes to the destination address, after the Pattern Detection event has occurred, when performing transfers with the DCHxSSIZ set to greater than 1.	X	X	X	X
Output Compare	PWM Mode	9.	The Output Compare module in PWM mode outputs a high of period register (PRx) length when attempting to use PWM values of 0x00 followed by 0x01.	X	X	X	X
PMP	Slave Mode	10.	In PMP Slave 4B Buffer mode, if the underflow Status bit OBF (PMSTAT<6>) is cleared at the same time a PMP read is attempted, the PMP could receive incorrect data.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				B2	B3	B4	B6
I/O PORTs	—	11.	When using the hardware assisted read-modify-write registers, PORTxINV, PORTxSET and PORTxCLR, the source used for the operation is the LATx register, not the PORTx register.	X	X	X	X
Timers	—	12.	The TMRx register stays at zero for two timer clock cycles when the PRx register is 0x0000.	X	X	X	X
Timers	—	13.	The timer prescaler may not be reset correctly when it is used with a slow external clock.	X	X	X	X
Timers	Asynchronous Mode	14.	The Timer1 prescaler may not be reset correctly when it is used with a slow external clock.	X	X	X	X
UART	Hardware Handshake Mode	15.	The CTS pin does not deassert until at least 2 bytes are free in the UART FIFO.	X	X	X	X
Watchdog Timer (WDT)	—	16.	An incorrect WDT Time-out Reset may occur.	X	X	X	X
DMA	Channel Abort	17.	DMA channel abort on a channel that is not currently active may have unintended effects on other active channels.	X	X	X	X
Oscillator	Operating Condition	18.	The Primary Oscillator Circuit (POSC), when using XT, XTPLL, HS and HSPLL modes, does not operate over the voltage and temperature range that is listed as item D5 in the device data sheet.	X	X	X	X
PMP	Wait States	19.	The WAITE field in PMMODE<1:0> does not add a Wait state to PMP master reads when it is programmed to the value '01'.	X	X	X	X
UART	Baud Rate Generator	20.	Using BRG values of 0, 1 or 2 cause the Start bit to be shortened.	X	X	X	X
Input Capture	16-bit Mode with DMA	21.	16-bit DMA transfers from the ICAP module FIFO buffer do not advance the ICAP FIFO pointer.	X	X	X	X
USB	Speed Switch	22.	The USB module does not correctly switch from full-speed to low-speed after sending a PRE packet to a hub.	X	X	X	X
DMA	Breakpoints	23.	The DMA buffer may be erroneously filled with the last data read prior to the breakpoint.	X	X	X	X
PMP	DMA Read	24.	Events can be missed if the PMDIN register is used as the DMA source or destination and the PMP IRQ is used as the DMA trigger.	X	X	X	X
Input Capture	—	25.	When in 16-bit mode, the upper 16 bits of the 32-bit ICxBUF register contain Timer3 values.	X	X	X	X
ICSP™	Programming	26.	When programming the PIC32 using the 2-wire PGC and PGD pins, programming data appears as an output on the JTAG TDO pin.	X	X	X	X
UART	High-Speed Mode	27.	In BRGH = 1 mode, the received data is not sampled in the middle of the bit.	X	X	X	X
Oscillator	Clock Out	28.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLOCKOUT Configuration bit, under certain conditions.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				B2	B3	B4	B6
ADC	—	29.	Enabling the primary programming/debug port (PGC1/PGD1) on 64 lead variants disables the external and internal references for the ADC, making the ADC unusable.	X	X	X	X
Oscillator	Clock Switch	30.	Firmware clock switch requests to switch from FRC mode, after a FSCM event, may fail.	X	X	X	X
USB	5V Tolerance	31.	The D+ and D– pins are not 5V tolerant.	X	X		
USB	SE0 Transition Detection	32.	The single-ended comparator detects SE0 transitions at a voltage higher than the USB specification.	X	X		
Prefetch Cache	—	33.	If the Predictive Prefetch Cache Enable bits (PREFEN<1:0>) in the CHECON register are non-zero, improper processor behavior may occur during a rare boundary condition.	X			
Flash Program Memory	Programming Operation	34.	NVM registers must not be written immediately after a programming operation is complete.	X			
ADC	Signal Source	35.	When the ADC is in operation, the current channel is shorted to VREF during the conversion period (12 TAD) after sampling.	X			
Timers	—	36.	Writes to the timer registers PRx and TIMERx through the Set/Clear/Invert registers corrupts the data written.	X	X	X	X
USB	Clock	37.	The USB clock does not automatically suspend when entering Sleep mode.	X	X	X	X
UART	—	38.	The TRMT bit is asserted before the transmission is complete.	X	X	X	X
Output Compare	Fault Mode	39.	PWM fault override is not asynchronous.	X	X	X	X
SPI	—	40.	The SPIBUSY and SRMT bits assert 1 bit time before the end of the transaction.	X	X	X	X
Output Compare	—	41.	Faults may be cleared erroneously due to an aborted read.	X	X	X	X
USB	—	42.	The TOKBUSY bit does not correctly indicate status when a transfer completes within the Start of Frame (SOF) threshold.	X	X	X	X
USB	—	43.	The interval between the first two SOF packets generated does not meet USB specification.	X	X	X	X
Output Compare	—	44.	If firmware clears a PWM Fault while a Fault condition is asserted, an interrupt will not be generated for the current Fault.	X	X	X	X
Oscillator	Clock Switch	45.	Clock switching and Two-Speed Start-up may cause a general exception when the reserved bit 8 of the DDPCON register is '0'.	X	X	X	X
UART	—	46.	The RXDA bit does not correctly reflect the RX FIFO status after an overrun event.	X	X	X	X
DMA	CRC Append Mode	47.	In Pattern Match mode, the DMA module may not append all of the CRC results to the result buffer.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				B2	B3	B4	B6
Oscillator	Clock Switch	48.	Clock source switching may cause a general exception or a POR when switching from a slow clock to a fast clock.	X	X	X	X
JTAG	—	49.	On 64-pin devices, the TMS pin requires an external pull-up.	X	X	X	X
Oscillator	—	50.	Changing the PB divisor on the fly may generate exceptions.	X	X	X	X
DMA	—	51.	A suspend followed by an abort does not reset the DMA pointers.	X	X	X	X
DMA	—	52.	Turning off DMA during a transfer may have unintended results.	X	X	X	X
PMP	Slave Mode	53.	The PMP interrupt is generated at the start of the PMP write.	X	X	X	X
PMP	Slave Mode	54.	The IBOV overflow flag may not become set when an overflow occurs.	X	X	X	X
DMA	—	55.	The channel event bit may be incorrect after a suspend.	X	X	X	X
DMA	—	56.	DMA events are not detected during a DMA suspend.	X	X	X	X
SPI	—	57.	Reads of SPIxBUF when SPIRBF is clear will cause erroneous SPIRBF behavior.	X	X	X	X
SPI	Slave Mode	58.	A wake-up interrupt may not be clearable.	X	X	X	X
UART	IrDA®	59.	TX data is corrupted when BRG values greater than 0x200 are used.	X	X	X	X
UART	IrDA	60.	The IrDA minimum bit time is not detected at all baud rates.	X	X	X	X
RTCC	—	61.	The RTCC alarm registers are reset by any device Reset.	X	X	X	X
PORTs	—	62.	I/O pins do not tri-state immediately if previously driven high.	X	X	X	X
UART	UART Receive Buffer Overrun Error Status	63.	The OERR bit does not get cleared on a module Reset. The OERR bit retains its value even after the UART module is reinitialized.	X	X	X	X
ADC	Conversion Trigger from INT0 Interrupt	64.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	X	X	X	X
Comparator	Voltage Reference	65.	The Internal Voltage Reference (IV_{REF}) is set to 1.2V (typical) instead of 0.6V as specified in the device data sheet electrical specifications.	X			
Voltage Regulator	BOR	66.	Device may not exit BOR state if BOR event occurs.	X	X	X	X
I^2C™	Slave Mode	67.	The I^2C module does not respond to address 0x78 when the STRICT and A10M bits are cleared in the I2CxCON register.	X	X	X	X
USB	UIDLE Interrupt	68.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B6**).

1. Module: Device Reset

A Reset ($\overline{MCLR}$) Pulse that is shorter than 2 SYSCLK will not reset the device properly.

Work around

Ensure that the device is held in Reset for more than 2 SYSCLK to ensure proper device Reset operation.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

2. Module: Device Reset

All Resets, except Power-on Reset, can cause a Fail-Safe Clock Monitor event (if enabled) when the duration of the Reset pulse exceeds the clock period of the internal fail-safe clock reference clock (31 kHz).

Work around

If long Reset pulses are anticipated, ignore or disable Fail-Safe Clock Monitor events.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

3. Module: Device Reset

Attempting to perform a software device Reset with PBDIV set to 1:1, and SYSCLK less than 1 MHz will not reset the device properly.

Work arounds

Work around 1:

Change PBDIV before performing a software Reset.

Work around 2:

Set SYSCLK to a value that is greater than 1 MHz.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

4. Module: External Voltage Regulator

A V_{DDCORE} voltage less than 1.75V will cause the CPU to reset when using an external core voltage supply.

Work arounds

Work around 1:

Use the internal voltage regulator.

Work around 2:

Use an external 1.8V regulator, which has a regulation specification of $\leq$ 2.5%. The Microchip TC1055-1.8VCT713 Low Drop-Out (LDO) regulator, or an equivalent, is recommended.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

5. Module: ADC

When running the Analog-to-Digital Converter (ADC) module in Internal Reference mode, the gain error is 3-4 LSb and the offset error is 1-2 LSb across voltage and speed.

Work around

Use in-system calibration and software techniques to compensate for these errors.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

6. Module: Bus Matrix

The BMXDUDBA, BMXDUPBA and BMXPUPBA registers can be set to values that are outside the device's actual memory size limit.

Work around

Do not write values greater than the specified memory size of the device to the Bus Matrix registers. Ensure that the upper bits of the registers remain clear ('0').

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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7. Module: Oscillator

After a clock failure event, any write to the OSCCON register erroneously clears the fail-safe condition and attempts to switch to a new clock source that is specified by the NOSC bits in the OSCCON register.

Work around

After a clock failure event, perform the following steps:

1. Write '000' to the NOSC bits in the OSCCON register to select the Fast RC oscillator. This will ensure that an erroneous clock switch selects the known good on-chip Fast RC oscillator.
2. Modify the OSCCON register with any value your application requires.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

8. Module: DMA

In Pattern Match mode, the DMA will generate up to three additional byte writes to the destination address, after the Pattern Detection event has occurred, when performing transfers with the DCHxSSIZ set to greater than 1.

Work arounds

Work around 1:

The destination buffer needs to be large enough to accommodate the extra bytes (up to 3 extra bytes).

Work around 2:

Set the destination size register to 1.

Work around 3:

Set the source size register to 1.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

9. Module: Output Compare

The Output Compare module in PWM mode outputs a high of period register (PRx) length when attempting to use PWM values of 0x00 followed by 0x01.

Work around

Do not use a PWM value of 0x01.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

10. Module: PMP

In PMP Slave 4B Buffer mode, if the underflow Status bit OBF (PMSTAT<6>) is cleared at the same time a PMP read is attempted, the PMP could receive incorrect data.

Work around

The CPU can read the underflow flag OBUF and set/clear an I/O pin for the external master device to read. The state of the pin should indicate to the external master device that an underflow has occurred and no additional reads should occur until the underflow status has been cleared by the CPU.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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11. Module: I/O PORTs

When using the hardware assisted read-modify-write registers, PORTxINV, PORTxSET and PORTxCLR, the source used for the operation is the LATx register, not the PORTx register. This only affects users who want to use the pins in a bidirectional mode or to store sampled PORTx data in the LATx register.

Work around

Use a software read-modify-write sequence, such as:

```
//replaces PORTAINV = mask;
x = PORTA ^ mask;
LATA = x;

//replaces PORTASET = mask;
x = PORTA | mask;
LATA = x;

//replaces PORTACLR = mask;
x = PORTA & ~mask;
LATA = x;
```

Note: These sequences are not atomic.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

12. Module: Timers

The TMRx register stays at zero for two timer clock cycles when the PRx register is 0x0000.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

13. Module: Timers

The timer prescaler may not be reset correctly when it is used with a slow external clock. This can occur when the timer is disabled and then re-enabled. The result could be a spurious count in the prescaler.

Work around

To ensure a Reset of the prescaler, firmware must wait for at least 2 input clock periods before re-enabling the timer.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

14. Module: Timers

The Timer1 prescaler may not be reset correctly when it is used with a slow external clock. This can occur when the timer is disabled and then re-enabled. The result could be a spurious count in the prescaler.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

15. Module: UART

The CTS pin does not deassert until at least 2 bytes are free in the UART FIFO.

Work around

The UART TXREG must be read at least 2 times to rearm the hardware handshaking lines.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

16. Module: Watchdog Timer (WDT)

An incorrect WDT Time-out Reset may occur when both of these conditions are present:

1. WDT is enabled.
2. Either a $\overline{\text{MCLR}}$ (EXTR) or Software Reset (SWR) occurs just before WDT is about to expire.

Work around

To detect incorrect WDT Time-out Reset, always confirm that only the WDTO bit is set in the RCON register. If EXTR, SWR, or any other Reset bits are set, it indicates that an incorrect WDT has occurred.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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17. Module: DMA

DMA channel abort on a channel that is not currently active may have unintended effects on other active channels.

Work around

1. Suspend the channel, rather than abort, by clearing the channel enable bit DCHxCON<CHEN>.
2. Wait until other DMA channels complete before issuing the abort.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

18. Module: Oscillator

The Primary Oscillator Circuit (POSC), when using XT, XTPLL, HS and HSPLL modes, does not operate over the voltage and temperature range that is listed as item D5 in the device data sheet. The operation range without the work around is limited to -40°C through +70°C when V_{DD} < 3.0V.

Work around

Install a 4.1 MΩ resistor in parallel with the crystal. This allows operation across the temperature range that is listed in the data sheet.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

19. Module: PMP

The WAITE field in PMMODE<1:0> does not add a Wait state to PMP master reads when it is programmed to the value '01'. The WAITE field allows Wait states to be added to the end of PMP read/write operations. This field is intended to add the following Wait clocks after the read operation completes:

00 – no Wait states
01 – 1 Wait state
10 – 2 Wait states
11 – 3 Wait states

Current behavior is the following:

00 – no Wait states
01 – no Wait states
10 – 2 Wait states
11 – 3 Wait states

Work around

This erratum only applies to PMP master read operations. PMP writes work correctly. Use another Wait state control value that is allowed for the attached device.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

20. Module: UART

Using BRG values of 0, 1 or 2 cause the Start bit to be shortened. This results in errors when receiving the data. This issue exists for BRGH values of '0' and '1'.

Work around

Do not use BRG values of 0, 1 or 2. Select system and peripheral bus clocks' frequencies such that the BRG value for the desired Baud Rate Generator value is greater than 2.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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21. Module: Input Capture

16-bit DMA transfers from the ICAP module FIFO buffer do not advance the ICAP FIFO pointer. This results in the entire DMA output buffer being filled with the first value from the ICAP FIFO.

Work around

Configure the DMA to perform 32-bit transfers from the ICAP FIFO.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

22. Module: USB

The USB module does not correctly switch from full-speed to low-speed after sending a PRE packet to a hub.

Work around

Connect a low-speed device directly to the PIC32.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

23. Module: DMA

The DMA buffer may be erroneously filled with the last data read prior to the breakpoint. This buffer fill will continue until the DMA buffer is full. However, the DMA buffer fills correctly if those same peripherals are used as DMA destinations, even when the CPU goes into Debug Exception mode.

This behavior occurs when the DMA controller is actively transferring data and a debugger hits a breakpoint, causes a single-step operation, or halts the target.

Refer to Table 3, which lists the peripherals and input registers that could affect DMA buffer usage.

TABLE 3: REGISTERS AND PERIPHERALS AFFECTED BY BREAKPOINTS DURING DMA TRANSFERS

Peripheral as DMA Source	Transfer from Input Register
Change Notice	PORTx
SPI	SPIxBUF
PMP	PMDIN
UART	UxRXREG
Input Capture	ICxBUF

Work around

If the debugger halts during a DMA transfer from one of these registers, either ignore the DMA transferred data or restart the debug session.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

24. Module: PMP

Events can be missed if the PMDIN register is used as the DMA source or destination and the PMP IRQ is used as the DMA trigger.

Work around

Do not use DMA for PMP read or write operations.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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25. Module: Input Capture

When in 16-bit mode, the upper 16 bits of the 32-bit ICxBUF register contain Timer3 values.

Work around

Mask the upper 16 bits of the read value.

Example: result = 0xFFFF & IC1BUF

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

26. Module: ICSP™

When programming the PIC32 using the 2-wire PGC and PGD pins, programming data appears as an output on the JTAG TDO pin.

Work around

Do not connect the TDO pin to a device that would be adversely affected by rapid pin toggling during programming.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

27. Module: UART

In BRGH = 1 mode, the received data is not sampled in the middle of the bit. This reduces the UART's baud rate mismatch tolerance.

Work around

Use BRGH = 0 mode.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

28. Module: Oscillator

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLOCKOUT Configuration bit, under any of the following conditions.

1. During a Power-on Reset.
2. During device programming.
3. After a JTAG erase. A clock is present on the CLKO pin until the Configuration bit to disable CLOCKOUT is programmed.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

29. Module: ADC

Enabling the primary programming/debug port (PGC1/PGD1) on 64-lead variants disables the external and internal references for the ADC, making the ADC unusable.

Work around

Use the secondary programming/debug port.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

30. Module: Oscillator

After a Fail-Safe Clock Monitor (FSCM) event, the clock source will be FRC. Firmware clock switch requests to switch from FRC mode after an FSCM event may fail. If the clock switch does fail, subsequent retries by firmware will also fail and the clock source will be FRC.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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31. Module: USB

The D+ and D– pins are not 5V tolerant. During normal operation these pins are not subject to 5V. The 5V tolerance specification is intended to prevent device damage in an abnormal operation mode such as connecting a shorted USB cable to the device.

Work around

Do not subject D+ or D– to 5V.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X						

32. Module: USB

The single-ended comparator is detecting SE0 transitions at a higher voltage than indicated in the USB specification. This is a compliance issue relating to items ST2 and ST3 in the Peripheral Silicon checklist, which may result in reduced noise immunity.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X						

33. Module: Prefetch Cache

If the Predictive Prefetch Cache Enable bits (PREFEN<1:0>) in the CHECON register are non-zero, improper processor behavior may occur during a rare boundary condition. This condition occurs only when predictive prefetch is enabled, and can occur in both cacheable and non-cacheable memory areas. The prefetch buffer can be overwritten by the “next” 16-bytes of instructions causing invalid instruction execution. This may cause an invalid instruction fault, or execution of a wrong instruction.

Work around

Make sure that the PREFEN field in CHECON is programmed to ‘00’. The cache is still used, although predictive prefetching will be disabled.

Affected Silicon Revisions

B2	B3	B4	B6				
X							

34. Module: Flash Program Memory

NVM registers must not be written immediately after a programming operation is complete. When a NVM operation completes, the NVMWR bit (NVMCON<15>) switches states from ‘1’ to ‘0’, indicating that another NVM operation may be started. However, there is a period of two internal FRC clocks after this transition where a write to NVMCON may not work correctly. Since the internal FRC clock is 8 MHz, and the system clock may be much faster, care must be taken to ensure that the correct delay is met.

Work around

Wait at least 500 ns after seeing a ‘0’ in NVMCON<15> before writing to any NVM registers.

Affected Silicon Revisions

B2	B3	B4	B6				
X							

35. Module: ADC

When the ADC is in operation, the current channel is shorted to VREF during the conversion period (12 TAD) after sampling. The impact on high-impedance sources is that they may not have time to recover between conversions. The impact on low-impedance sources is a high current draw, which may damage either the source or the device.

Work around

Place a 5k resistor between the device and any external capacitance on the board to limit current draw.

Affected Silicon Revisions

B2	B3	B4	B6				
X							

36. Module: Timers

Writes to the timer registers PRx and TIMERx through the Set/Clear/Invert registers corrupts the data written.

Work around

Do not write to the affected Set/Clear/Invert registers. Use software read-modify-write sequences to change individual bits or write directly to the PRx and TIMERx registers.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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37. Module: USB

The USB clock does not automatically suspend when entering Sleep mode.

Work around

Turn off the USB clock before entering Sleep mode.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

38. Module: UART

The TRMT bit is asserted during the STOP bit generation not after the STOP bit has been sent.

Work around

If firmware needs to be aware when the transmission is complete, firmware should add a half bit time delay after the TRMT bit is asserted.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

39. Module: Output Compare

The fault override of the PWM output pin(s) does not occur asynchronously; it is synchronized to the PB clock. The synchronization takes up to 2 PB clock periods for the fault event to tri-state the PWM output pin.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

40. Module: SPI

The SPIBUSY and SRMT bits assert 1 bit time before the end of the transaction.

Work around

Firmware must provide a 1 bit time delay between the assertion of these bits and performing any operation that requires the transaction to be complete.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

41. Module: Output Compare

The Output Compare module may reinitialize or clear a Fault on an aborted read of the OCxCON register. An aborted read occurs when a read instruction in the CPU pipeline has started execution, but is aborted due to an interrupt.

Work around

Disable interrupts before reading the contents of the OCxCON register, and then re-enable interrupts after reading the register.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

42. Module: USB

The TOKBUSY bit does not correctly indicate status when a transfer completes within the Start of Frame threshold.

Work around

Use a firmware semaphore to track when a token is written to U1TOK. Firmware then clears the semaphore when the transfer is complete.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

43. Module: USB

The interval between the first two SOF packets generated does not meet the USB specification. The first count could be short due to an uninitialized counter.

Work around

There is no work around for the non-compliant timing. It is recommended that firmware not send data in the first frame.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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44. Module: Output Compare

If firmware clears a PWM Fault while a Fault condition is asserted, an interrupt will not be generated for the current Fault.

Work around

Firmware must poll the OCFLT bit to determine if a Fault condition still exists.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

45. Module: Oscillator

Clock switching and Two-Speed Start-up may cause a general exception when the reserved bit 8 of the DDPCON register is '0'.

Work around

Ensure that the reserved bit 8 of the DDPCON register to set to '1'. For example, DDPCON = 0x100.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

46. Module: UART

The RXDA bit does not correctly reflect the RX FIFO status after an overrun event.

Work around

1. Clear the OERR bit. The FIFO pointer will be reset and the RXDA bit will reflect the current FIFO status.
2. If the contents of the FIFO are required, they can be read by reading the UxRXREG register four times. There are no status bits that will correctly reflect when the last valid data was read.
3. Clear the OERR bit. The FIFO pointer will be reset and the RXDA will reflect the current FIFO status.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

47. Module: DMA

In Pattern Match mode, the DMA module may not append all of the CRC results to the result buffer.

Work around

Use firmware to read the CRC result and append it to the result buffer.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

48. Module: Oscillator

Clock source switching may cause a general exception or a POR when switching from a slow clock to a fast clock.

Work around

Clock source switches should be performed by first switching to the FRC, and then switching to the target clock source.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

49. Module: JTAG

On 64-pin devices, an external pull-up resistor is required on the TMS pin for proper JTAG.

Work around

Connect a 100k-200k pull-up to the TMS pin.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

50. Module: Oscillator

Changing the PB divisor on the fly may generate exceptions.

Work around

Ensure 8 NOP instructions precede the write to the PBDIV bits and 8 NOP instructions follow the write to the PBDIV bits.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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51. Module: DMA

If a DMA channel is suspend in the middle of a transfer and an abort is issued, the channel's source, destination and cell pointer registers are not reset.

Work around

Suspend the channel after the channel is aborted.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

52. Module: DMA

Turning the DMA module off while a transaction is in progress may cause invalid instruction or data fetches.

Work around

Ensure all DMA transactions are complete or abort DMA transactions before turning off the DMA module.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

53. Module: PMP

In Slave mode, the PMP interrupt is generated at the start of the PMP write instead of at the end of the write generated by the master. When the master write occurs slowly in relation to the PB clock, it is possible for the CPU to respond to the interrupt before the data written by the master has been latched.

Work around

Poll the PMSTAT register in the ISR to determine when the data is available.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

54. Module: PMP

In Slave mode, the IBOV overflow flag may not become set when an overflow occurs.

Work around

Do not allow the PMP buffer to overflow.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

55. Module: DMA

The channel event bit may remain set if a transaction completes as the user suspends the channel by clearing the corresponding CHEN bit. This has the effect that as soon as the channel is re-enabled the event that should have been cleared after the last transfer will still be pending and the transfer will begin immediately after the channel is re-enabled without waiting for an interrupt.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

56. Module: DMA

DMA events are not detected during DMA suspend. Any interrupt event that would initiate a DMA transfer will not be captured while DMA is suspended. When DMA is re-enabled the event will have been lost.

Work around

Read the status of the peripheral interrupt flag. If the interrupt has been asserted, force a DMA transaction.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

57. Module: SPI

Reads of the SPIxBUF register when the SPIRBF bit is clear will cause erroneous SPIRBF behavior. Subsequent data in the buffer will not be reflected by the SPIRBF bit.

Work around

Only read the SPIxBUF register when the SPIRBF bit is set.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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58. Module: SPI

In Slave mode when entering Sleep mode after a SPI transfer with SPI interrupts enabled, a false interrupt may be generated waking the device. This interrupt can be cleared; however, entering Sleep may cause the condition to occur again.

Work around

Do not use SPI in Slave mode as a wake-up source from Sleep.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

59. Module: UART

In IrDA® mode with baud clock output enabled, the UART TX data is corrupted when the BRG value is greater than 0x200.

Work around

Use the Peripheral Bus (PB) divisor to lower the PB frequency such that the required UART BRG value is less than 0x201.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

60. Module: UART

The UART module is not fully IrDA compliant. The module does not detect the 1.6 µs minimum bit width at all baud rates as defined in the IrDA specification. The module does detect the 3/16 bit width at all baud rates.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

61. Module: RTCC

The RTCC alarm registers (RTCALRM, ALRMTIME and ALRMDATE) are reset by any device Reset.

Work around

For devices with code-protect disabled: If the alarm information must be retained through a Reset, the information must be stored in RAM or Flash.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

62. Module: PORTs

When an I/O pin is set to output a logic high signal, and is then changed to an input using the TRISx registers, the I/O pin should immediately tri-state and let the pin float. Instead, the pin will continue to partially drive a logic high signal out for a period of time.

Work around

The pin should be driven low prior to being tri-stated if it is desirable for the pin to tri-state quickly.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

63. Module: UART

The OERR bit does not get cleared on a module reset. If the OERR bit is set and the module is disabled, the OERR bit retains its status even after the UART module is reinitialized.

Work around

The user software must check this bit in the UART module initialization routine and clear it if it is set.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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64. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternatively, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

65. Module: Comparator

The Internal Voltage Reference (IV_{REF}) is set to 1.2V (typical) instead of 0.6V as specified in the device data sheet electrical specifications.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X							

66. Module: Voltage Regulator

Device may not exit BOR state if BOR event occurs.

Work arounds

Work around 1:

V_{DD} must remain within the published specification (see parameter DC10 of the device data sheet).

Work around 2:

Reset device by providing POR condition.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

67. Module: I^2C™

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I^2C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but does not.

Work around

None.

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

68. Module: USB

In the case where the bus has been idle for > 3 ms, and the UIDLE interrupt flag is set, if software clears the interrupt flag, and the bus remains idle, the UIDLE interrupt flag will not be set again.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption. (Resume, Reset, SOF, or Error).

Note: Resume and Reset are the only interrupts that should be gotten following UIDLE assertion. If, at any point in time, the UIDLE bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). Note that this will require software to clear the UIDLE interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

B2	B3	B4	B6				
X	X	X	X				

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS61143**H**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Comparator Specifications

The minimum, typical and maximum values for the Internal Voltage Reference (parameter D305) in Table 29-12 were stated incorrectly in the data sheet. The correct values are shown in bold type in Table 4.

TABLE 4: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D305	IVREF	Internal Voltage Reference	**0.57**	**0.6**	**0.63**	V	—

2. Module: Flash Program Memory

The following Note and Example will be added to **Section 5.0 "Flash Program Memory"** in the next revision of the data sheet.

Note:	Flash LVD Delay (LVDstartup) must be taken into account between setting up and executing any Flash command operation. See Example 5-1 for a code example to set up and execute a Flash command operation.

EXAMPLE 5-1:

```
NVMCON = 0x4004;           // Enable and configure for erase operation
Wait(delay);               // Delay for 6 µs for LVDstartup

NVMKEY = 0xAA996655;
NVMKEY = 0x556699AA;
NVMCONSET = 0x8000;        // Initiate operation

while(NVMCONbits.WR==1);   // Wait for current operation to complete
```

3. Module: Pin Diagrams

In all pin diagrams in the current revision of the data sheet, the D– and D+ pins are incorrectly indicated as 5V-tolerant pins through the use of shading. The D– and D+ pins are not 5V-tolerant pins and should not be shaded in the pin diagrams.

4. Module: AC Characteristics: Standard Operating Conditions

The Standard Operating conditions in the following tables show the incorrect starting voltage range of 2.3V. The correct starting range is: **2.5V**:

- Table 29-34: ADC Module Specifications
- Table 29-35: 10-bit ADC Conversion Rate Parameters
- Table 29-36: Analog-to-Digital Conversion Timing Requirements

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APPENDIX A: REVISION HISTORY

Rev A Document (4/2009)

Initial release of this document; issued for revision B2, B3, and B4 silicon.

Includes silicon issues 1 (Device Reset), 2-3 (Device Reset), 4 (External Voltage Regulator), 5 (ADC), 6 (Bus Matrix), 7 (Oscillator), 8 (DMA), 9 (Output Compare), 10 (PMP), 11 (I/O PORTs), 12-14 (Timers), 15 (UART), 16 (Watchdog Timer (WDT)), 17 (DMA), 18 (Oscillator), 19 (PMP), 20 (UART), 21 (Input Capture), 22 (USB), 23 (DMA), 24 (PMP), 25 (Input Capture), 26 (ICSP™), 27 (UART), 28 (Oscillator), 29 (ADC), 30 (Oscillator), 31-32 (USB), 33 (Prefetch Cache), 34 (Flash Program Memory) and 35 (ADC), and data sheet clarification 1 (D+ and D– Inputs).

This document replaces the following errata documents:

- DS80350, *"PIC32MX3XX/4XX Rev. B2 Silicon Errata"*
- DS80367, *"PIC32MX3XX/4XX Rev. B3 Silicon Errata"*
- DS80402, *"PIC32MX3XX/4XX Rev. B4 Silicon Errata"*

Rev B Document (9/2010)

Updated silicon issue 24 (PMP).

Added silicon issues 36 (Timers), 37 (USB), 38 (UART), 39 (Output Compare), 40 (SPI), 41 (Output Compare), 42-43 (USB), 44 (Output Compare), 45 (Oscillator), 46 (UART), 47 (DMA), 48 (Oscillator), 49 (JTAG), 50 (Oscillator), 51-52 (DMA), 53-54 (PMP), 55-56 (DMA), 57-58 (SPI), 59-60 (UART), 61 (RTCC), 62 (PORTs) and 63 (UART).

Removed data sheet clarification 1; data sheet was updated.

Rev C Document (11/2010)

Updated current silicon revision to B6.

Added silicon issues 64 (ADC) and 65 (Comparator), and data sheet clarification 1 (Comparator Specifications).

Rev D Document (12/2010)

Added silicon issue 66 (Voltage Regulator).

Rev E Document (3/2011)

Added data sheet clarification issues 2 (Flash Program Memory) and 3 (Pin Diagrams).

Rev F Document (10/2011)

Added silicon issues 67 (I^2C™) and 68 (USB).

Added data sheet clarification issue 4 (AC Characteristics: Standard Operating Conditions).

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NOTES:

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