

## Pin Description

Pin#	Pin Name	Type		Description
1, 3, 5, 7, 8, 17, 18, 20, 22, 24	CLK0~9	Output		Clock Outputs
2, 6, 19, 23	V <sub>DDO</sub>	Power		Output Power Supplier
15, 26	GND	Power		Output Ground
4, 9, 16, 21, 25, 32	G <sub>NDO</sub>	Power		Core Ground
10	V <sub>DD</sub>	Power		Core Power Supplier
11	XIN	Input		Crystal interface
12	XOUT	Output		Crystal interface
13	IN0	Input	Pull-down	REF0 Diff or Single End
14	IN0#	Input	Pull-up/ Pull-down	REF0 Diff, When IN0 is single end ref clock0 and IN0# internal bias as V <sub>dd</sub> /2
27	IN1#	Input	Pull-up/ Pull-down	REF1 Diff, When IN1 is single end ref clock1 and IN1# internal bias as V <sub>dd</sub> /2
28	IN1	Input	Pull-down	REF1 Diff or Single End
30, 29	IN_SEL[0:1]	Input	Pull-down	IN-SEL[0:1] select XTAL, REF1 and REF0 input
31	ENABLE	Input		Active High Output Enable

## Input Mode Selection Logic

IN_SEL0	IN_SEL1	Selected Input
1	1	XTAL
0	1	XTAL
1	0	REF1 Diff or Single End
0	0	REF0 Diff or Single End

## Input/Output Operation State

Input State	Output State
IN[0:1], IN[0:1]# open	Logic Low
IN[0:1], IN[0:1]# both to ground	Logic Low
IN[0:1]=High, IN[0:1]# =Low	Logic High
IN[0:1]=Low, IN[0:1]# =High	Logic Low

## Output Mode Selection

ENABLE	Output CLK0~9
GND	High-impedance
VDD	Enabled

**PI6C49X0210-A**
**Power Supply DC Characteristics** ( $V_{DD}/V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			32	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			1	mA

**Power Supply DC Characteristics** ( $V_{DD}/V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			15	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.7	mA

**Power Supply DC Characteristics** ( $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			29	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.6	mA

**Power Supply DC Characteristics** ( $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			29	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.4	mA

**Power Supply DC Characteristics** ( $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.35	1.5	1.65	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			29	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.3	mA

**Power Supply DC Characteristics** ( $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			13	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.4	mA

**Power Supply DC Characteristics** ( $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.35	1.5	1.65	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			13	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.3	mA

**Single-Ended DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  or  $T_B = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ )

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3\text{V} \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5\text{V} \pm 5\%$	1.7		$V_{DD} + 0.3$	V
		IN0, IN1, $V_{DD} = 3.3\text{V} \pm 5\%$	2		$V_{DD} + 0.3$	V
		IN0, IN1, $V_{DD} = 2.5\text{V} \pm 5\%$	1.6		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3\text{V} \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5\text{V} \pm 5\%$	-0.3		0.7	V
		IN0, IN1, $V_{DD} = 3.3\text{V} \pm 5\%$	-0.3		1.3	V
		IN0, IN1, $V_{DD} = 2.5\text{V} \pm 5\%$	-0.3		0.9	V
$V_{OH}$	Output High Voltage ( $I_{OH} = -8\text{mA}$ )	$V_{DDO} = 3.3\text{V} \pm 5\%$ <sup>(1)</sup>	2.6			V
		$V_{DDO} = 2.5\text{V} \pm 5\%$	2.0			V
		$V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$ <sup>(1)</sup>	1.5			V
		$V_{DDO} = 1.5\text{V} \pm 0.15\text{V}$ <sup>(1)</sup>	1.0			V
	Output High Voltage ( $I_{OH} = -12\text{mA}$ )	$V_{DDO} = 3.3\text{V} \pm 5\%$ <sup>(1)</sup>	3.0			V
		$V_{DDO} = 2.5\text{V} \pm 5\%$	2.0			V
		$V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$ <sup>(1)</sup>	1.5			V
		$V_{DDO} = 1.5\text{V} \pm 0.15\text{V}$ <sup>(1)</sup>	1.0			V
$V_{OL}$	Output Low Voltage ( $I_{OL} = 8\text{mA}$ )	$V_{DDO} = 3.3\text{V} \pm 5\%$ <sup>(1)</sup>			0.5	V
		$V_{DDO} = 2.5\text{V} \pm 5\%$			0.5	V
		$V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$ <sup>(1)</sup>			0.4	V
		$V_{DDO} = 1.5\text{V} \pm 0.15\text{V}$ <sup>(1)</sup>			0.35	V
	Output Low Voltage ( $I_{OL} = 12\text{mA}$ )	$V_{DDO} = 3.3\text{V} \pm 5\%$ <sup>(1)</sup>			0.25	V
		$V_{DDO} = 2.5\text{V} \pm 5\%$			0.25	V
		$V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$ <sup>(1)</sup>			0.3	V
		$V_{DDO} = 1.5\text{V} \pm 0.15\text{V}$ <sup>(1)</sup>			0.35	V
$R_{OUT}$	Output Impedence	$V_{DDO} = 3.3\text{V} \pm 5\%$ <sup>(1)</sup>		9		$\Omega$
		$V_{DDO} = 2.5\text{V} \pm 5\%$		10		$\Omega$
		$V_{DDO} = 1.8\text{V} \pm 0.2\text{V}$		20		$\Omega$
		$V_{DDO} = 1.5\text{V} \pm 0.15\text{V}$		30		$\Omega$

**Notes:**

1. Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, "Load Test Circuit" diagrams.

**Differential input DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  or  $T_B = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ )

Symbols	Parameters		Test Conditions	Min.	Typ	Max.	Units
$I_{IH}$	Input High Current	IN[0:1], IN[0:1]#	$V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			100	$\mu\text{A}$
$I_{IL}$	Input Low Current	IN[0:1]	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ $V_{IN} = 0\text{V}$	-1			$\mu\text{A}$
		IN[0:1]#	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ $V_{IN} = 0\text{V}$	-50			$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage <sup>(1)</sup>		$V_{DD} = 3.3\text{V}$	0.25		1.3	V
			$V_{DD} = 2.5\text{V}$	0.25		1.3	
$V_{CMR}$	Common Mode Input Voltage <sup>(1,2)</sup>		$V_{DD} = 3.3\text{V}$	0.5		$V_{DD} - 0.85\text{V}$	V
			$V_{DD} = 2.5\text{V}$	0.5		$V_{DD} - 0.85\text{V}$	

**Notes:**

- $V_{IL}$  should not be less than  $-0.3\text{V}$ .
- Common mode voltage is defined as  $V_{IH}$ .

**Absolute Maximum Ratings** (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V <sub>DD</sub> , V <sub>DDO</sub> Voltage .....	-0.5V to +3.6V
Output Voltage .....	-0.5V to V <sub>DD</sub> +0.5V
Input Voltage .....	-0.5V to V <sub>DD</sub> +0.5V
Junction Temperature .....	125°C max

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**AC Characteristics** (Over Operating Range: V<sub>DD</sub>/V<sub>DDO</sub> = 3.3V ± 5%, T<sub>A</sub> = -40°C to 85°C or T<sub>B</sub> = -40°C to 105°C)

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jitt(Ø)</sub>	RMS Phase Jitter (Random)		25MHz crystal @ (Integration Range: 100Hz-1MHz)		0.2		ps
t <sub>jitt(additive)</sub>	Additive RMS Phase Jitter (Random)		125MHz reference input @ (Integration Range: 12kHz-20MHz)		0.05		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		800	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		64		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

**Notes:**

1. Unless noted otherwise, all parameters are tested with xtal @ f ≤ F<sub>xtal\_max</sub>; outputs are terminated @ 50Ω to V<sub>DDO</sub>/2, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as V<sub>DD</sub>/2
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

**Absolute Maximum Ratings** (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V <sub>DD</sub> , V <sub>DDO</sub> Voltage .....	-0.5V to +3.6V
Output Voltage .....	-0.5V to V <sub>DD</sub> +0.5V
Input Voltage .....	-0.5V to V <sub>DD</sub> +0.5V
Junction Temperature .....	125°C max

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**AC Characteristics** (Over Operating Range: V<sub>DD</sub>/V<sub>DDO</sub> = 2.5V ± 5%, T<sub>A</sub> = -40°C to 85°C or T<sub>B</sub> = -40°C to 105°C)

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jitt(Ø)</sub>	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.2		ps
t <sub>jitt(additive)</sub>	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		800	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		63		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

**Notes:**

1. Unless noted otherwise, all parameters are tested with xtal @ f ≤ F<sub>xtal\_max</sub>; outputs are terminated @ 50Ω to V<sub>DDO</sub>/2, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as V<sub>DD</sub>/2
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

## AC Characteristics

(Over Operating Range:  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jitter</sub> (Ø)	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.2		ps
t <sub>jitter</sub> (additive)	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		800	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		62		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

### Notes:

1. Unless noted otherwise, all parameters are tested with xtal @  $f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.



## AC Characteristics

(Over Operating Range:  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jitt(Ø)</sub>	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.15		ps
t <sub>jitt(additive)</sub>	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		900	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		58		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

### Notes:

1. Unless noted otherwise, all parameters are tested with xtal @  $f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

## AC Characteristics

(Over Operating Range:  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jitt(Ø)</sub>	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.2		ps
t <sub>jitt(additive)</sub>	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		900	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		53		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

### Notes:

1. Unless noted otherwise, all parameters are tested with xtal @  $f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

## AC Characteristics

(Over Operating Range:  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jit(Ø)</sub>	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.15		ps
t <sub>jit(additive)</sub>	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.12		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		900	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		59		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

### Notes:

1. Unless noted otherwise, all parameters are tested with xtal @  $f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

## AC Characteristics

(Over Operating Range:  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  or  $T_B = -40^\circ C$  to  $105^\circ C$ )

Parameters	Description		Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal		10		50	MHz
		Using External Clock Source <sup>(2)</sup>		DC		200	
odc	Output Duty Cycle		125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>					80	ps
t <sub>jit(Ø)</sub>	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.15		ps
t <sub>jit(additive)</sub>	Additive RMS Phase Jitter (Random)		125MHz @ (Integration Range: 12kHz-20MHz)		0.05		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		900	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>	ENABLE				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>	ENABLE				5	cycles
MUX <sub>isolation</sub>	MUX Isolation		155.52MHz		55		dB
t <sub>STARTUP</sub>	Crystal Input Start up time		From 90% VDD		2	10	ms

### Notes:

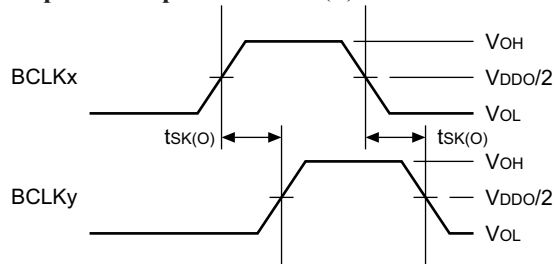
1. Unless noted otherwise, all parameters are tested with xtal @  $f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 4 cycles. Min. setup time = 3ns.

## Crystal Oscillator Characteristics

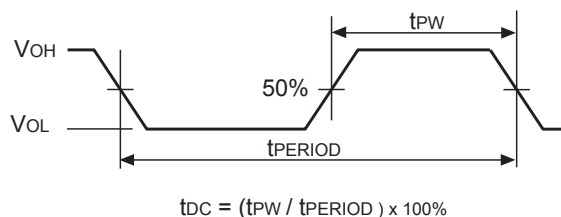
Parameters	Description	Min	Typ	Max.	Units
OSCMODE	Mode of Oscillation	Fundamental			
FREQ	Frequency	10	25	50	MHz
CON-CHIP	On chip Load Capacitance		12		pF

## Waveforms

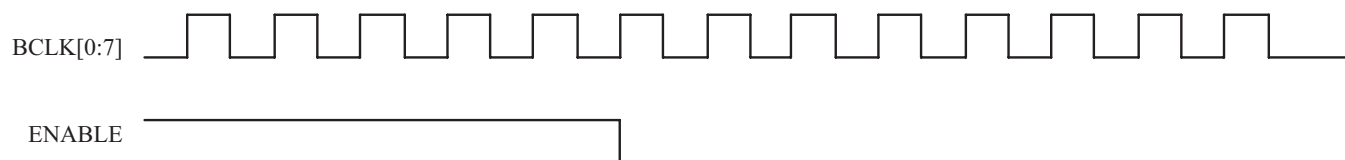
**Output to Output Skew –  $t_{sk(O)}$**



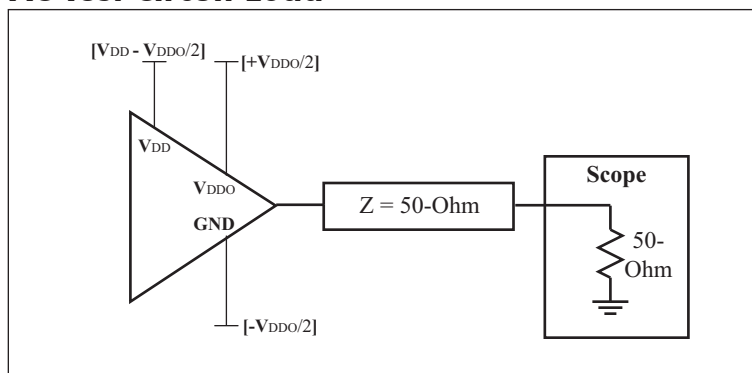
**Duty Cycle –  $t_{DC}$**



**ENABLE Timing Diagram**



## AC Test Circuit Load



**Note:**

$V_{DD}/V_{DDO} = 1.8V \pm 0.2V,$   
 $2.5V \pm 5\%,$   
 $3.3V \pm 5\%$

**Crystal Characteristic** (link to "<http://www.pericom.com/products/timing/crystals/index.php>" for more detailed and different size crystal specifications)

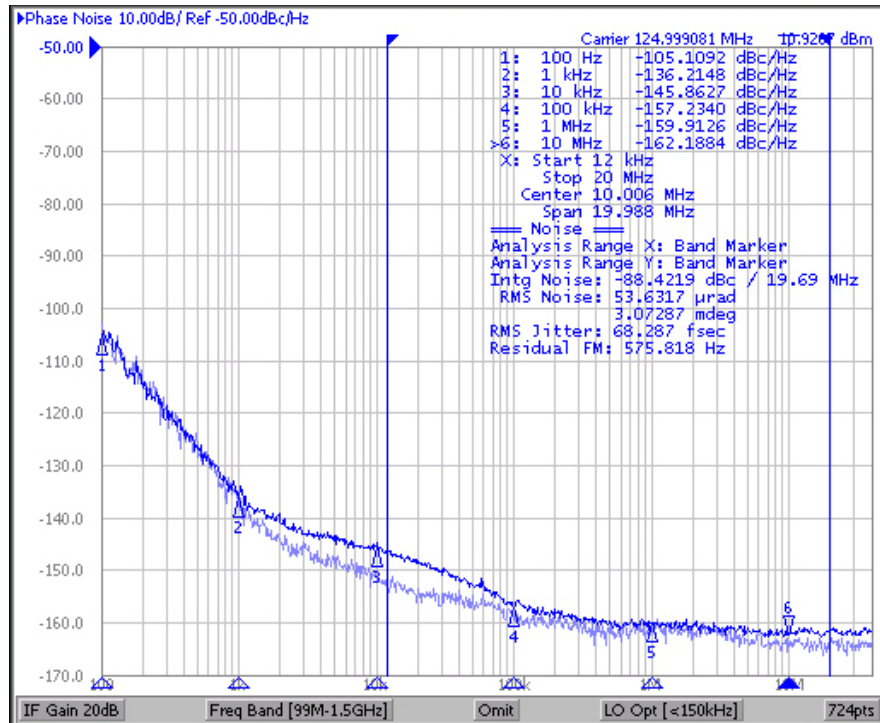
Parameters	Description	Min	Typ	Max.	Units
OSCMODE	Mode of Oscillation	Fundamental			
FREQ	Frequency	10	25	50	MHz
ESR <sup>(1)</sup>	Equivalent Series Resistance	30		50	Ohm
CLOAD	Load Capacitance		18		pF
CSHUNT	Shunt Capacitance			7	pF
DRIVE level				1	mW

**Note:** 1. ESR value is dependent upon frequency of oscillation

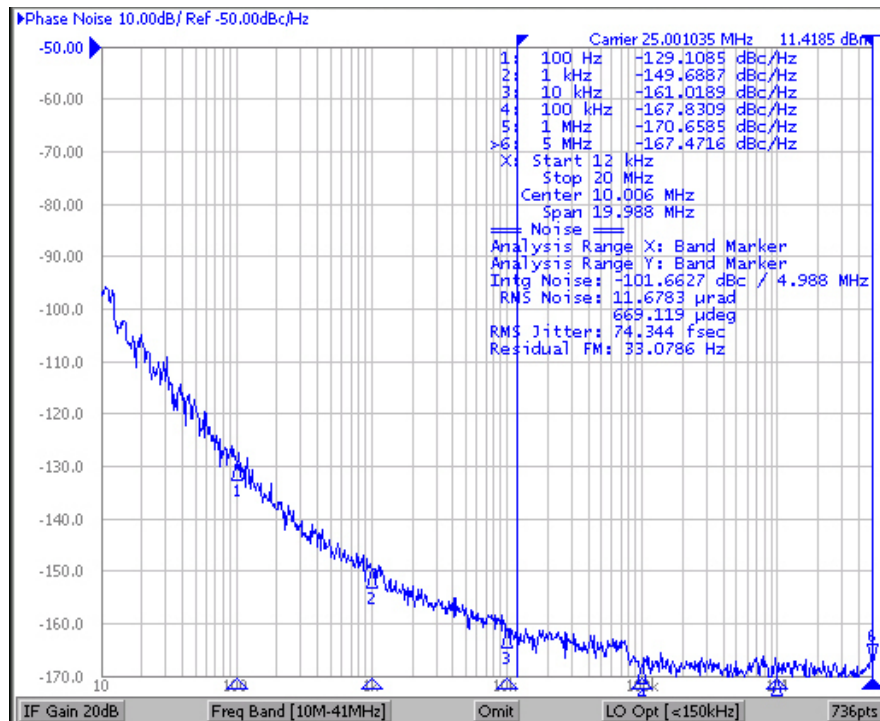
## Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at ~47fs RMS (12kHz to 20MHz). Additive jitter =  $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



## Oscillator Phase Jitter



## Application Information

### Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .

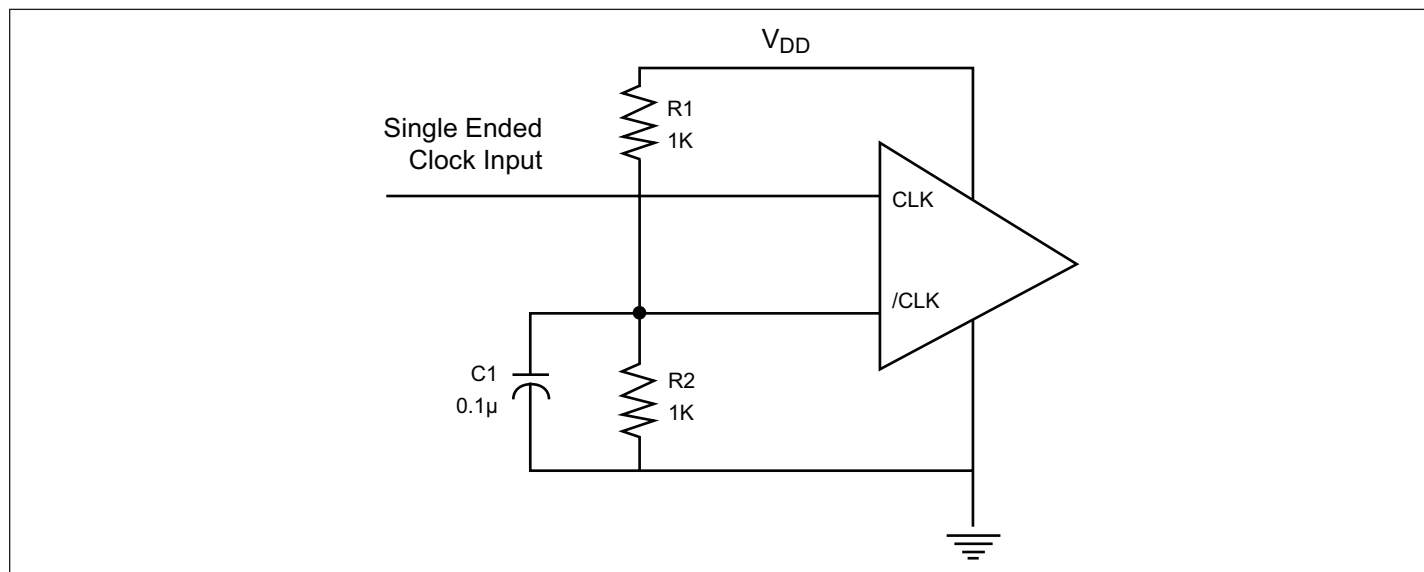
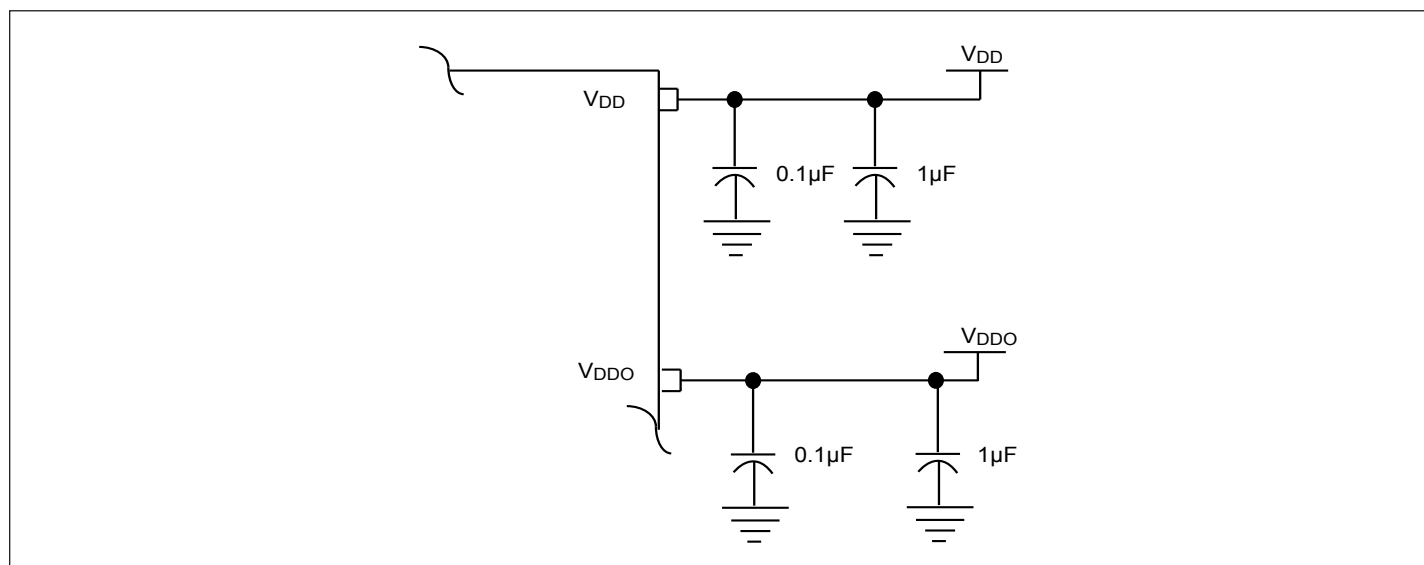


Figure 1. Single-ended input to Differential input device

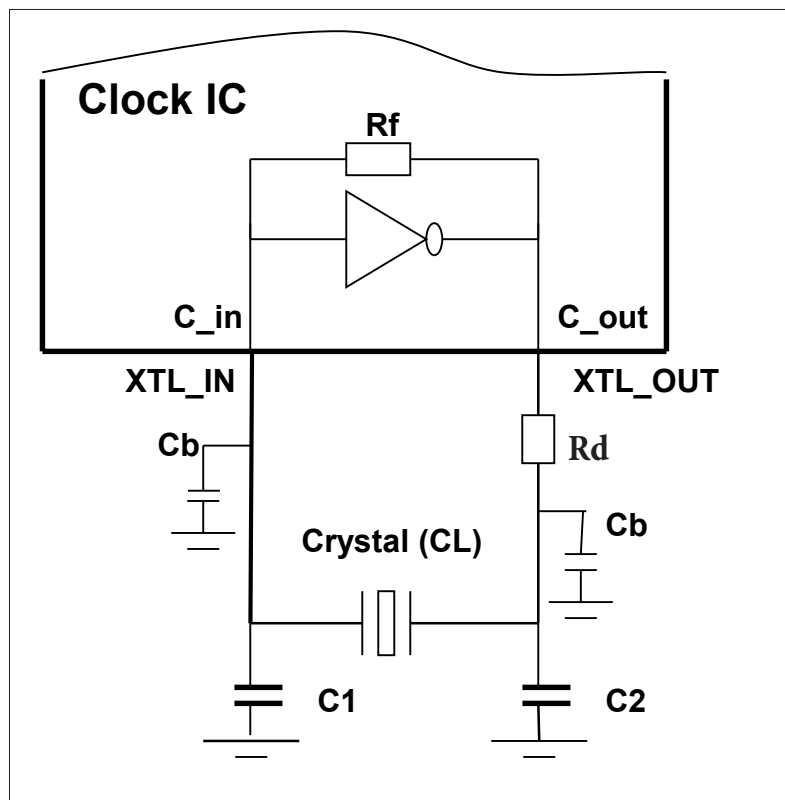
## Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, 0.1μF and 1μF bypass capacitors should be used for each pin.



## Application Notes

### Clock IC Crystal loading cap. design guide



CL =crystal spec. loading cap.

C\_in/out = (3~5pF) of IC pin cap.

Cb = PCB trace (2~4pF)

C1,C2 = load cap. of design

Rd = 50 to 100ohm drive level limit  
(Optimized for 25MHz 18pf XTAL  
without Rd)

Design guide:  $C1=C2=2 * CL - (Cb + C_{in/out})$  to meet target +/-ppm < 20 ppm

Example1: Select CL=18 pF crystal,  $C1=C2=2*(18pF) - (4pF+5pF)=27pF$ , check datasheet too

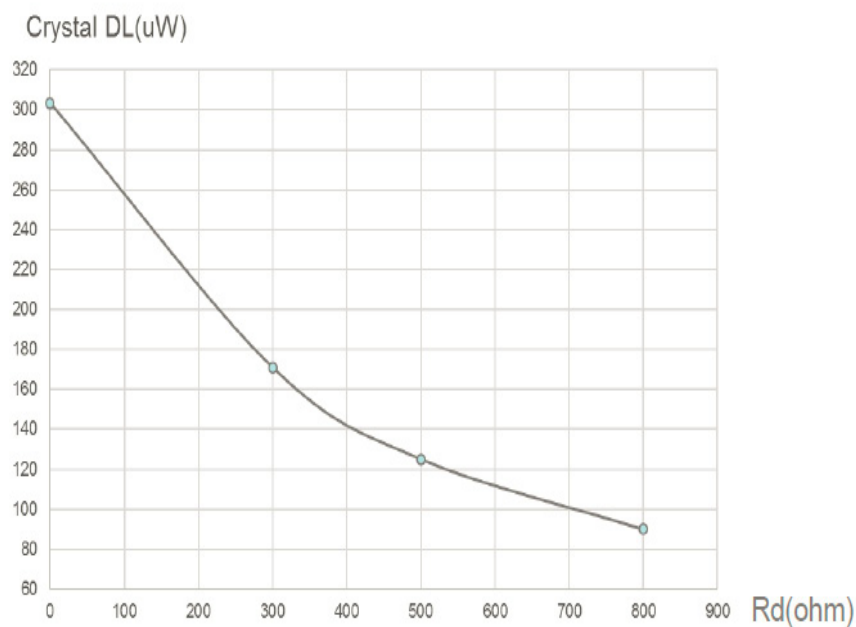
Example2: For higher frequency crystal ( $\Rightarrow 20MHz$ ), can use formula  $C1=C2=2*(CL-6)$ , can do fine tune of C1, C2 for more accurate ppm if necessary

### Thermal Information

Symbol	Description	Condition	
$\Theta_{JA}$	Junction-to-ambient thermal resistance	Still air	44.7 °C/W
$\Theta_{JC}$	Junction-to-case thermal resistance		21.7 °C/W



## Crystal Input Drive Level vs Series Resistor Value



Note:

1. Drive Level above is with regards to VDD = 3.3V. If VDD = 2.5V, drive level is 25% lower
2. For Rd = 0 Ohm, Drive Level = 310  $\mu$ W

## Part Marking

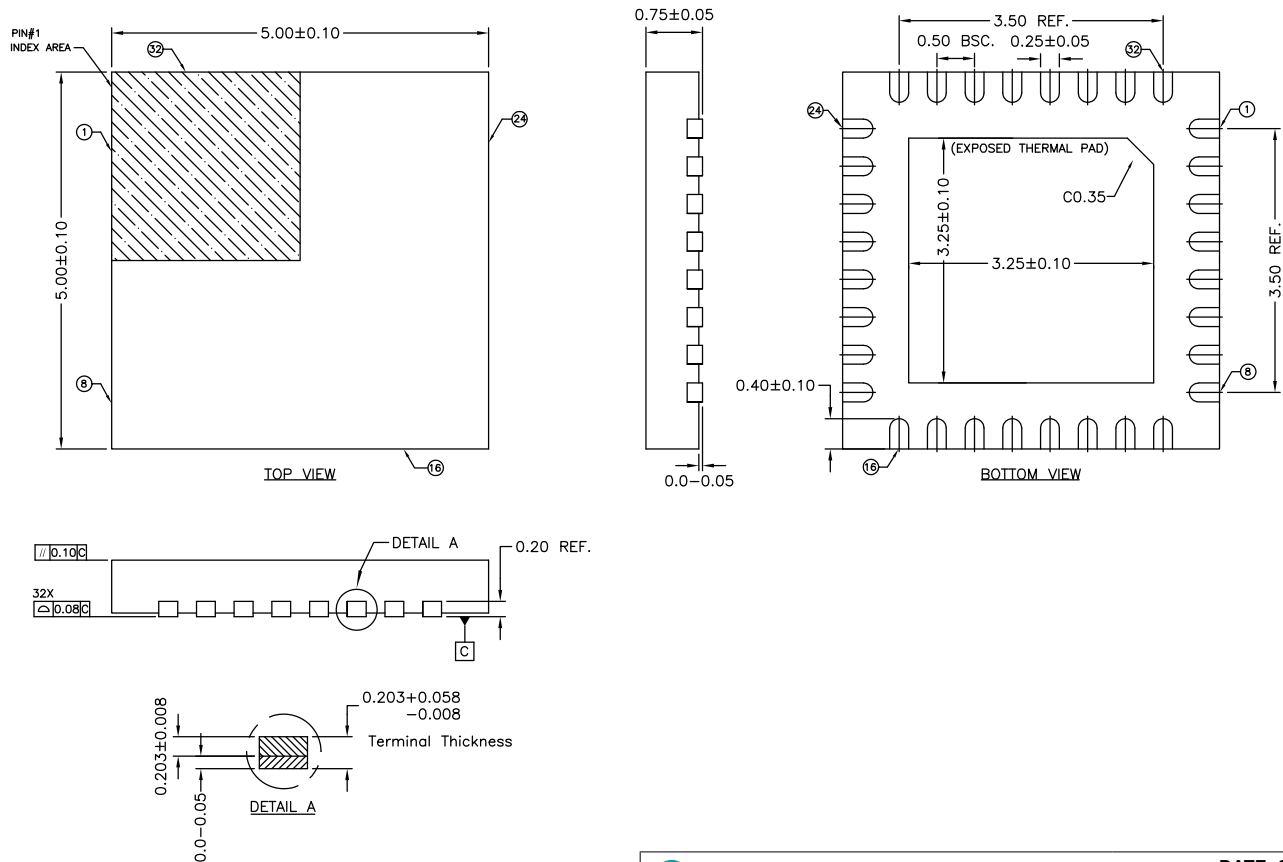
ZH Package



YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

**PI6C49X0210-A**

## Packaging Mechanical: 32-TQFN (ZH)



### Notes:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)
5. THIS POD IS FOR DEVICE: PI6C49X0210.



DATE: 05/15/13

DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH32

DOCUMENT CONTROL #: PD-2070HW

REVISION: B

### For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

## Ordering Information<sup>(1,2,3)</sup>

Ordering Code	Package Code	Package Description
PI6C49X0210-AZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN)

### Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at [www.diodes.com/design/support/packaging/](http://www.diodes.com/design/support/packaging/)
3. E = Pb-free and Green
4. X suffix = Tape/Reel

**IMPORTANT NOTICE**

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

**LIFE SUPPORT**

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2016, Diodes Incorporated  
[www.diodes.com](http://www.diodes.com)