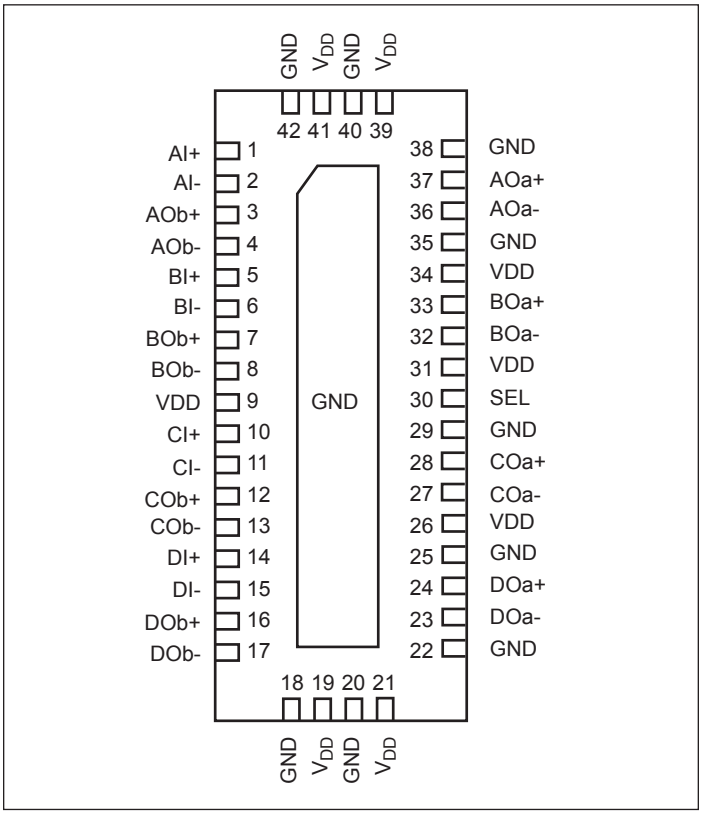
Pin Configuration

42-TQFN (ZH) Top-Side View



Pin Descriptions

Pin#	Pin Name	Type	Description
1, 2	AI+, AI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the AOa+, AOa- pin respectively when SEL=0. Signal is routed to the AOb+, AOb- pin respectively when SEL = 1.
37, 36	AOa+, AOa-	Differential I/O	Differential analog pass-through I/O. Signal from AI+ and AI- is routed to AOa+ and AOa- respectively when SEL=0.
3, 4	AOb+, AOb-	Differential I/O	Differential analog pass-through I/O. Signal from AI+ and AI- is routed to AOb+ and AOb- respectively when SEL=1.
5, 6	BI+, BI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the BOa+, BOa- pin respectively when SEL=0. Signal is routed to the BOb+, BOb- pin respectively when SEL = 1.
33, 32	BOa+, BOa-	Differential I/O	Differential analog pass-through I/O. Signal from BI+ and BI- is routed to BOa+ and BOa- respectively when SEL=0.
7, 8	BOb+, BOb-	Differential I/O	Differential analog pass-through I/O. Signal from BI+ and BI- is routed to BOb+ and BOb- respectively when SEL=1.
10, 11	CI+, CI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the COa+, COa- pin respectively When SEL=0. Signal is routed to the COb+, COb- pin respectively when SEL = 1.

Pin Descriptions Cont.

Pin#	Pin Name	Type	Description
28, 27	COa+, COa-	Differential I/O	Differential analog pass-through I/O. Signal from CI+ and CI- is routed to COa+, COa- pin respectively when SEL = 0.
12, 13	COb+, COb-	Differential I/O	Differential analog pass-through I/O. Signal from CI+ and CI- is routed to COb+, COb- pin respectively when SEL = 1.
14, 15	DI+, DI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the DOa+, DOa- pin respectively when SEL=0. Signal is routed to the DOb+, DOb- pin respectively when SEL = 1.
24, 23	DOa+, DOa-	Differential I/O	Differential analog pass-through I/O. Signal from DI+ and DI- is routed to DOa+, DOa- pin respectively when SEL = 0.
16, 17	DOb+, DOb-	Differential I/O	Differential analog pass-through I/O. Signal from DI+ and DI- is routed to DOb+, DOb- pin respectively when SEL = 1.
30	SEL	3.6V Tolerant Low-voltage Single-ended Input	SEL controls the mux through a flow-through latch.
9, 19, 21, 26, 31, 34, 39, 41	VDD	Power Supply	Power, 3.3V ±10%
18, 20, 22, 25, 29, 35, 38, 40, 42	GND	Power Supply	Power ground

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +3.7V
Channel DC Input Voltage	–0.5V to 1.5V
DC Output Current	120mA
SEL DC Input Voltage	–0.5V to 3.7V
Junction Temperature	125°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	3.3V Power Supply	—	3.0	3.3	3.6	V
I_{DD}	Total Current from V_{DD} 3.3V Supply	SEL = 0V or V_{DD}	0	0.15	1	mA
T_A	Operating Temperature Range	—	-40	—	85	°C

DC Electrical Characteristics (T_A = –40°C to +85°C, V_{DD} = 3.3V ± 10%)

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{IH-SEL}	Input High Level, SEL Input	—	2.0	—	3.6	V
V_{IL-SEL}	Input Low Level, SEL Input	—	0	—	0.8	V
I_{IN_SEL}	Input Leakage Current, SEL Input	Measured with input at VIH-SEL max and VIL-SEL min	–10	—	10	µA
I_{IH}	Input High Current, xI, xO	V_{DD} = Max, V_{IN} = 1.5V	–10	—	10	µA
I_{IL}	Input Low Current, xI, xO	V_{DD} = Max, V_{IN} = 0V	–10	—	10	µA
I_{IH}	Input High Current, SEL	V_{DD} = Max, V_{IN} = V_{DD}	–5	—	5	µA
I_{IL}	Input Low Current, SEL	V_{DD} = Max, V_{IN} = 0V	–5	—	5	µA
I_{OZH}	HighZ High Current xOa, xOb	V_{DD} = Max, V_{IN} = 1.5V	–10	—	10	µA
I_{OZL}	HighZ Low Current xOa, xOb	V_{DD} = Max, V_{IN} = 0V	–10	—	10	µA

Note:

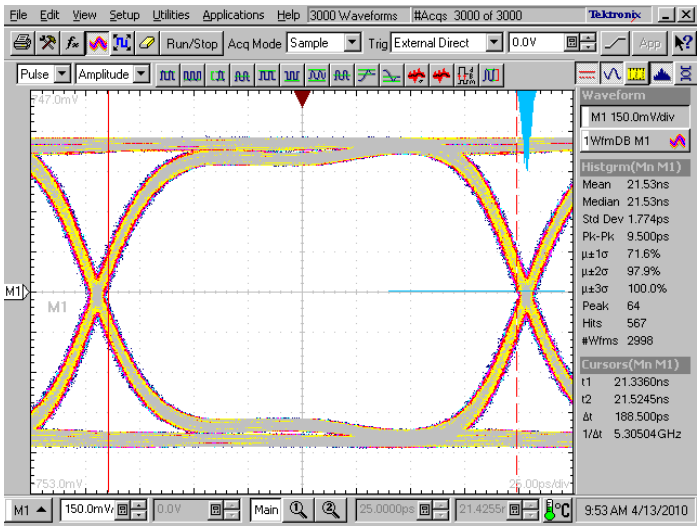
1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics for xI+/-, xOy+/-

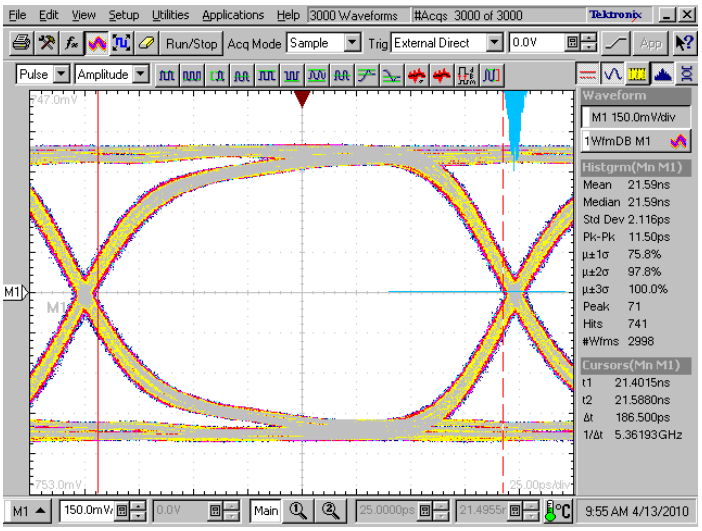
Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
DDIL	Differential Insertion Loss	f = 50MHz -1.25GHz f = 1.25GHz - 2.5GHz f = 2.5GHz - 4GHz f = 5.0GHz	—	-0.8 -1.1 -1.2 -1.7	-1.0 -1.3 -1.5 -2.0	dB
$DDIL_{OFF}$	Differential Off Isolation	f = 0 to 4.0GHz	-25.8 -20.6 -17.6 -15.4	-32.2 -25.8 -22.0 -19.3	—	
DDRL	Differential Return Loss	f = 50MHz - 1.25GHz f = 1.25GHz - 2.5GHz f = 2.5GHz - 4GHz f = 5.0GHz	-18.2 -16.8 -12 -8	-22.7 -21.0 -15.0 -10.0	—	
DDNEXT	Near End Crosstalk	f = 50MHz -1.25GHz f = 1.25GHz - 2.5GHz f = 2.5GHz - 4GHz f = 5.0GHz	-44.8 -41.6 -38.4 -36	-56 -52 -48 -45	—	
BW	Bandwidth -3dB	—	—	8.4	—	GHz

Switching Characteristics

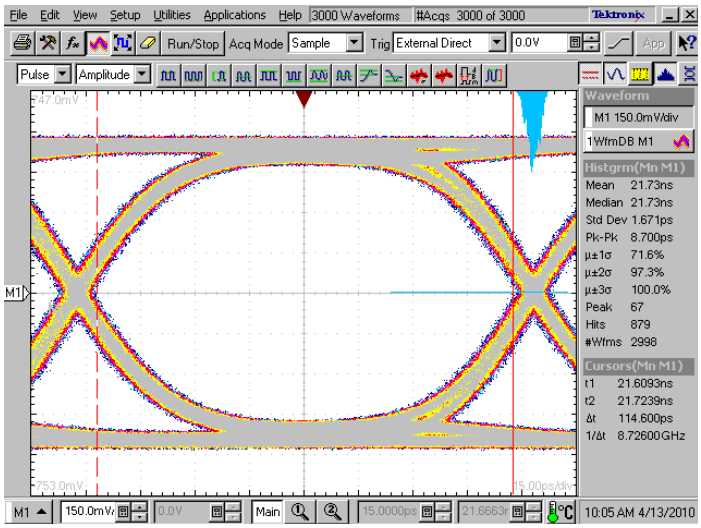
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time - SEL to xI+/-, xOy+/-	See "Test Circuit for Electrical Characteristics"	0.5	15	25	ns
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to xI+/-, xOy+/-	See "Test Circuit for Electrical Characteristics"	0.5	5	25	ns
t_{PLH}	Propagation Delay, LOW to HIGH	—	17	—	36	ps
t_{PHL}	Propagation Delay, HIGH to LOW	—	21	—	39	ps
t_{b-b}	Bit-to-Bit Skew Within Same Differential Pair	See "Test Circuit for Electrical Characteristics"	—	4	10	ps
t_{ch-ch}	Channel-to-Channel Skew	See "Test Circuit for Electrical Characteristics"	—	—	20	ps



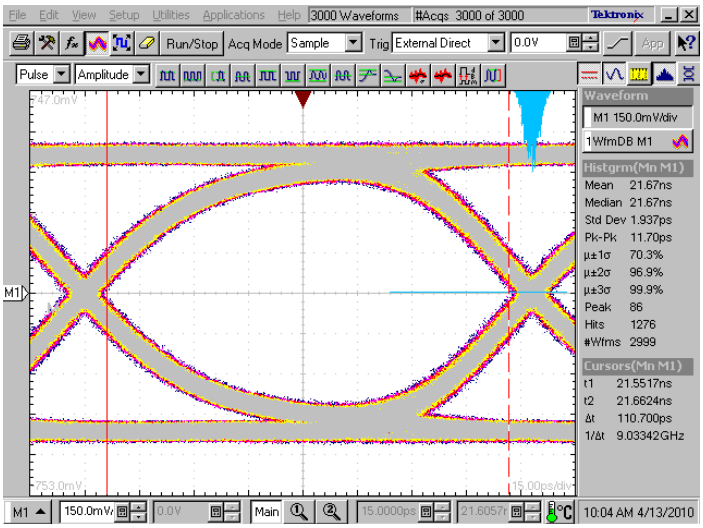
5.0Gbps RX Signal Eye Without PI3PCIE3415A



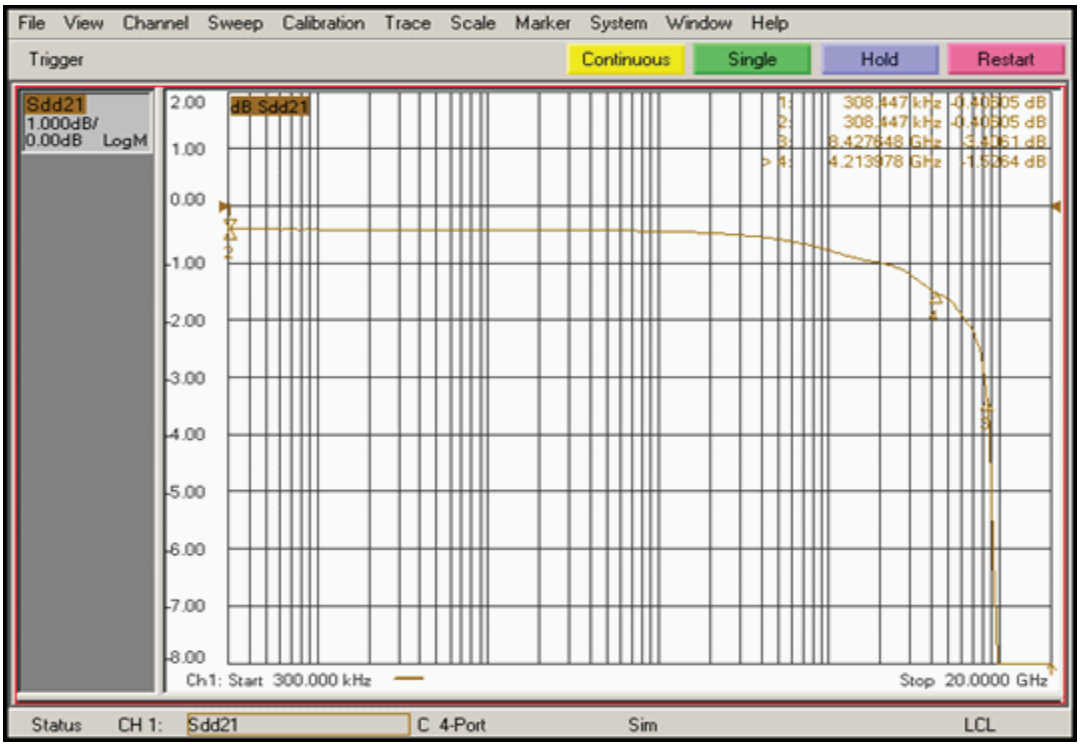
5.0Gbps RX Signal Eye With PI3PCIE3415A



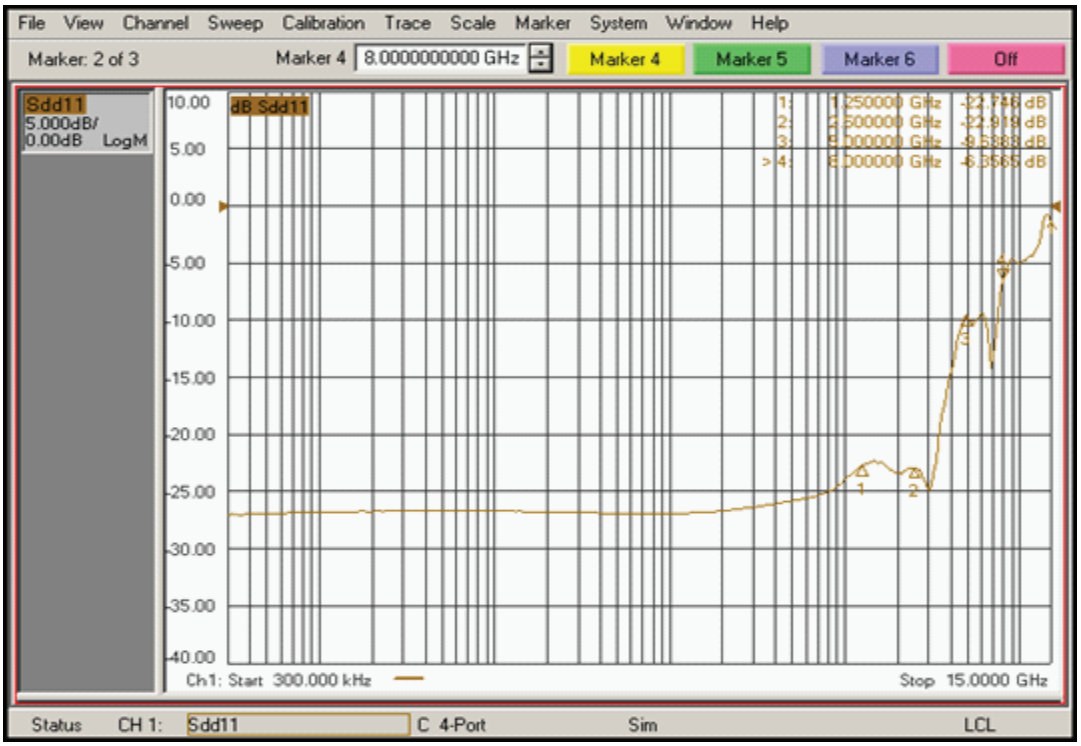
8.0Gbps RX Signal Eye Without PI3PCIE3415A



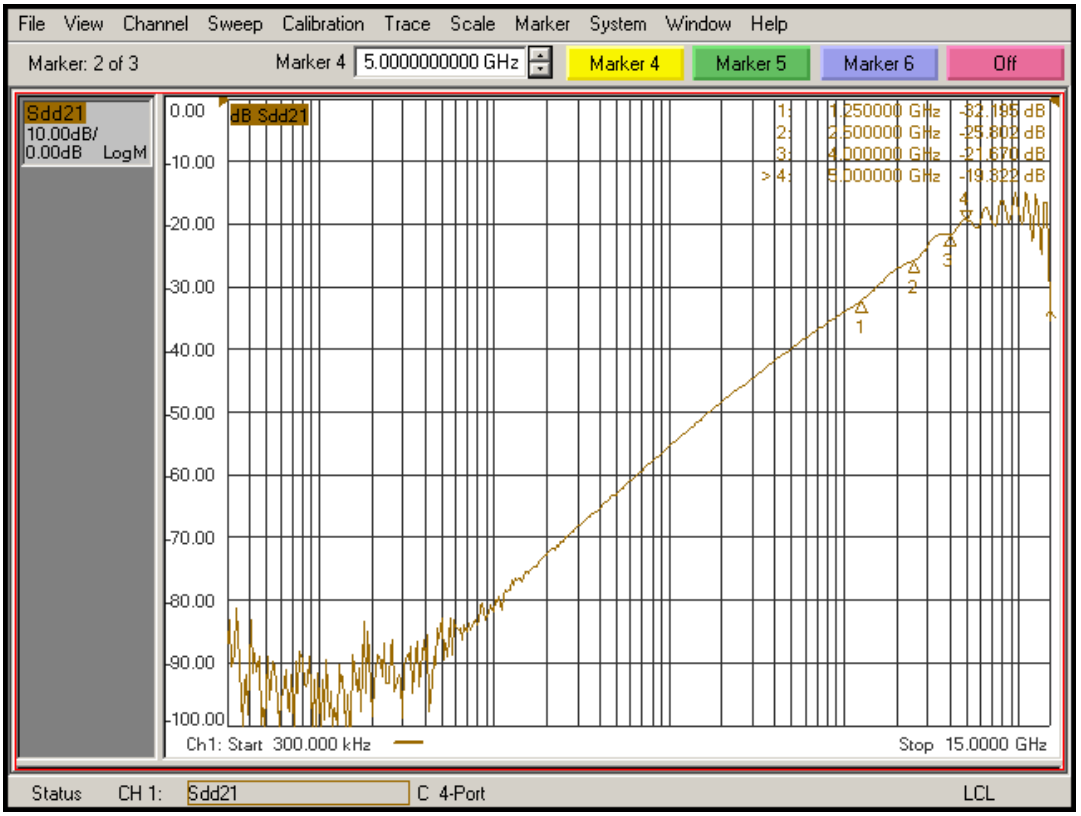
8.0Gbps RX Signal Eye With PI3PCIE3415A



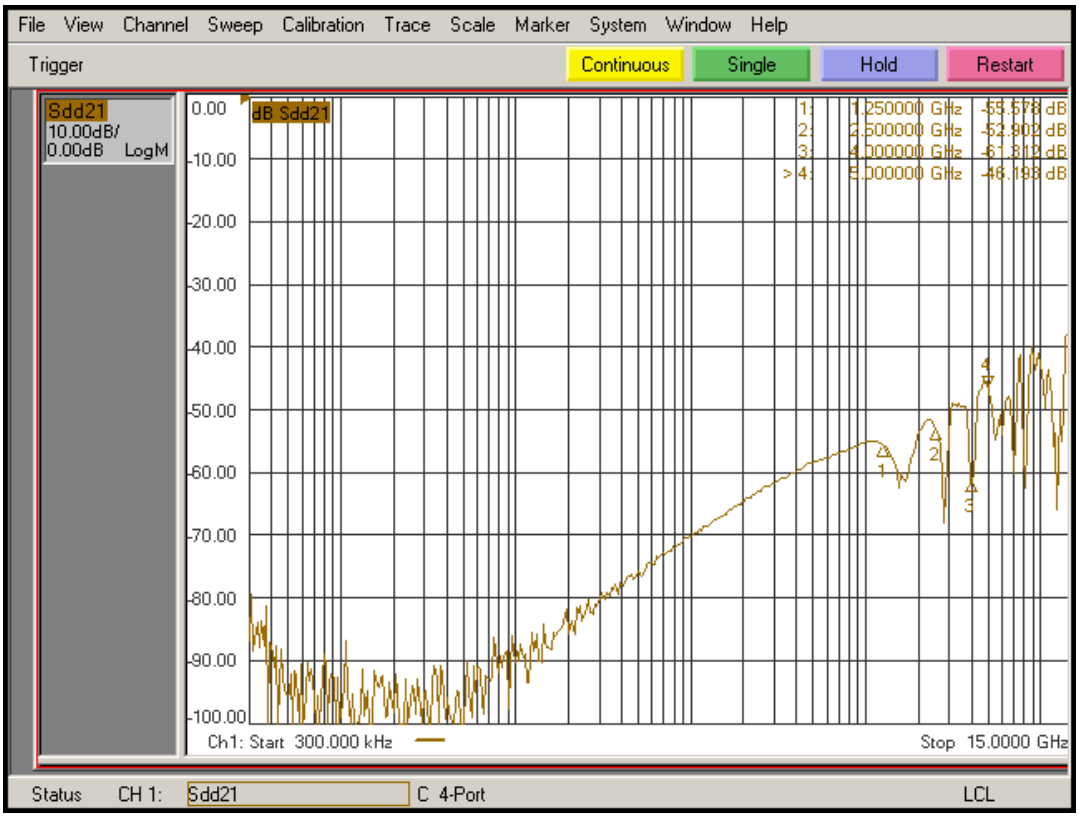
Differential Insertion Loss



Differential Return Loss

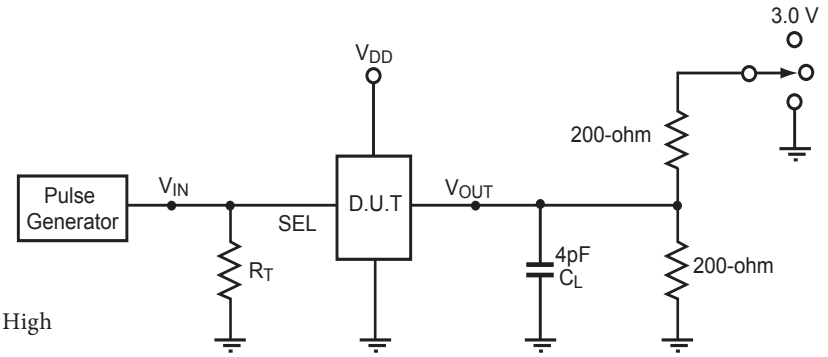


Differential Off Isolation



Differential Crosstalk

Test Circuit for Electrical Characteristics(1-5)



*V_{OUT} = Port 1 or Port 2

tpZH/HZ = COM Port is High

tpLZ/ZL = COM Port is Low

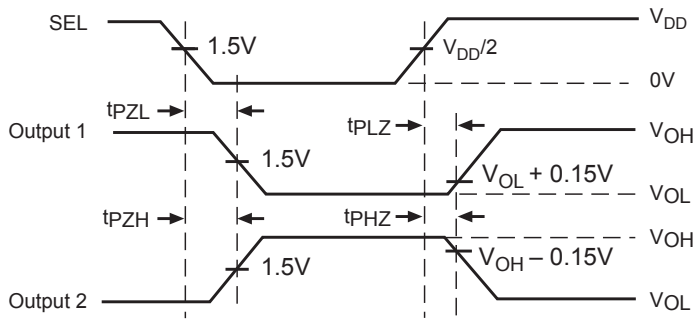
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
5. The outputs are measured one at a time with one transition per measurement.

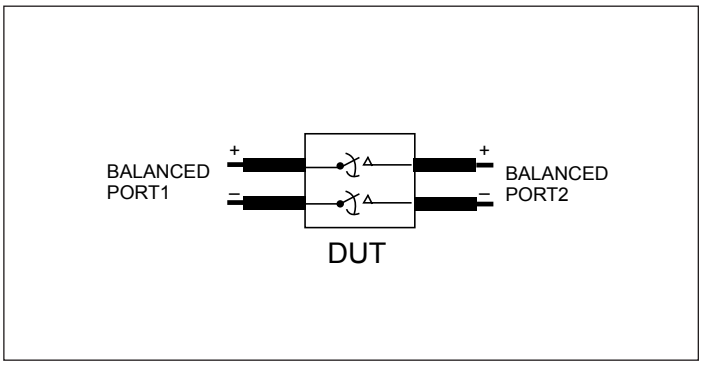
Switch Positions

Test	Switch
t_{PLZ}, t_{PZL}	3.0V
t_{PHZ}, t_{PZH}	GND

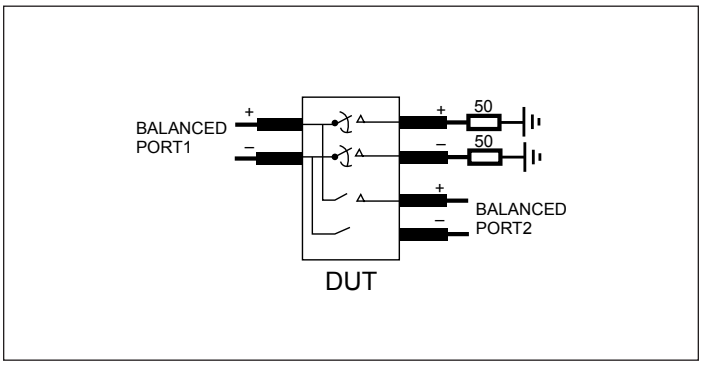
Switching Waveforms



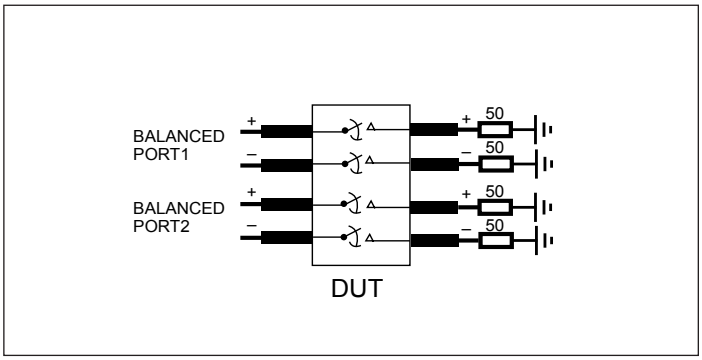
Voltage Waveforms Enable and Disable Times



Differential Insertion Loss and Return Test Circuit



Differential Off Isolation Test Circuit



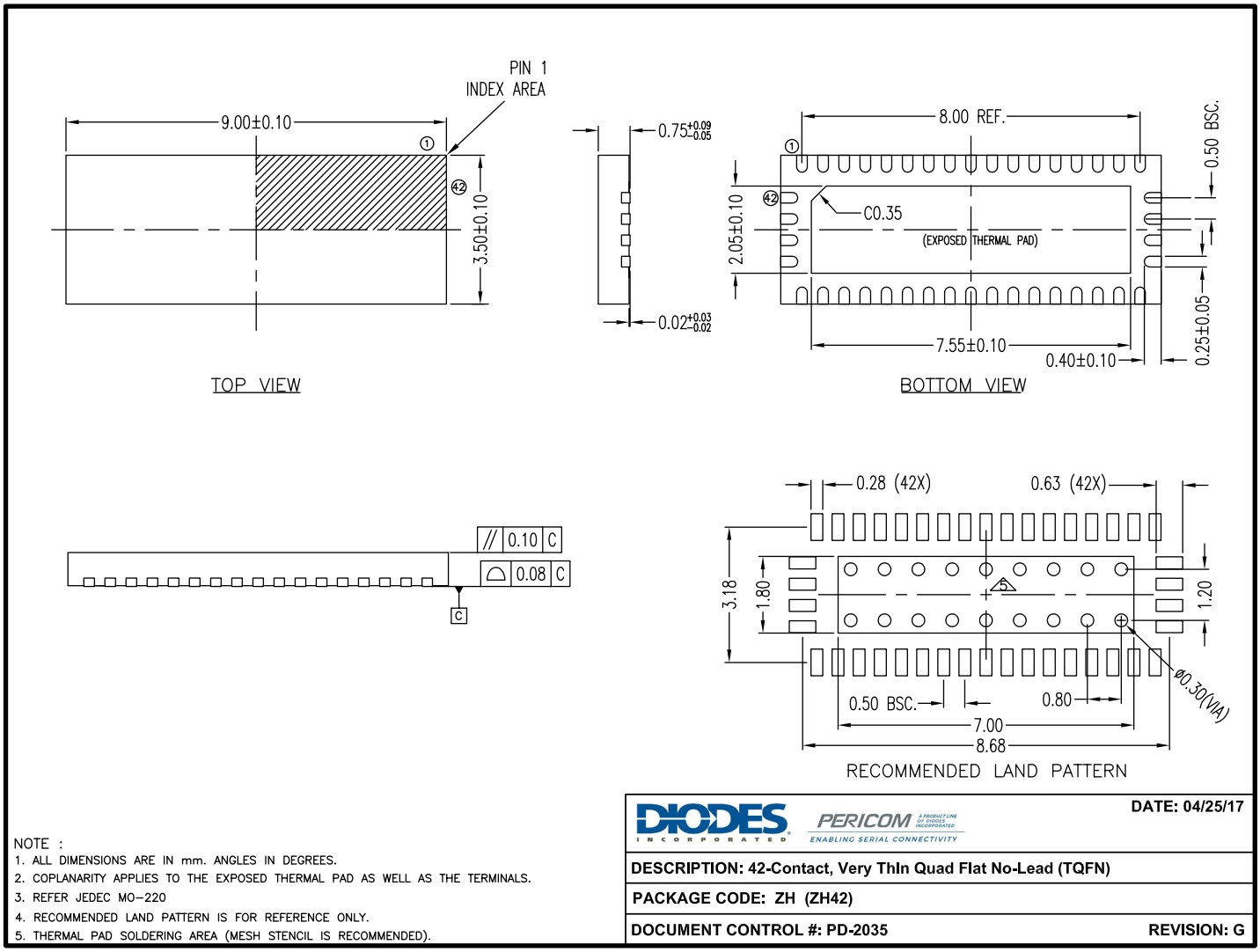
Differential Near End Xtalk Test Circuit

Part Marking

ZH Package

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 42-TQFN (ZH)



17-0266

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE3415AZHEX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN), (width 24mm)
PI3PCIE3415AZHE+DRX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN), (width 16mm)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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