Features

- 4 independent channels
- IEEE802.3af-2003 compliant
- IEEE802.3at-2009 compliant, including two-event classification
- IEEE802.3bt draft 2.0
- Supports Three Event Classification based on PoH
- Drives 2-pairs power ports or 4-pairs ports
- Supports pre-standard PD detection
- Single DC voltage input (32V to 57V)
- Built in 3.3V and 5V regulators
- Input voltage out of range protection
- Wide ambient temperature range: -40°C to +85°C
- On-chip Over-temperature thermal protection and monitoring
- Low power dissipation (0.1Ω sense resistor and 0.2Ω MOSFET Rdson per channel)
- Includes Reset command pin
- 4 x direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable 'PSE Type' AT/AF/BT/PoH modes
- Power soft start mechanism
- Voltage monitoring/protection
- Internal power on reset
- Emergency power management supporting four configurable power bank I/Os
- Advance System Power Management algorithm supports up to 96 physical ports
- Can be cascaded to up to 12 PoE devices (96 ports)
- Easy system implementation of PD69204T4 and PD69208T4 for multiplications of 4 ports systems. i.e. 12 ports system (consist of 1xPD69208T4 and 1xPD69204T4)
- Supports both UART and I^2C interfaces to Host CPU
- Backwards compatible with Microsemi communication protocol used at prior generations
- LED stream support
- System OK indication
- Disable ports input pin
- Software download via I^2C or UART
- Detailed port status
- Programmable threshold temperature alarm limit
- Interrupt out pin for system and port events
- Forced port power ON function
- Port power limit setting
- Port matrix and priority
- Automatic PoE device type detection
- MSL3, RoHS compliant

Applications

- Power over Ethernet (all IEEE compliant 2-pair modes)
- support 4-pair, UPOE (Universal PoE), IEEE802.3bt draft 2.0 and POH
- Switches/Routers/Midspans
- Industrial automation
- PoE for LED lighting

Typical Application

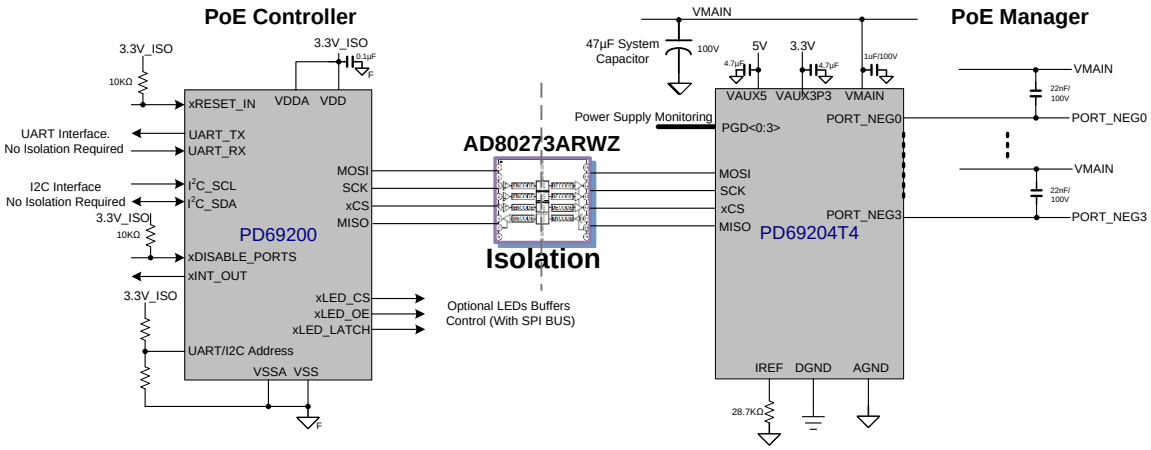


Figure 1: Typical PoE Application

Note: Fuses per port are not required for use in circuits with total power level of up to 3kW as the PD69204T4 designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1

PD69204T4 Absolute maximum ratings

PoE performance is not guaranteed when exceeding the recommended rating . Exposure to any stress in the range between the recommended rating (listed given in the Electrical Characteristics table) and the absolute maximum rating should be limited to a short time period. Exceeding these ratings may impact long-term operating reliability.

Table 1

	Min	Max	Units
Supply Input Voltage (V_{MAIN}) (1) (2)	-0.3	72	V
PORT_NEG[0..3] pins	-0.3	V_{MAIN}+0.5	V
VAUX5	-0.3	6	V
VAUX3P3, DVDD	-0.3	4	V
Digital pins: MISO, MOSI, SCK, CS_N, ADDR[3:0], PGD[3:0], RESET_N, TRIM	-0.3	DVDD + 0.3 and <4.0	V
Junction Temperature		130	°C
Lead Soldering Temperature (40s, reflow)		260	°C
Storage Temperature	-65	130	°C

Note: (1) Power Sequence Requirement: Vmain>VAUX5>VAUX3P3, DVDD.
(2) PD69204T4 EPAD is connected by copper plane on PCB to AGND. AGND is ground for IC.
(3) DRV_VAUX5 is an output pin, do not apply voltage or current. Can be left open when not used.
(4) IREF is an output pin, do not apply voltage or current.

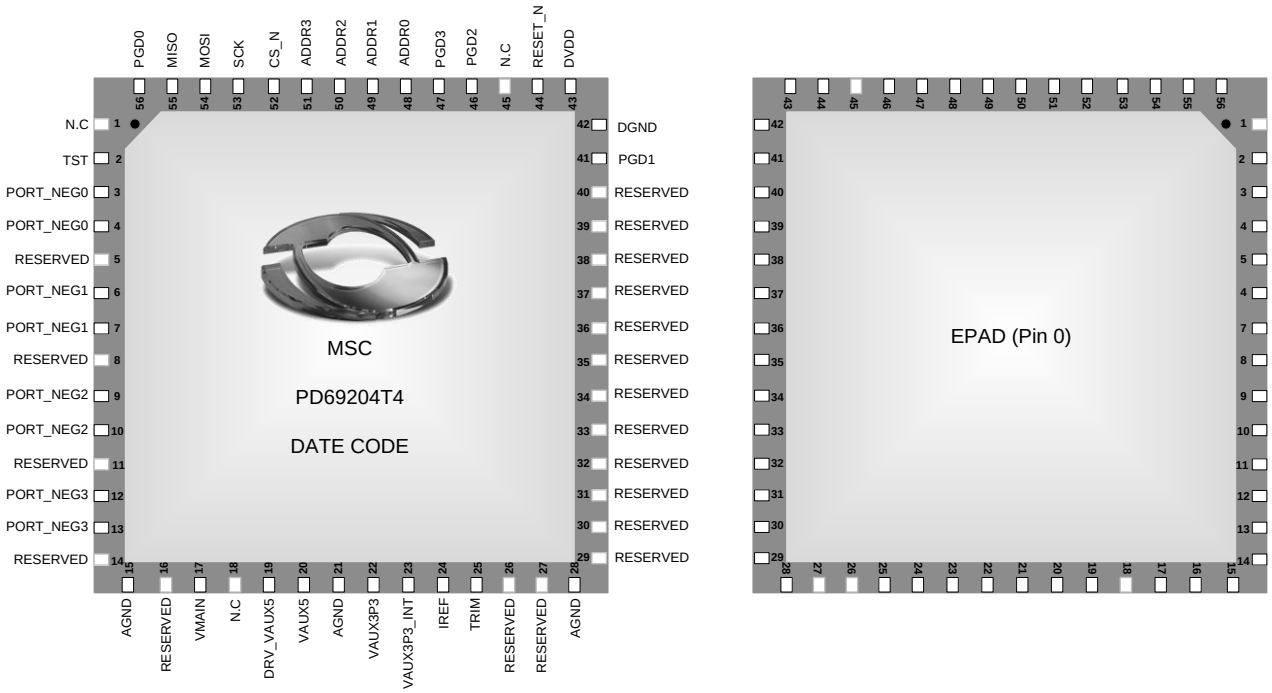
For a detailed electrical specification of PD69200 refer to the following datasheets at **www.freescale.com**

- **Manufacturer**: Freescale
- **Manufacturer part number: MKL15Z128VFM4**

Applicable Documentation

- IEEE 802.3at-2009 standard, DTE Power via MDI
- IEEE802.3bt draft 2.0 standard
- Microsemi, Serial communication protocol user guide , Catalog Number: PD69200_UG_COMM_PROT
- Microsemi , Designing 48-port Enhanced PoE System (802.3af/802.3at Compliant) application note, Catalog Number: PD69208_AN_211
- Microsemi , PoE LED Stream Interface technical note, Catalog Number: PD69200_TN_218
- Microsemi , Design for surge immunity within PSE systems, Catalog Number: PD69208/4_TN_205
- Microsemi , PD69208T4 and PD69200 datasheet, Catalog Number: DS_PD69208T4_PD69200
- Freecale , Kinetis_L MKL15Z128VFM4 datasheet
- Freescale package drawings 98ASA00473D

Pin Configuration and Pinout



TOP VIEW
8×8 QFN – 56L

BOTTOM VIEW
8×8 QFN – 56L

Figure 2: PD69204T4 Pinout

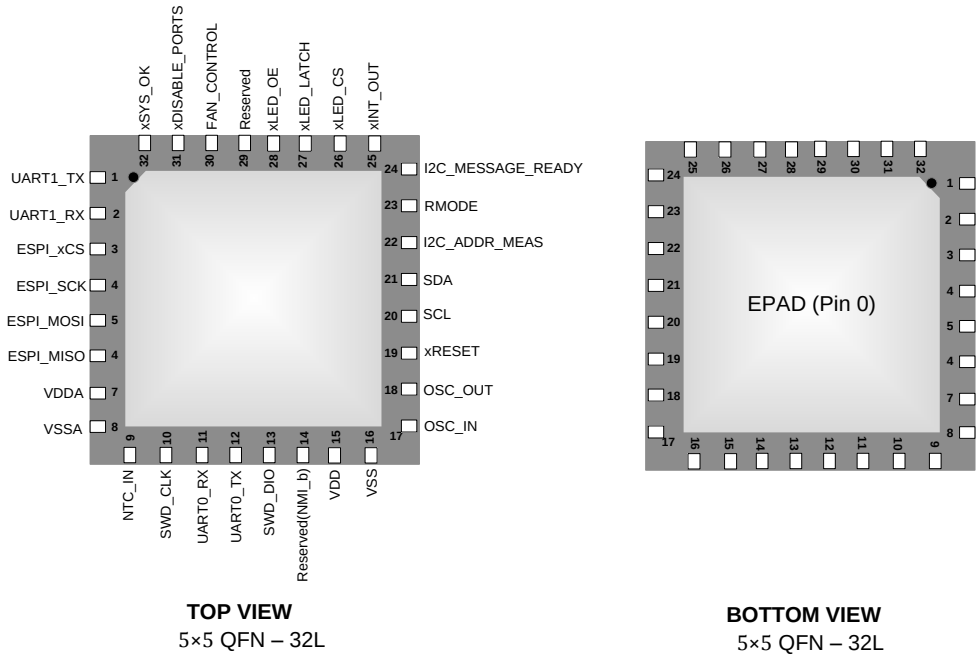
Ordering Information

Table 2

Ambient Temperature	Type	Package	Part Number	Packaging Type	Part Marking
-40 to 85°C	RoHS compliant, Pb-free,MSL3	Plastic QFN 8 mm x 8 mm (56 lead)	PD69204T4ILQ-TR	Tape and Reel	Microsemi Logo PD69204T4 F R e4** YYWWAZZ***

** F R e4
F = FAB Code
R = Product revision code
e4 = 2nd level interconnect

*** YYWWAZZ
YY = Year
WW = Week
A = Assembly location
ZZ = Assembly Lot sequence code



TOP VIEW
5×5 QFN – 32L

BOTTOM VIEW
5×5 QFN – 32L

Figure 3: PD69200 Pinout

Ordering Information

Table 3

Ambient Temperature	Type	Package	Part Number	Packaging Type	Part marking	Tray Marking
-40 to 85°C	RoHS compliant, Pb-free,MSL3	Plastic QFN 5 mm x 5 mm (32 lead)	PD69200D-VVVVSS	Tray	Microsemi Logo Freescale Logo 69200 M15M7V** XXXXX*** YYYYY****	PD69200-VVVVSS PD-OOOOG3bb* YYWW

Note:

1. *MKTG Product Type / **V**ersion / **S**W Parameters / **O**peration P/N
2. For latest firmware version available, refer to Microsemi's website or Customer Care Support.
3. Initial burning of controller's firmware is performed in factory. Firmware upgrades can be performed by users using communication interface (see TN-140 ,Catalog Number: 06-0024-081).
4. ** Short part number, *** Mask set, **** Date code

PD69204T4 Pin Description

Table 4

Pin Number	Pin Designator	Pin Type	Description
0	**EPAD**		Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin whenever possible (refer to PD69208 Layout Design Guidelines in the HW app note, Catalog Number: PD69208_AN_211).
1	**N.C**	N/A	Not connected; do not connect externally (leave floating).
2	**TST**	Digital Input	Test pin for production use only. Keep connected to DGND.
3	**VPORT_NEG0**	Analog I/O	Negative port0 output.
4	**VPORT_NEG0**	Analog I/O	Negative port0 output.
5	**RESERVED**	N/A	Reserved Pin. do not connect externally.
6	**VPORT_NEG1**	Analog I/O	Negative port1 output.
7	**VPORT_NEG1**	Analog I/O	Negative port1 output.
8	**RESERVED**	N/A	Reserved Pin. do not connect externally.
9	**VPORT_NEG2**	Analog I/O	Negative port2 output.
10	**VPORT_NEG2**	Analog I/O	Negative port2 output.
11	**RESERVED**	N/A	Reserved Pin. do not connect externally.
12	**VPORT_NEG3**	Analog I/O	Negative port3 output.
13	**VPORT_NEG3**	Analog I/O	Negative port3 output.
14	**RESERVED**	N/A	Reserved Pin. do not connect externally.
15	**AGND**	Power	Analog ground.
16	**RESERVED**	N/A	Reserved Pin. do not connect externally.
17	**VMAIN**	Power	Main High Voltage Supply voltage. A low ESR 1µF (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
18	**N.C**	N/A	not connected. do not connect externally.
19	**DRV_VAUX5**	Power	Driven outputs for 5 V external regulation; if internal regulation is used, connect to pin 20. If an external NPN is used to regulate the voltage, connect this pin to "Base".

20	**VAUX5**	Power	Regulated 5 V output voltage source; A 4.7µF or higher filtering capacitor should be connected between this pin and AGND. If an external NPN is used to regulate the voltage, connect this pin to the "Emitter" (the "collector" should be connected to V_{main}).
21	**AGND**	Power	Analog ground.
22	**VAUX3P3**	Power	Regulated 3.3V output voltage source. A 4.7 µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 V regulator is used, connect it to this pin to supply the chip.
23	**VAUX3P3_INT**	Power	Connected to VAUX3P3 (pin 22) if internal 3.3 V regulator is used. Leave unconnected (Floating) if external 3.3V regulator is used.
24	**IREF**	Analog Input	Reference resistor pin. Connect a 28.7kΩ 1% resistor to AGND. Use 0.1% resistor in PoH applications
25	**TRIM**	Test Input	Test Input pin; Keep Connected to VAUX3P3.
26	**RESERVED**	N/A	Reserved Pin. do not connect externally.
27	**RESERVED**	N/A	Reserved Pin. do not connect externally.
28	**AGND**	Power	Analog ground.
29	**RESERVED**	N/A	Reserved Pin. do not connect externally.
30	**RESERVED**	N/A	Reserved Pin. do not connect externally.
31	**RESERVED**	N/A	Reserved Pin. do not connect externally.
32	**RESERVED**	N/A	Reserved Pin. do not connect externally.
33	**RESERVED**	N/A	Reserved Pin. do not connect externally.
34	**RESERVED**	N/A	Reserved Pin. do not connect externally.
35	**RESERVED**	N/A	Reserved Pin. do not connect externally.
36	**RESERVED**	N/A	Reserved Pin. do not connect externally.
37	**RESERVED**	N/A	Reserved Pin. do not connect externally.
38	**RESERVED**	N/A	Reserved Pin. do not connect externally.
39	**RESERVED**	N/A	Reserved Pin. do not connect externally.
40	**RESERVED**	N/A	Reserved Pin. do not connect externally.
41	**PGD1**	Digital I/O	Power good input from system power supply.
42	**DGND**	Power	Digital Ground.

43	**DVDD**	Power In	Regulated 3.3V for digital circuitry. Connect voltage from pin VAUX3P3 or from external power supply source if used. A 1 µF or higher filtering capacitor should be connected between this pin and DGND.
44	**RESET_N**	Digital Input	Reset input – active low ('0' = reset). An external 10K pull-up resistor should be connected between this pin and DVDD.
45	**N.C**	N/A	not connected. do not connect externally.
46	**PGD2**	Digital Input	Power good input from system power supply.
47	**PGD3**	Digital Input	Power good input from system power supply.
48	**ADDR0**	Digital Input	SPI Address Bit 0 to set chip address.
49	**ADDR1**	Digital Input	SPI Address Bit 1 to set chip address.
50	**ADDR2**	Digital Input	SPI Address Bit 2 to set chip address.
51	**ADDR3**	Digital Input	SPI Address Bit 3 to set chip address.
52	**CS_N**	Digital Input	SPI bus, chip select.
53	**SCK**	Digital Input	SPI bus, Serial clock Input.
54	**MOSI**	Digital Input	SPI bus, Master Data out/slave in.
55	**MISO**	Digital Output	SPI bus, Master Data in/slave out.
56	**PGD0**	Digital Input	Power good input from system power supply.

PD69200 Pin Description

Table 5

Pin Number	Pin Designator	PIN TYPE	PIN DESCRIPTION
0	**EPAD**	Thermal	Isolated Thermal PAD, recommended to tie to GND.
1	**UART1 TX**	OUT***	Reserved UART.
2	**UART1 RX**	IN***	Reserved UART.
3	**ESPI_xCS**	OUT	ESPI Bus to PoE Manager. SPI chip select (Active Low). CS will be asserted during all SPI frame.
4	**ESPI_SCK**	OUT	ESPI Bus to PoE Manager. SPI clock output to PD6920x, and LED stream clock output, set to 1MHz.
5	**ESPI_MOSI**	OUT	ESPI Bus to PoE Manager. SPI Master Out Slave In. SPI packets will be transmitted on this line.
6	**ESPI_MISO**	IN	ESPI Bus to PoE Manager. SPI Master In Slave Out. SPI packets will be received on this line.
7	**VDDA**	Supply	Main Supply 3.3v.
8	**VSSA**	GND	Analog ground.
9	**Analog Input**	Analog_IN	Analog input. Should be connected to 3.3v.
10	**SWD_CLK**	DEBUG	Serial Debug Data Bus Clock.
11	**UART0_RX**	IN***	UART receive from host. 15 byte protocol commands are received on this line. The baud rate is set to 19200bps. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD69200_UG_COMM_PROT).
12	**UART0_TX**	OUT***	UART transmit to host. 15 byte protocol reply / telemetry are transmitted on this line. The baud rate is set to 19200bps. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD69200_UG_COMM_PROT).
13	**SWD_DIO**	DEBUG	Serial Debug Data Bus.
14	**PTA4 (NMI_b)**	IRQ_Input	Spare, Ext Pull Up . must be connected.
15	**VDD**	Supply	Main Supply 3.3v.
16	**VSS**	GND	Digital ground.

Pin Number	Pin Designator	PIN TYPE	PIN DESCRIPTION
17	**EXTAL0**	Oscillator*	Oscillator input – Reserved.
18	**XTAL0**	Oscillator*	Oscillator output – Reserved.
19	**xRESET**	IN/OUT**	Host Reset input (Active Low). • The shortest reset pulse from the host that is required for the PD69200 application is 150uSec. • PD69200 can generate self-reset. In this case xRESET pin is driven low by the PD69200 for about 100uSec. • It is recommended to connect this pin to a host open drain output with 10Kohm pullup. • An 47nF filter capacitor should be connected between this pin to GND, close to the PD69200 device. • If this pin is connected to a push/pull driver, a serial resistor of 1.5Kohm must be connected instead of the pullup. The required shortest reset pulse in this case is 300uSec. For more information about this pin connectivity refer to HW app note, Catalog Number: PD69208_AN_211.
20	**I2C0_SCL**	IN/OUT**	I^2C Clock from host master. Speed is limited to 400KHz and clock stretching functionality must be implemented in the Host Master (If the PD69200 is busy it will hold the clock line).
21	**I2C0_SDA**	IN/OUT**	I^2C bidirectional data. 15 byte protocol messages are transmitted on this line (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD62000_UG_COMM_PROT).
22	**I2C_ADDR_Meas**	Analog_IN	I^2C address of PD69200. Analog input to determine I^2C address or UART operation. See I^2C address selection in Table 12.
23	**Analog Input**	Analog_IN	Reserved Analog input. connect to GND.
24	**xI2C_Message_Ready**	OUT	I^2C Message Ready for read by the Host. PD69200 will assert low this line when it has an answer to the host. This way, the host can poll this line and initiate I^2C read cycle only when the message is ready. (This pin is active low).

Pin Number	Pin Designator	PIN TYPE	PIN DESCRIPTION
25	**xInt_Out**	OUT **	Interrupt output indication. This line is asserted low when a pre-configured event is happening. The host configure (through 15 bytes protocol) which event will generate an interrupt. When this event occurs, the xInt_Out is asserted. (This pin is active low).
26	**xLed_CS**	OUT	Chip select signal for LED stream (This pin is active low).
27	**xLED_Latch**	OUT	Latch signal for LED stream (This pin is active low).
28	**xLED_OE**	OUT	Output enable signal for LED stream (This pin is active low).
29	**Reserved**	IN	Reserved for MPRPD counter (future support). If not used, Connect to VDD.
30	**Fan_Control**	OUT	Optional FAN control to operate a FAN in case that any PD69204T4 device temperature is above the temperature alarm threshold. (This pin is active high).
31	**xDisable_Ports**	IN	Disable all PoE Ports. When this input is asserted low, the PD69200 shutdown all the PoE ports in the system. This pin contains software filter of 480mSec to reject noise and false disable scenarios.
32	**xSys_OK / LED System OK**	OUT	System validity indication, when system is OK pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0x28). The mask default settings is 0, means this pin indicates valid software and Vmain is in Range. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD69200_UG_COMM_PROT). (This pin is active low).

Note:

1. *The oscillator pins are reserved and unused. The MCU uses internal clock source set to 47.972MHz +/- 1.5%(max)
2. ** Open drain output, requires external pullup. Refer to HW app note : PD69208_AN_211 document
3. *** Weak pullup is recommended. Refer to PD69208_AN_211 document
4. All I/Os in this application can sink or source 3mA maximum
5. Initial "x" indicate pin active low

Microsemi

PD69204T4 Thermal Properties

Table 6

Thermal Resistance	Typ	Units	Notes
θ_{JA}	25	°C/W	Mount on PCB of 76x114mm
θ_{JL}	0.5	°C/W	Junction to thermal pad
θ_{JC}	1	°C/W	Junction to top case

Note: θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of PCB construction. Stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

PD69204T4 Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25°C ambient.

Table 7

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{MAIN}	Main Supply Voltage	Supports Full IEEE802.3af/at/bt functionality	32		57	V
V_{PORT_NEGx}	Port Output	V_{MAIN}- V_{PORT_NEGx}	0		57	V
I_Q	Quiescent Current	V_{MAIN}≤8V			100	µA
I_{MAIN}		Main Power Supply Current @ Operating Mode. V_{MAIN}=55V		14		mA
V_{AUX5}	5V Output Voltage	V_{AUX5}-AGND	4.5	5	5.5	V
V_{AUX3P3}	3.3V Output Voltage	V_{AUX3P3}-AGND	3	3.3	3.6	V
I_{AUX3P3}	3.3V Output Current	Without external NPN			5	mA
		With external NPN transistor on VAUX5			30	mA
V_{AUX3P3_IN}	3.3V Input Voltage	V_{AUX3P3}-AGND	3	3.3	3.6	V
DV_{DD}	Digital 3.3V Input Voltage	DV_{DD}-DGND	3	3.3	3.6	V
POR_{TP}	Power On Reset DV_{DD} Trip Point	DV_{DD}-DGND	2.575	2.775	2.975	V

POR_{HYS}	Power On Reset DV_{DD} Hysteresis	POR_{TP}-DGND	0.2	0.25	0.3	V
R_{CH_ON}	Total Channel Resistance	$R_{ds\_on} + R_{sense} + R_{bonding}$		0.34		Ω
Detection						
V_{OC}	Pre Detection Voltage, Open Circuit Voltage	V_{MAIN}- V_{PORT_NEGx}, open port			7.8	V
V_{VALID}	Detection Voltage	V_{MAIN}- V_{PORT_NEGx}, for IEEE802.3 compliant signature resistance (R_{SIG}<33K)			9.3	V
I_{SC}	Short Circuit Current	V_{MAIN}- V_{PORT_NEGx}=0V		388	408	µA
R_{SIG_LOW}	Minimum Valid Detection Resistance		15		19	KΩ
R_{SIG_HIGH}	Maximum Valid Detection Resistance		26.5		33	KΩ
Classification						
V_{CLASS}	Class Event Output Voltage	V_{MAIN}- V_{PORT_NEGx}; 0mA≤ IPORT≤50mA	15.5	18	20.5	V
V_{MARK}	Mark Event Output Voltage	V_{MAIN}- V_{PORT_NEGx} ; 0.1mA≤ IPORT≤5mA	7	8.5	10	V
I_{CLASS_LIM}	Class event current limitation	V_{MAIN}- V_{PORT_NEGx}=0V	51	70	100	mA
I_{MARK_LIM}	Mark event current limitation	V_{MAIN}- V_{PORT_NEGx}=0V	51	70	100	mA
	Classification Current Thresholds	Class 0 Class 1 Class 2 Class 3 Class 4 Class Error	0 8 16 25 35 51		5 13 21 31 45 100	mA
Port Real Time Protection						
T_{RISE}	Turn on rise time	From 10 % to 90 % of the voltage difference at the VPORT_NEGx in POWER_ON state from the beginning of POWER_UP	15			µS

I_{INRUSH}	Output current in POWER_UP state	C_{LOAD} ≤180µF (Note 1)	400	425	450	mA
T_{INRUSH}	Inrush Time				65	mS
I_{PORT}	Output Operating Current	802.3af 802.3at PoH	10 10 10		360 627 967	mA
I_{CUT}	Overload Current	802.3af 802.3at PoH (Note 2)		375 645 995		mA
T_{CUT}	Overload Time Limit		62	64	66	mS
I_{LIM}	Port Current Limit	802.3af 802.3at , 802.3bt Type 3 802.3bt Type 4	400 702 990	425 850 1150	450 892 1300	mA
T_{LIM}	Port Current Limit Time	V_{MAIN}- V_{PORT_NEGx}<30V	1	2	3	mS
I_{UDL}	DC Disconnect Under-load Current	2 Pairs	5	7.5	10	mA
		4 Pairs (for each 2 pair)	2.5	3.75	5	mA
T_{MPDO}	PD Maintain Power Signature Dropout Time Limit		322	324	326	mS
T_{MPS}	PD Maintain Power Signature Time For Validity		46	48	50	mS
T_{OFF}	Turn Off Time	From V_{MAIN} to 2.8V			500	mS
Port Current Monitoring						
	Resolution	Reported as 14 Bits		10		Bits
	LSB			122.07		µA
	Measurement Period			16		mS
	Accuracy	50mA < I_{PORT} < 150mA 150mA < I_{PORT} < 350mA I_{PORT}>350mA			9 4.5 3.5	%
Port Voltage Monitoring						
	Resolution			10		Bits
	LSB			58.6		mV
	Measurement Period			3		mS
	Accuracy				3.3	%

Main Voltage Monitoring						
	Resolution			10		Bits
	LSB			58.6		mV
	Measurement Period			3		mS
	Accuracy	42v < V_{MAIN} < 50v 50v < V_{MAIN} < 57v			3 2.2	%
Temperature Monitoring						
	Resolution			8		Bits
	LSB	Temperature=(DATA x 1.9384)-277		1.9384		°C
	Measurement Period			3		mS
	Accuracy		-3		3	°C
Digital Interface						
V_{IH}	Input Logic High Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	2.2			V
V_{IL}	Input Logic Low Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]			0.8	V
Hyst	Input Logic Hysteresis Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	0.4	0.6	0.8	V
I_{IH}	Input Logic High Current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	-10		10	µA
I_{IL}	Input Logic Low Current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	-10		10	µA
V_{OH}	Output Logic High Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I_{OH} = -1mA	2.4			V
V_{OL}	Output Logic Low Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I_{OH} = 1mA			0.4	V
Immunity						
ESD	ESD rating	HBM	-2		2	KV
Surge	lightning surge (3)	EN61000 4-5	-1		1	KV

Note:

1. Can be overridden by communication command.
2. Port Power is limited to maximum 100W according to UL's LPS requirements. (Port Power= IPORT x VMAIN)
3. System level common mode 10/700 according to IEC61000-4-5 without external components.

PD69200 Electrical Characteristics

In this application PD69200 consumption is ~20mA.
For a detailed electrical specification refer to the following datasheets at **www.freescale.com**

- **Manufacturer**: Freescale
- **Manufacturer part number**: MKL15Z128VFM4
- Maximum pull-ups consumption based on PD69200 application is 2mA.
  Refer to HW app note document : catalog number PD69208_AN_211

PD69200 Main Features Description

Table 8

Function	Description
Supports up to 12 PoE devices – 48 physical ports (24 logical)	Up to 12 PoE devices can be cascaded, fitting into a 48 physical port PoE system that utilizes one PoE controller (PD69200). PD69200 can support up to 24 logical ports. A logical port can be built from 2xPhysical ports or 1xPhysical port.
Power Management	The system supports three power management modes: Class (LLDP) mode, Dynamic mode and Static mode.
Threshold Configuration	Configure overvoltage and under-voltage thresholds for disconnection purposes.
High power ports, 2 pairs or 4 pairs	PoE devices can be configured (both hardware and software) to enable higher current through ports (up to ~950mA) or double power at the RJ in case of 4 pairs.
Communication	Supports both I^2C and UART interfaces with Host CPU.
Legacy (Reduced capacitance) Detection	Enables detection and powering of pre-standard devices (PDs) up to 130uF.
LED Stream	Direct SPI interface to an external LED stream circuitry. Enables designers to implement a simple LED circuit that does not require a software code. (LED stream clock frequency is 1MHz)
System OK Indication	Digital output pin to Host. System validity indication, when system is OK pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0x28). The mask default settings is 0, means this pin indicates valid software and V_{main} is in Range. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD62000_UG_COMM_PROT) (This pin is active low)
System and Port Measurements	Measurements of the following parameters: Current (mA), Power Consumption (W), V_{main} (V), Port Voltage (V), PD Class (0-4).
Detailed Port Status	Port statuses are received from PoE managers. Statuses such as ‘port on’ and ‘port off due to disconnection or due to overload.
Interrupt Pin	Interrupt out from PoE controller, PD69200, indicating events such as: port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events refer to For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD62000_UG_COMM_PROT)
Port Power Limit	Configurable port power limit; when a port exceeds the limit, it is automatically disconnected
Port Matrix Control	Enables layout designers to connect any physical port to any logical port as required.
‘Power Good’ Interrupt from Power Supply directly to PoE Drivers.	For systems comprising more than a single power supply, in case one power supply fails, a fast port disconnection mechanism is executed to maintain operation and prevent collapse of other power supplies.

PD69204T4 Package Outline Drawing 56 Pin QFN 8x8 mm

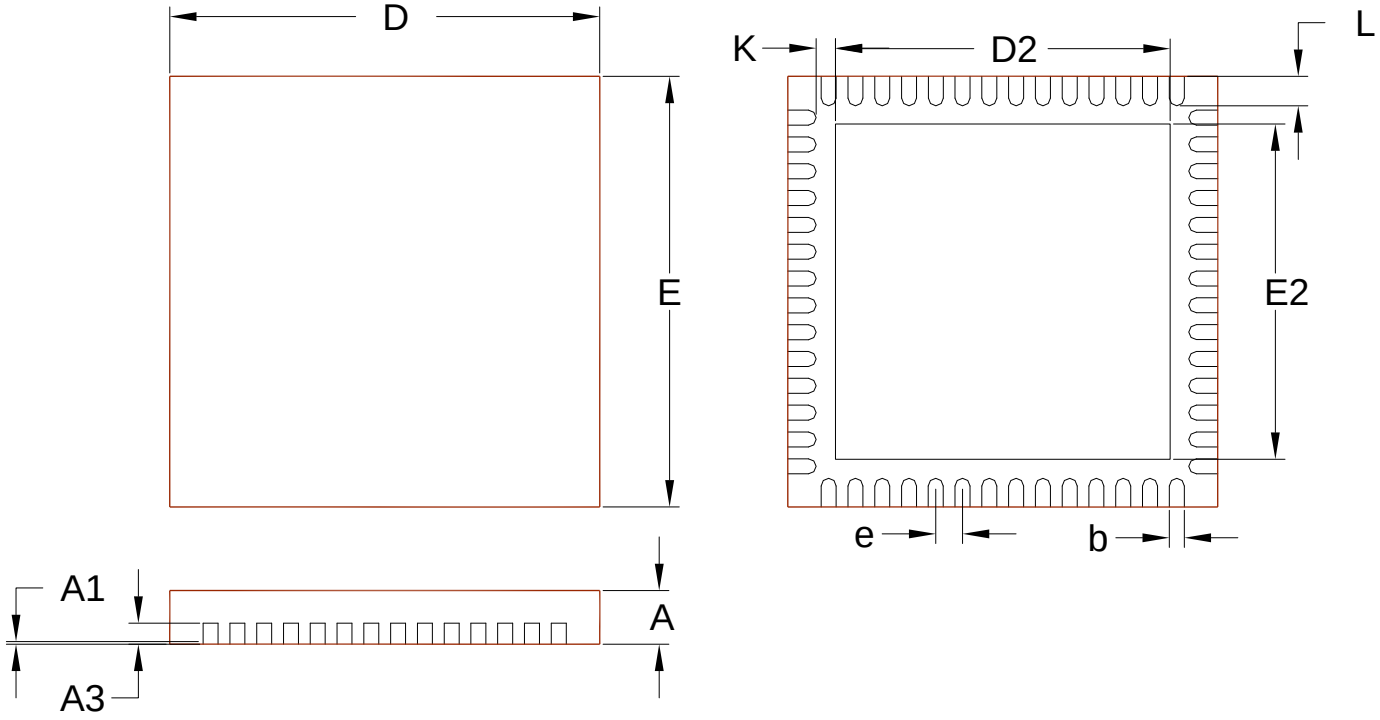


Figure 4 : PD69204T4 Package Outline Drawing

Table 9

Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

PD69200 Package Outline Drawing 32 Pin QFN 5x5 mm

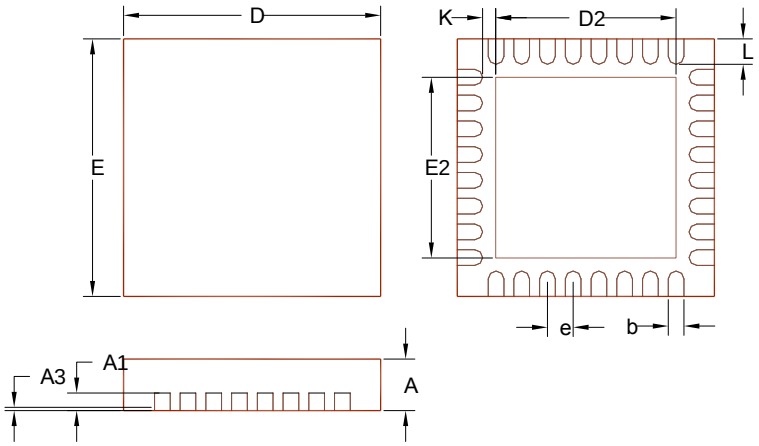


Figure 5 : PD69200 Package Outline Drawing

Table 10

Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC		0.197 BSC	
E	5.00 BSC		0.197 BSC	

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

PD69204T4 Recommended PCB layout for 56 Pin QFN 8x8 mm

Recommended PCB layout pattern for PD69204T4 is described in the following three figures.

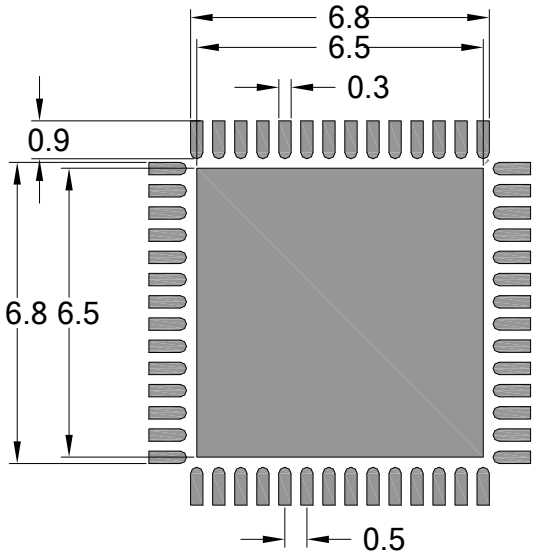


Figure 6: PD69204T4 Top layer Copper Recommended PCB Layout (mm)

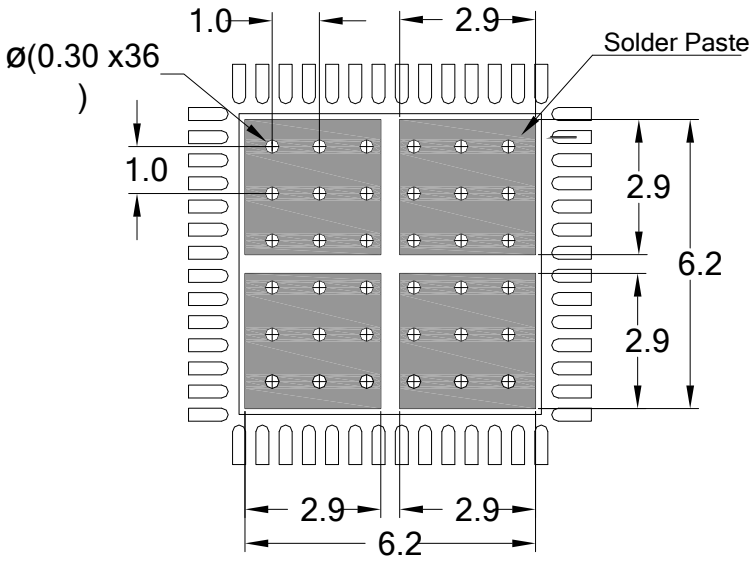


Figure 7: PD69204T4 Top layer Solder Paste and Vias Recommended PCB Layout for Thermal Pad Array (mm)

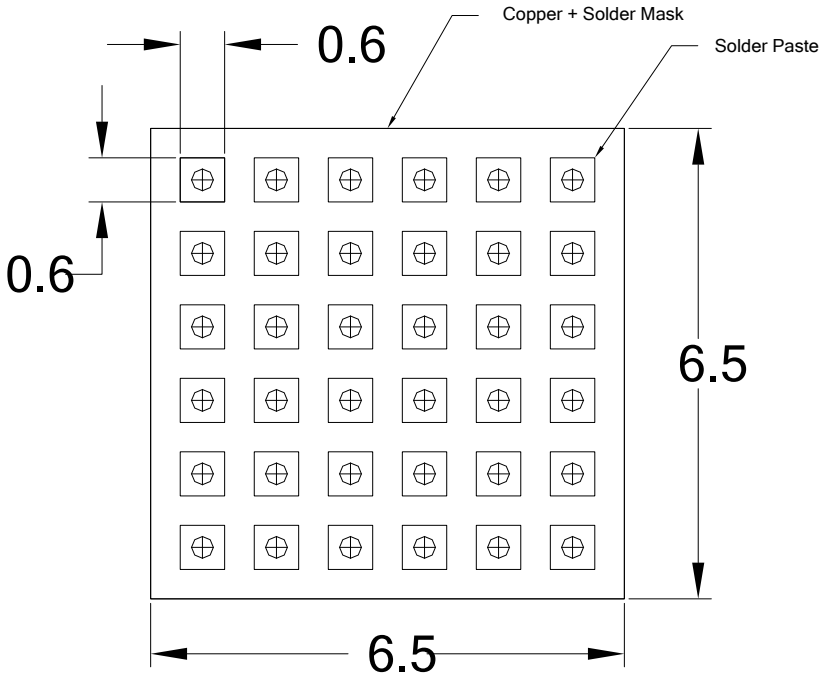


Figure 8: PD69204T4 Bottom layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)

PD69200 Recommended PCB layout for 32 Pin QFN 5x5 mm

Recommended PCB layout pattern for PD69200 is described in the following two figures.

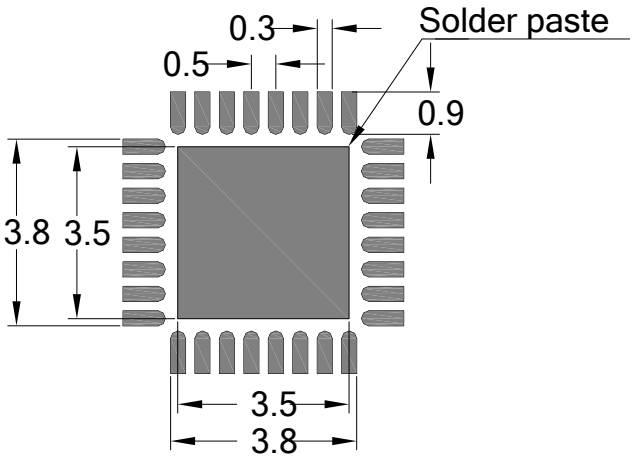


Figure 9: PD69200 Top layer Copper Recommended PCB Layout (mm)

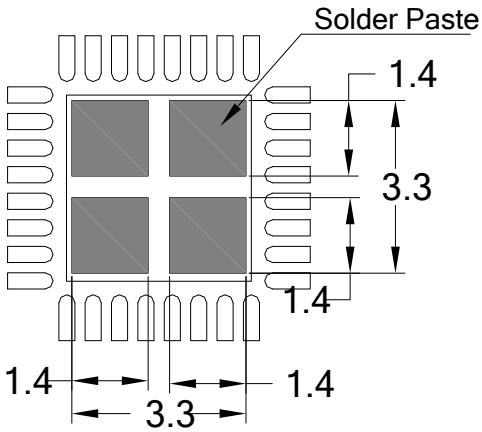


Figure 10: PD69200 Top layer Solder Paste and Vias Recommended PCB Layout for Thermal Pad Array (mm)

Recommended Solder Reflow Information

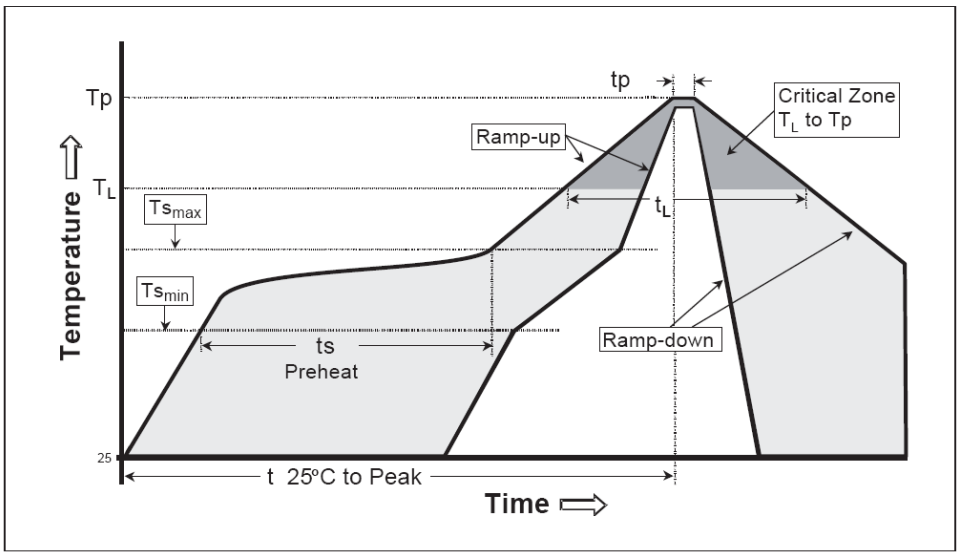
RoHS 6/6
Pb-free 100% Matte Tin Finish
Package Peak Temperature for Solder Reflow 260°C (+0°C, -5°C)
(40 seconds maximum exposure)

IPC/JEDEC J-STD-020C

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



Classification Reflow Profile

Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.

Note: Exceeding these ratings may cause damage to the device.

Application Information

PD69204T4 performs IEEE802.3af, IEEE802.3at and IEEE802.3bt functionality, as well as legacy (capacitor) and pre standard PDs detection. Moreover it includes additional protections such as short circuit and dV/dT protection upon startup.

PD Detection

The PD Detection feature detects a valid AF or AT load, as specified in the AF / AT standard. PD detection is based on four different voltage levels generated over PD (the load) as illustrated in Figure 12.

Legacy (Reduced Capacitor) Detection

In cases where legacy is set, PD Detection mechanism detects and powers up legacy PDs as well as AF/AT compliant PDs. This mechanism is designed to detect and power up pre standard legacy PDs.

Classification

The classification process takes place immediately after PD detection is successfully completed. The goal of the classification process is to detect PD class, as specified in IEEE802.3 standards.

In AF mode, the classification mechanism is based on a single voltage level (single event).

In AT and BT modes, the classification mechanism is based on two voltage levels (multiple events) as defined in IEEE802.3at-2009 and IEEE802.3bt.

In PoH mode, the classification mechanism is based on three events classification as defined in HDBaseT standard.

Port Start Up

Upon a successful detection and classification process, power is applied to the load via a controlled Start Up mechanism.
During this period inrush current is limited to 425mA for a typical duration of 65mS, which allows PD load to charge and allow steady state power condition.

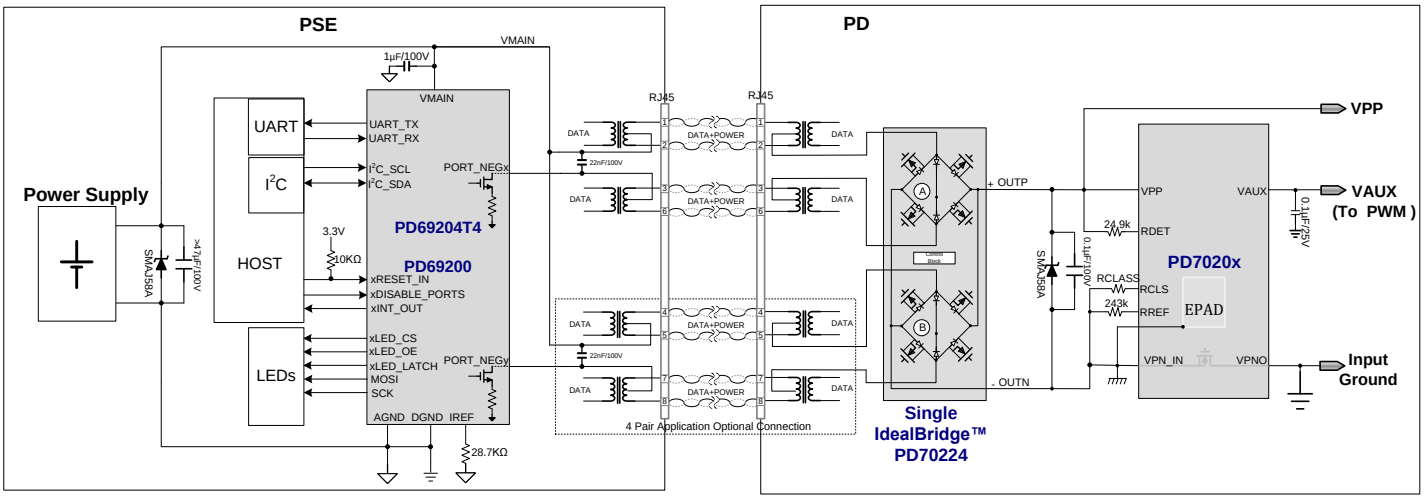


Figure 11:4-Pairs PoE System Diagram

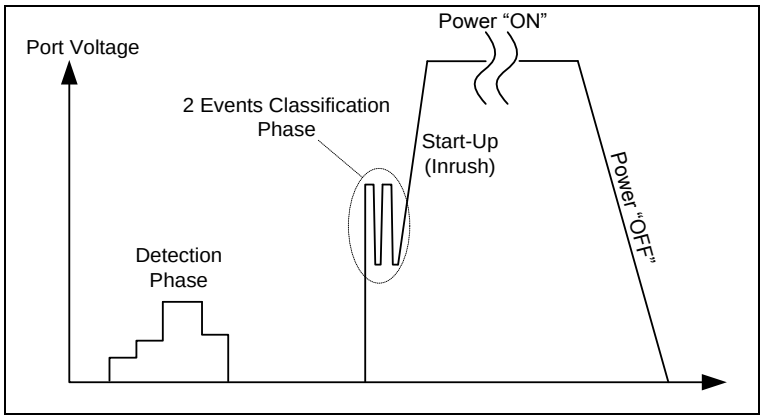


Figure 12: Typical IEEE802.3at Port PoE Voltage Diagram

Over-Load Detection and Port Shut Down

After power up, PD69204T4 automatically initializes its internal protection mechanisms. These are utilized to monitor and disconnect power from the PD in cases where extreme conditions occur, as specified in IEEE802.3 standard. These conditions include over-current or short ports terminals scenario.

Disconnect Detection

PD69204T4 supports DC Disconnect Function as per IEEE802.3 standard.

This mechanism continuously monitors load current and disconnects power in cases where load current is below 7.5mA (typical) for more than 324mS.

IC Thermal monitoring

The PD69204T4 contain a thermal sensor that is sampled by the PD69200 every 20mS so the PD69204T4 die temperature is monitored at all times. In order to protect the PD69208T4 from damage the system ports will be disconnected before damage can occur.

An temperature alarm threshold can be set by PD69200 controller to send interrupt indication by the xINT_OUT pin before ports disconnects.

The temperature can be read and monitored by the host as well, if required.

Over-Temperature Protection

In addition to the die thermal sensor there are thermal sensors on each MOSFET that continuously monitor per port main MOSFETs junction temperature and will shut down the port load power in cases where temperature exceeds 200°C.

V_{MAIN} Out of Range Protection

The system will automatically disconnect ports power in cases where V_{MAIN} exceeds pre configure over-voltage and under-voltage thresholds.

4-Pairs Ports

In order to have the ability to deliver to the PD more than 30w, 4 pairs powering is used.
4 pairs powering utilizes all 8 RJ45 wires for delivering the power.
It is implemented by utilizing as 2 physical ports of (1 logical port) PD69204T4 with 2 separate front-ends, each delivers maximum AT power, enabling delivery of 60W over 4 pairs.
The 2 ports drive separate 2 pairs and connect together inside the PD after the serial diodes as shown in Figure 11.
The 2 ports will be managed by PD69200 with certain rules.
In this case, PD69200 can support up to 48 logical 4 pairs ports (96 physical ports)

- The 2 ports that compound the 4 pairs port is predefine prior the system startup. 4 pairs port can be built from combination of any 2 ports in the system, same PD69204T4 or separate ones. Ports status is unified.
- Line detection:
  - In case one port fails Pre-Detection:
    - If the port is connected as ALT-A - the port will turn on as 2-pair port.
    - If the port is connected as ALT-B - the port will not power on.
  - In case both pairs pass Pre-Detection and fail Line Detection, port will not power-on.
- Classification:
  - PD should have mechanism that counts the number of class events and determines PSE type.
    - 2 class events – PSE is 2 pairs AT.
    - 4 class events – PSE is 4 pairs AT/UPoE.
    - 6 class events – PSE is 4 pairs PoH.
  - In IEEE802.3bt mode, the PSE-PD will have mutual identification mechanism that will determine what power will be supplied to the pd.
  - When ALT-A class is 4 and ALT-B class is valid, port will be turned on as 4-pairs.
- Startup:
  - Startup of the ports is done simultaneously with maximum gap of 100µS.
- Port disconnection:

In case one of the ports disconnects from some reason (OVL, UDL, OVT, SC, TLIM), second port will follow it and also disconnect within 50mSec.

Power Management

System supports three power management modes:

- Class (LLDP & CDP) mode
- Dynamic mode
- Static mode.

PPL (Port Power Limit)

Configurable port power limit; when a port exceeds the limit, it is automatically disconnected

PoH – Power over HDBaseT

PoH powering enables PSE to provide 95W power. Detection, powering, and disconnection are same as 4 pairs powering.

- Power:
  - According to PoH standard, minimal power on PSE output should be 95W.
  - Due to UL restriction, maximum power on PSE output is limited to 100W.
- Classification:
  - Each port classification will have 3 class events so that PD will detect 6 events.

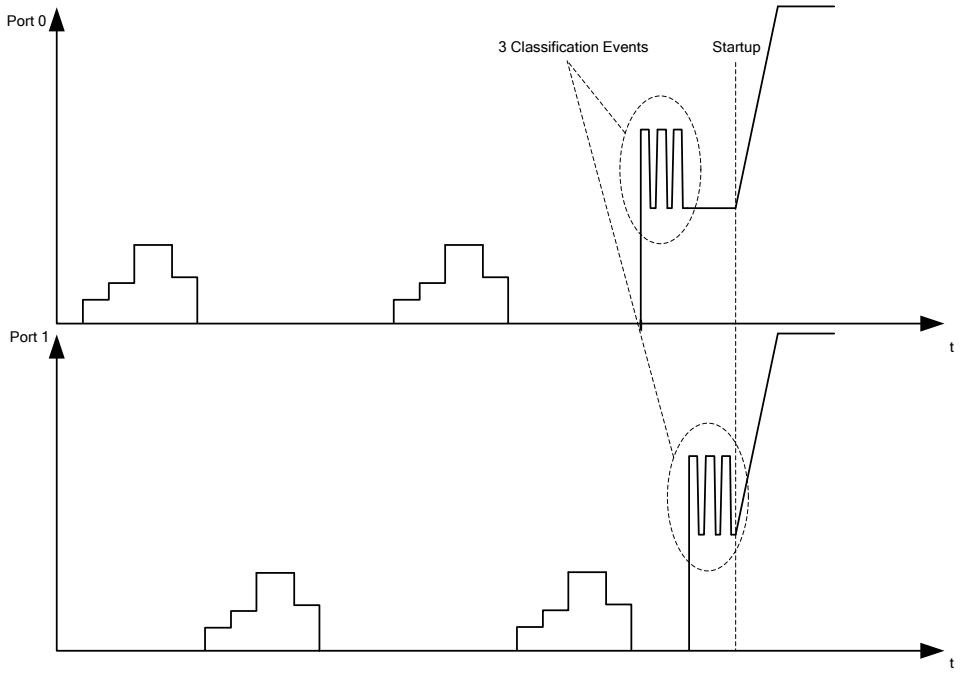


Figure 13 – 4 pairs PoH detection diagram

Reset Pin

xRESET pin is PD69200 Digital Host Reset input (Active Low).

The shortest pulse that is guaranteed to be recognized is 150uSec.

PD69200 can generate self-reset. In this case xRESET pin is driven low by PD69200 for about 100uSec.

It is recommended to connect this pin to a host open drain output with pull-up in a range of 4.7Kohm to 10Kohm.

If this pin is connected to a push/pull driver, a serial resistor of 4.7Kohm must be connected instead of pull-up.

Avoid resetting the PD69204T4 IC directly by the RESET_N pin. The PD69200 controls the PD69204T4 ICs in case of system reset is needed.

For more information about this pin connectivity refer to HW app note, Catalog Number: PD69208_AN_211.

System OK Indication

Digital output pin to Host is used as System validity indication. When system is OK pin state is low.
The behavior of this output is controlled by software mask register settings (Mask 0x28).
The mask default settings is 0, means this pin indicates valid software and Vmain is in Range. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD62000_UG_COMM_PROT)
(This pin is active low).

Interrupt Pin

Interrupt out from PoE controller, indicating events such as: port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events refer to the Serial Communication Protocol User Guide document - Catalog Number: PD62000_UG_COMM_PROT). This pin is active low.

Port Matrix Control

Enables layout designers to ascribe each physical port in the system to required logical port if required.

'Power Good' Interrupt

Interrupt from Power Supply directly to PD69204T4 manager.

For systems comprising more than a single power supply, in case one power supply fails, a port shutdown mechanism is executed to maintain operation and prevent collapse of other power supplies.
When function is used, PGD0, PGD1, PGD2, and PGD3 should be connected to main power supplies status indication pin. Any change of at least 1µS on these lines will trigger a pre-defined disconnection matrix. This matrix is defined by PD69200 system power parameters.
The port shutdown function reacts within 2 µS to any Power Good event.

LED Stream

Direct SPI interface to an external LED stream circuitry, that can drive LEDs directly without the host intervention. Enables designers to implement a simple LED circuit that does not require a software code. (LED stream clock frequency is 1MHz).
For more detailed information please refer to TN-218, *catalog number PD69200_TN_218.*

PD69204T4/PD69200 Product Overview

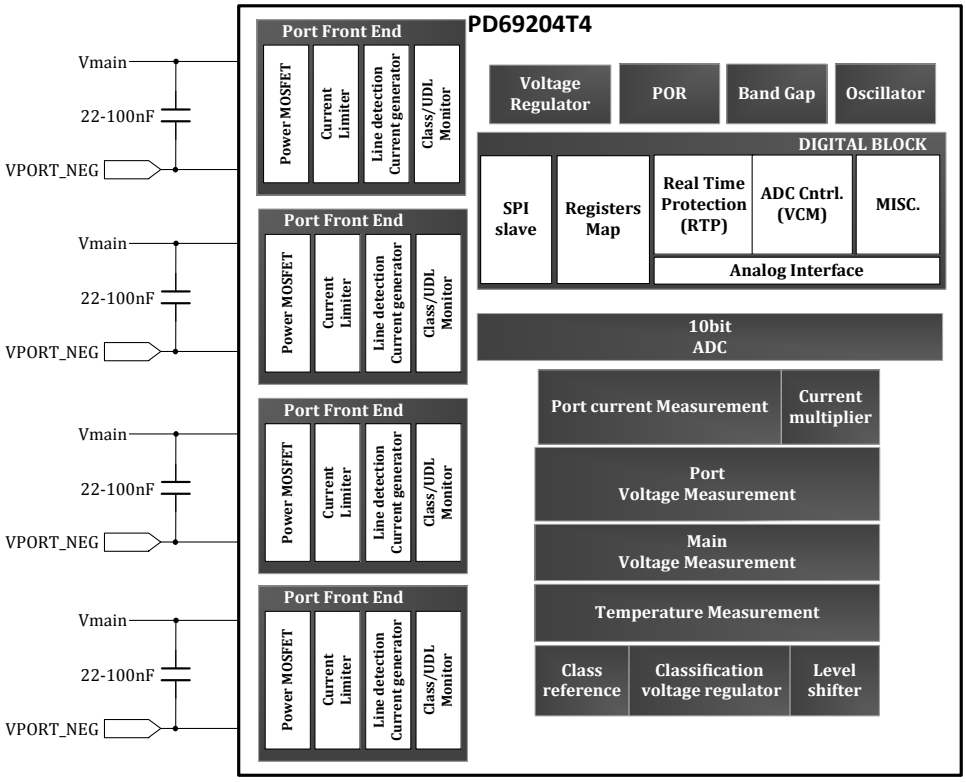


Figure 14: PD69204T4 Block Diagram

Digital Block Module

Logic Main Control Block includes Digital Timing Mechanisms and State Machines synchronizing and activating PoE functions according to PD69200 control commands, such as:

- Real Time Protection (RTP)
- Start Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring (VCM)
- ADC Interfacing
- Direct Digital Signals with Analog Block
- SPI Communication Block
- Registers

PD Detection Generator

Upon request from PD69200 to Main Control Module, PD Detection Generator generates four different voltage levels to ensure a robust AF / AT PD Detection functionality.

Classification Generator

Upon request from PD69200 to Main Control Module, State Machine applies a regulated Class Event and Mark Event voltage to ports, as required by IEEE standard.

Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a specific value, according to pre-defined limits as set by AF/AT/PoH. In cases where current exceeds this specific level, system starts measuring elapsed time. If this time period is greater than a preset threshold, port is disconnected.

Main Power MOSFET

Main power switching FET, used to control PoE current into load.

ADC

A 10-Bit Analog to Digital converter, used to convert analog signals into digital registers for Logic Control Module.

Power on Reset (POR)

Monitors the internal 3.3V voltage DC levels; if this voltage drops below specific thresholds, a reset signal is generated and PD69204T4 is reset.

Voltage Regulator

Voltage regulator generates 3.3V and 5V for internal circuitry. These voltages are derived from V_{MAIN} supply.

To use internal voltage regulator connect:

- VAUX5 to DRV_VAUX5
- VAUX3P3 to VAUX3P3_INT

There are three options to reduce PD69204T4 power dissipation by regulating voltage outside the chip:

- Use an external NPN transistor to regulate the 5V.
  In this setup, the configuration of regulators pins should be:
  - DRV_VAUX5 is connected to NPN BASE
  - VAUX5 is connected to NPN EMITTER

  (Connect Collector to V_{MAIN})
  - VAUX3P3 is connected to VAUX3P3_INT

- Supply PD69204T4 with an external 5V voltage regulator.
  In this setup, regulators pins configuration should be:
  - VAUX3P3 is connected to VAUX3P3_INT
  - DRV_VAUX5 is not connected (left open)
  - VAUX5 is connected to external 5 V

- Supply PD69204T4 with an external 3.3V voltage regulator.
  In this setup, regulators pins configuration should be:
  - VAUX5 is connected to DRV_VAUX5
  - VAUX3P3_INT is not connected (left open)
  - VAUX3P3 is connected to external 3.3 V

The options can be implemented simultaneously.

CLK

PD69204T4 CLK is an internal 8 MHz clock oscillator

SPI Communication

PD69204T4 uses SPI communication in order to communicate with PD69200 MCU.
SPI acts as an SPI slave mode only.
Each PD69204T4 has an address determined by ADDR0-ADDR3 pins. Up to 12 ICs can be supported by the PD69200 at addresses 0-11.
Actual frequency between PD69200 and PD69204T4 ICs is 1MHz.

Packets structure is as follows:

Control byte Selects PD69204T4 According to the address	R/W bit	Internal Register Address	Number of words (only in read access)	Data Written to IC (in write access) Read from IC (in read access)
8 bits	R(0)/W(1)	8 bits	8 bits	bits 16

PD69204T4 SPI Addressing

PD69204T4 Operates in 8 bit address and 16 bit data
PD69204T4 responds to SPI transaction if the first SPI byte (IC address byte bits[7:1]) complies with the following:

3bits:'000'	4bits: address input pin	1bit: r/w

Broadcast:

- A broadcast command is intended to instruct all connected PD69204T4 ICs to perform a specific operation.
- Broadcast command is a write command with the standard packet structure. In case of a broadcast read operation the read data is not valid and the read operation has no impact.
-

3bits:'001'	4bits: '0000'	1bit: w

SPI Detailed Timing Information

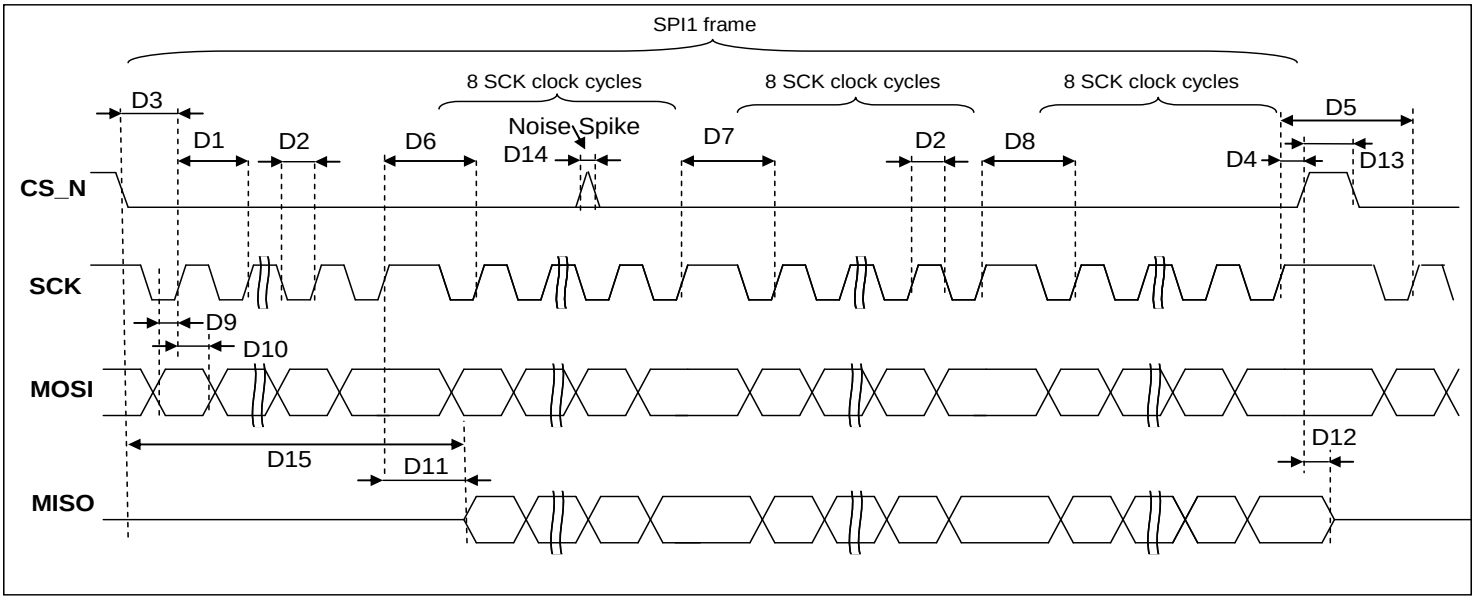


Figure 15 : SPI Detailed Timing Diagram

Table 11

Name	Min Delay	Max Delay	Description
D1	910nS		SPI clock period
D2	45%	55%	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock Positive Edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock Positive Edge (delay before SPI_CS inactive Signal)
D5	2 spi clock cycles		Delay between last SCK in SPI1 frame and first SCK at adjacent SPI1 frame
D6	1 spi clock cycles		Between byte 0 (IC addr) and byte 1(addr)
D7	1 spi clock cycles		Between byte 1 (addr) and byte 2(data).
D8	1 SPI clock cycles		Between byte 2 (MS data byte) and byte 3(LS data byte).
D9	340 ns		MOSI setup time

Name	Min Delay	Max Delay	Description
D10	340 ns		MOSI hold time
D11		700ns	MISO tri-state to valid data from clock positive edge
D12		700ns	MISO valid data to tri-state from SPI_CS positive edge
D13	1 SPI clock cycles		SPI_CS width (Delay SPI1 frame to adjacent SPI1 frame)
D14		60ns	Filtered Glitch Width
D15		D3 + D11 + 24 SPI clock cycles	MISO tri-state from SPI_CS Negative Edge to valid data
D16	200nS		MISO setup to SCK posedge
D17	200nS		MISO hold to SCK posedge

PD69200 I^2C Address Selection

I^2C interface between Host CPU and a specific PD69200 requires setting PD69200 address; this is done by applying a specific voltage level to pin #22 (I2C_ADDR_MEAS) as shown below:

Table 12

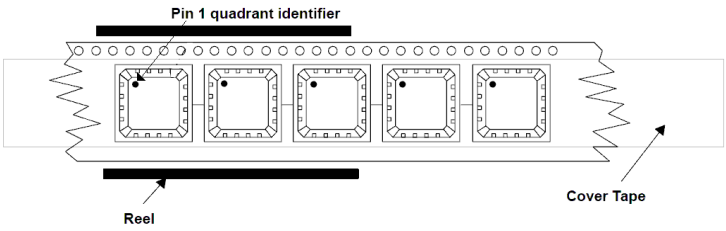
I2C_ADDR VOLTAGE LEVEL	I^2C ADDRESS (HEXADECIMAL)
0.00 to 0.21V_{DC}	UART
0.21 to 0.41V_{DC}	0x4
0.41 to 0.62V_{DC}	0x8
0.62 to 0.83V_{DC}	0xC
0.83 to 1.03V_{DC}	0x10
1.03 to 1.24V_{DC}	0x14
1.24 to 1.44V_{DC}	0x18
1.44 to 1.65V_{DC}	0x1C
1.65 to 1.86V_{DC}	0x20
1.86 to 2.06V_{DC}	0x24
2.06 to 2.27V_{DC}	0x28
2.27 to 2.48V_{DC}	0x2C
2.48 to 2.68V_{DC}	0x30
2.68 to 2.89V_{DC}	0x34
2.89 to 3.09V_{DC}	0x38
3.09 to 3.30V_{DC}	0x3C

Note: UART communications configuration:

- Bits per second: 19,200 bps

- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Tape and Reel – Packaging Information



Pin-1 Orientation of QFN Packages

Figure 16 : Tape and Reel Pin-1 Oreintation

Table 13

REEL MECHANICAL DATA		
	mm.	**inch**
Tape size	16.00 ±0.3	0.630 ±0.012
A max.	330	13”
B max.	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min.	20.2	0.795
N min.	50	1.968
G	16.4+2.0/-0.0	0.645+0.079/-0.0
T max.	29	1.142
BASE QUANTITY	2000 pcs.	

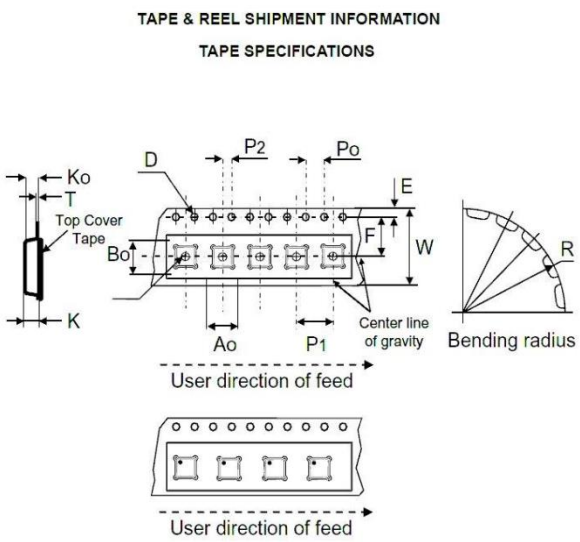


Figure 18 : Tape and Reel Tape specifications

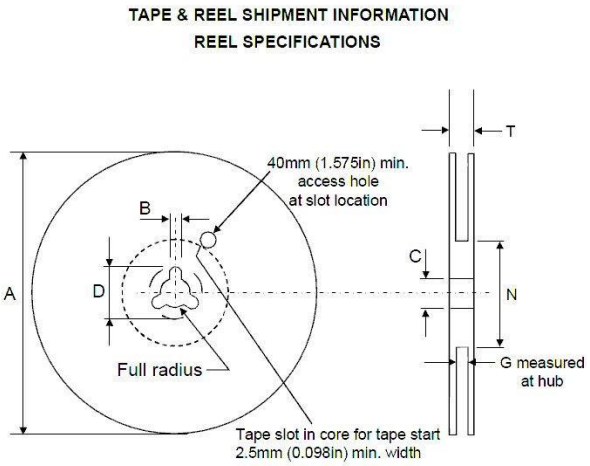


Figure 17 : Tape and Reel Rell specifications

Revision History

Revision Level / Date	Para. Affected	Description
0.21 / Nov 2016		Initial Release – Preliminary version

For support contact**:** PoEsupport@microsemi.com

Visit our web site at: **www.microsemi.com** **Catalog Number**: DS_PD69204T4_PD69200