Pin Configurations

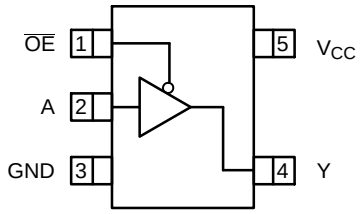


Figure 2. SC−88A and SC−74A (Top View)

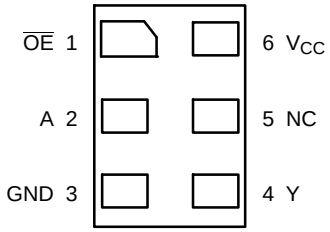


Figure 3. MicroPak (Top Through View)

PIN DEFINITIONS

Pin # SC−88A / SC74A	Pin # MicroPak	Name	Description
1	1	$\overline{OE}$	Input
2	2	A	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V_{CC}	Supply Voltage
	5	NC	No Connect

FUNCTION TABLE

Inputs		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

H = HIGH Logic Level
L = LOW Logic Level
X = HIGH or LOW Logic Level
Z = HIGH Impedance State

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−50	mA
I_{OUT}	DC Output Current		−	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		−	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias		−	+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
P_D	Power Dissipation in Still Air	SC−74A	−	390	mW
		SC−88A	−	332	
		MicroPak−6	−	812	
		MicroPak2™−6	−	812	
ESD	Human Body Model, JEDEC: JESD22−A114		−	4000	V
	Charge Device Model, JEDEC: JESD22−C101		−	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	Active State	0	V_{CC}	V
		Three−State	0	5.5	
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} at 3.3 V ±0.3 V	0	10	
		V_{CC} at 5.0 V ±0.5 V	0	5	
θ_{JA}	Thermal Resistance	SC−74A	−	320	°C/W
		SC−88A	−	377	
		MicroPak−6	−	154	
		MicroPak2−6	−	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

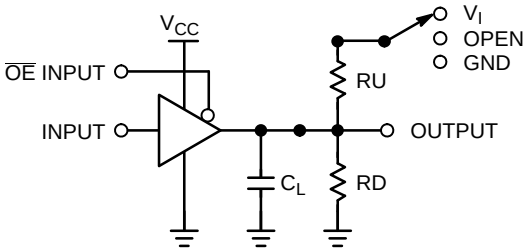
DC ELECTICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.65 V_{CC}	−	−	0.65 V_{CC}	−	V
		2.30 to 5.50		0.70 V_{CC}	−	−	0.70 V_{CC}	−	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95		−	−	0.35 V_{CC}	−	0.35 V_{CC}	V
		2.30 to 5.50		−	−	0.30 V_{CC}	−	0.30 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IH} or V_{IL}, I_{OH} = −100 μA	1.55	1.65	−	1.55	−	V
		1.80		1.70	1.80	−	1.70	−	
		2.30		2.20	2.30	−	2.20	−	
		3.00		2.90	3.00	−	2.90	−	
		4.50		4.40	4.50	−	4.40	−	
		1.65	I_{OH} = −4 mA	1.29	1.52	−	1.29	−	
		2.30	I_{OH} = −8 mA	1.90	2.15	−	1.90	−	
		3.00	I_{OH} = −16 mA	2.40	2.80	−	2.40	−	
		3.00	I_{OH} = −24 mA	2.30	2.68	−	2.30	−	
		4.50	I_{OH} = −32 mA	3.80	4.20	−	3.80	−	
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 100 μA	−	0.00	0.10	−	0.00	V
		1.80		−	0.00	0.10	−	0.10	
		2.30		−	0.00	0.10	−	0.10	
		3.00		−	0.00	0.10	−	0.10	
		4.50		−	0.00	0.10	−	0.10	
		1.65	I_{OL} = 4 mA	−	0.80	0.24	−	0.24	
		2.30	I_{OL} = 8 mA	−	0.10	0.30	−	0.30	
		3.00	I_{OL} = 16 mA	−	0.15	0.40	−	0.40	
		3.00	I_{OL} = 24 mA	−	0.22	0.55	−	0.55	
		4.50	I_{OL} = 32 mA	−	0.22	0.55	−	0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5	0 ≥ V_{IN} ≥ 5.5 V	−	−	±1	−	±10	μA
I_{OZ}	3−STATE Output Leakage	0 to 5.5	V_{IN} = V_{IH} or V_{IL} 0 ≥ V_O ≥ 5.5 V	−	−	±1	−	±10	μA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT} = 5.5 V	−	−	1	−	10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN} = 5.5 V, GND	−	−	2	−	20	μA

AC ELECTRICAL CHARACTERISTICS

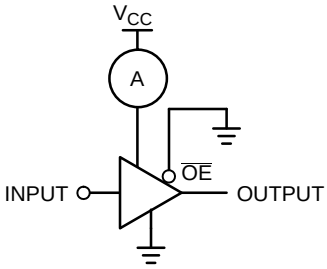
Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 4, 6)	1.65	C_L = 15 pF, R_D = 1 MΩ S_1=OPEN	−	6.4	13.2	−	13.8	ns
		1.80		−	5.3	11.0	−	11.5	
		2.50 ±0.20		−	3.4	7.5	−	8.0	
		3.30 ±0.30		−	2.5	5.2	−	5.5	
		5.00 ±0.50		−	2.1	4.5	−	4.8	
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω S_1 = OPEN	−	3.2	5.7	−	6.0	
		5.00 ±0.50		−	2.6	5.0	−	5.3	
t_{PZL}, t_{PZH}	Output Enable Time (Figure 4, 6)	1.65	C_L = 50 pF, R_D = 500 Ω RU = 500 Ω S_1 = GND for t_{PZH} S_1 = V_{IN} for t_{PZL} V_{IN} = 2 · V_{CC}	−	8.4	15.0	−	15.6	ns
		1.80		−	7.0	12.5	−	13.0	
		2.50 ±0.20		−	4.6	8.5	−	9.0	
		3.30 ±0.30		−	3.5	6.2	−	6.5	
		5.00 ±0.50		−	2.8	5.5	−	5.8	
t_{PLZ}, t_{PHZ}	Output Disable Time (Figure 4, 6)	1.65	C_L = 50 pF, R_D = 500 Ω RU = 500 Ω S_1 = GND for t_{PHZ} S_1 = V_{IN} for t_{PLZ} V_{IN} = 2 · V_{CC}	−	6.5	13.2	−	14.5	
		1.80		−	5.4	11.0	−	12.0	
		2.50 ±0.20		−	3.5	8.0	−	8.5	
		3.30 ±0.30		−	2.8	5.7	−	6.0	
		5.00 ±0.50		−	2.1	4.7	−	5.0	
C_{IN}	Input Capacitance	0.00		−	4	−	−	−	pF
C_{OUT}	Output Capacitance	0.00		−	8	−	−	−	
C_{PD}	Power Dissipation Capacitance (Note 2) (Figure 5)	3.30		−	17	−	−	−	pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).



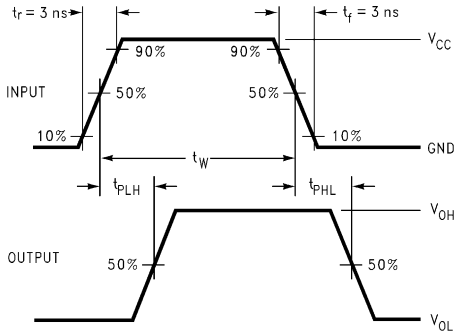
NOTE:
3. C_L includes load and stray capacitance; Input PRR = 1.0 MHz; t_W = 500 ns

Figure 4. AC Test Circuit



NOTE:
4. Input = AC Waveform; $t_r = t_f$ = 1.8 ns; PRR = 10 MHz; Duty Cycle = 50%.

Figure 5. I_{CCD} Test Circuit



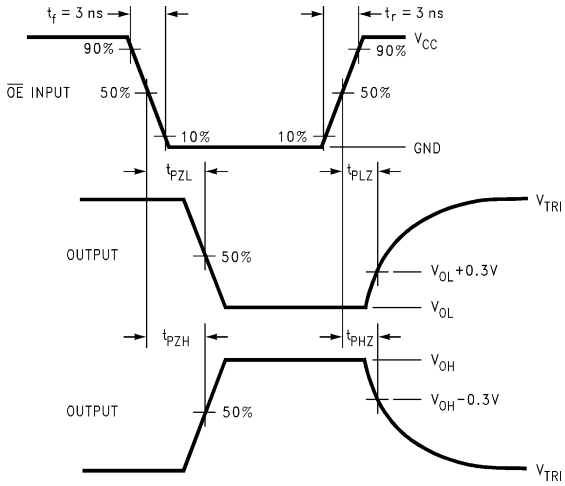


Figure 6. AC Waveforms

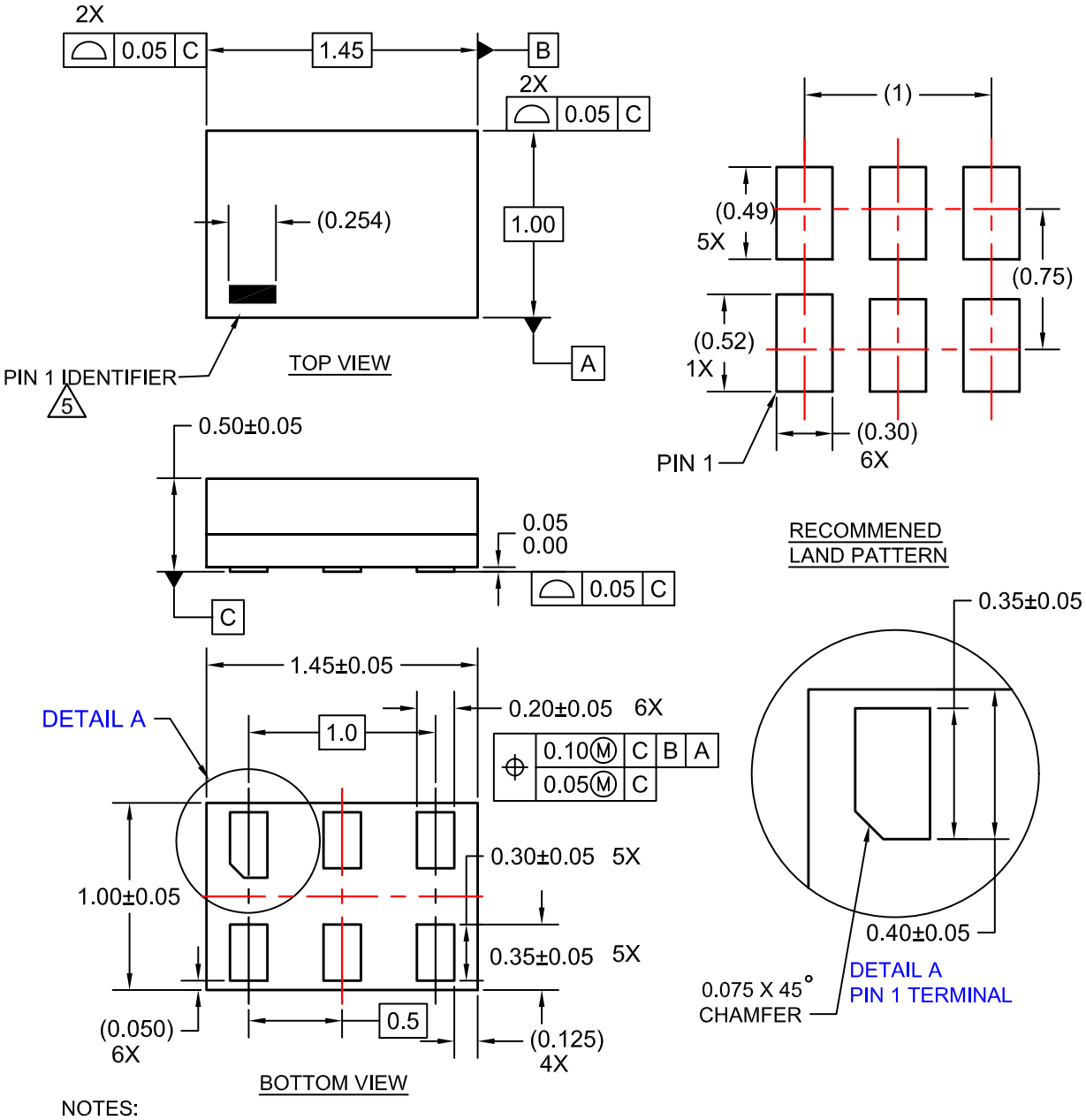
ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature	Packages	Shipping†
NC7SZ125M5X	7Z25	−40 to +85°C	SC−74A	3000 / Tape & Reel
NC7SZ125P5X	Z25	−40 to +85°C	SC−88A	3000 / Tape & Reel
NC7SZ125L6X	DD	−40 to +85°C	MicroPak	5000 / Tape & Reel
NC7SZ125FHX	DD	−40 to +85°C	MicroPak2	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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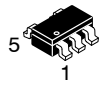
DESCRIPTION:	**SIP6 1.45X1.0**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

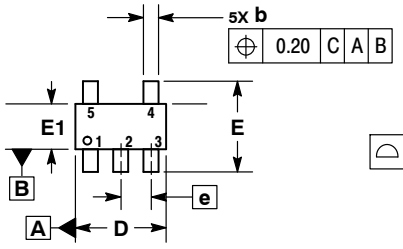
ON Semiconductor®

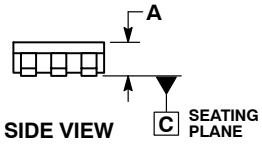
SC−74A
CASE 318BQ
ISSUE B

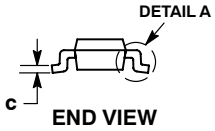
DATE 18 JAN 2018



SCALE 2:1



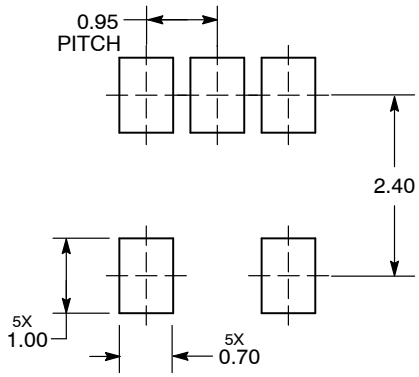




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

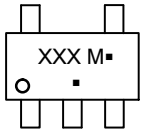
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SC−74A		PAGE 1 OF 1

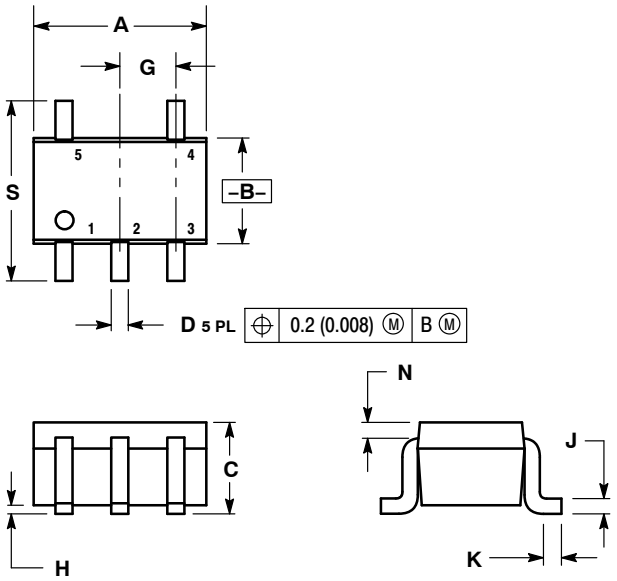
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

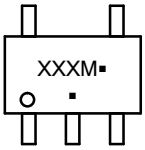
DATE 17 JAN 2013



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

GENERIC MARKING DIAGRAM*

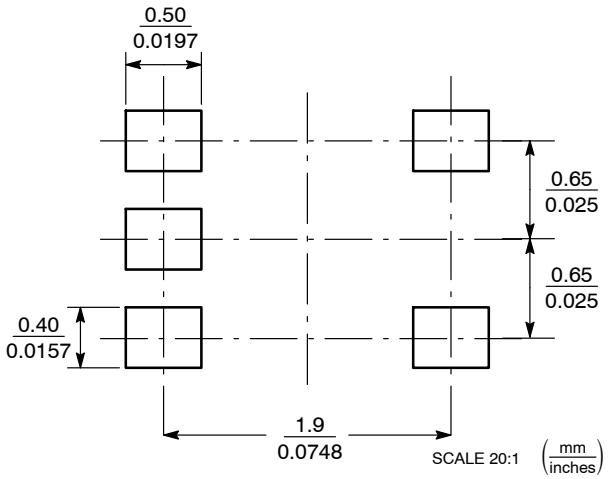


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

SOLDER FOOTPRINT



STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

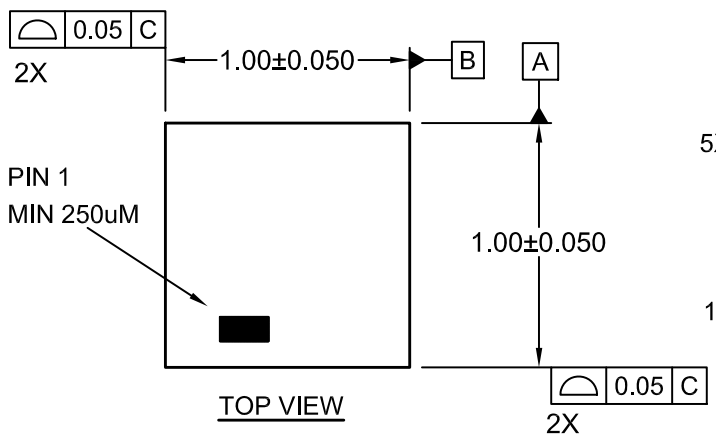
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

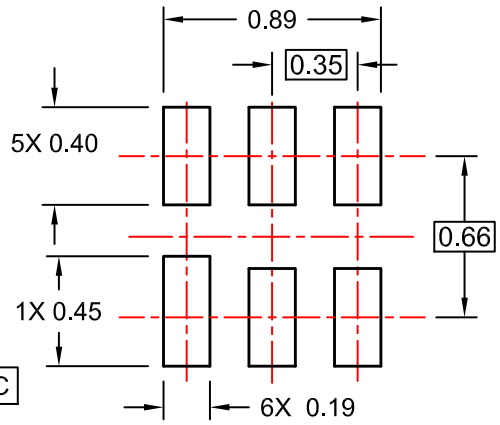
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

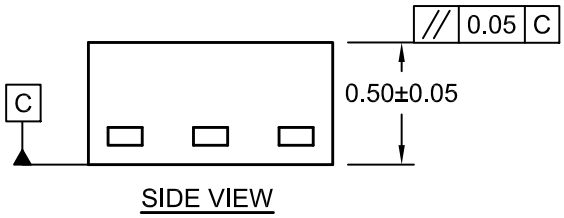
UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

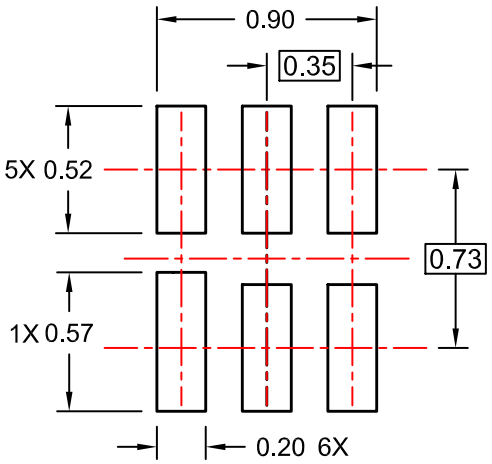
DATE 31 AUG 2016



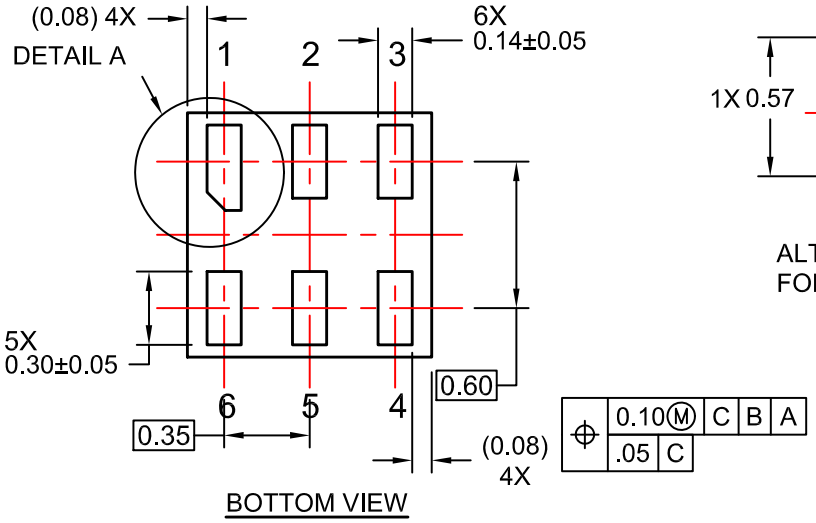


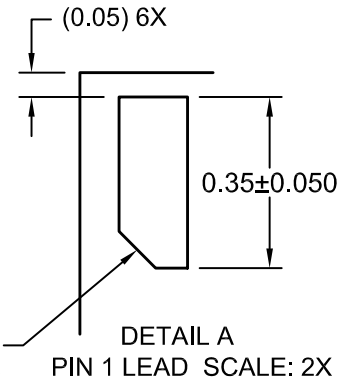
RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB





ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION





NOTES:
A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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DESCRIPTION:	**UDFN6 1.0X1.0, 0.35P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
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