

MM74HC123A Dual Retriggerable Monostable Multivibrator

General Description

The MM74HC123A high speed monostable multivibrators (one shots) utilize advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The MM74HC123A can be triggered on the positive transition of the clear while A is held LOW and B is held HIGH.

The MM74HC123A is retriggerable. That is it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT}) (C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

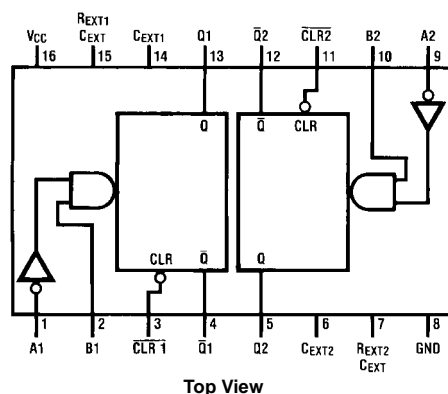
- Typical propagation delay: 25 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula $T = RC$
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: $\pm 5\%$ (typ)
- Schmitt Trigger A & B inputs allow rise and fall times to be as slow as one second

Ordering Code:

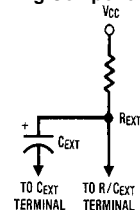
Order Number	Package Number	Package Description
MM74HC123AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC123ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC123AMTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC123AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Timing Component



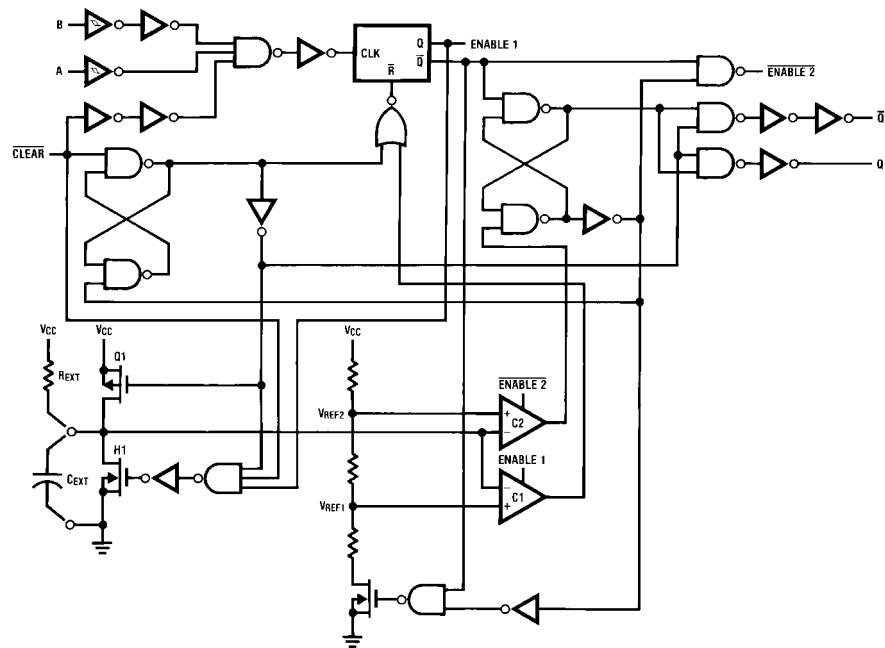
Note: Pin 6 and Pin 14 must be hard-wired to GND.

Truth Table

Inputs			Outputs	
Clear	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow	$\text{—}\text{H}\text{—}$	$\text{—}\text{L}\text{—}$
H	\downarrow	H	$\text{—}\text{L}\text{—}$	$\text{—}\text{H}\text{—}$
\uparrow	L	H	$\text{—}\text{H}\text{—}$	$\text{—}\text{L}\text{—}$

H = HIGH Level
 L = LOW Level
 \uparrow = Transition from LOW-to-HIGH
 \downarrow = Transition from HIGH-to-LOW
 $\text{—}\text{H}\text{—}$ = One HIGH Level Pulse
 $\text{—}\text{L}\text{—}$ = One LOW Level Pulse
 X = Irrelevant

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	−0.5V to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times (Clear Input)			
(t_r, t_f) $V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.**Note 2:** Unless otherwise specified all voltages are referenced to ground.**Note 3:** Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = −40 to 85°C	T _A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	mV
			6.0V	6.0	5.9	5.9	5.9	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
								V
I _{IN}	Maximum Input Current (Pins 7, 15)	V _{IN} = V _{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I _{IN}	Maximum Input Current (all other pins)	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (standby)	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		8.0	80	160	μA
I _{CC}	Maximum Active Supply Current (per monostable)	V _{IN} = V _{CC} or GND R/C _{EXT} = 0.5V _{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 4: For a power supply of $5V \pm 10\%$ the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to \bar{Q}		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to \bar{Q}		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT} = 28\text{ pF}$ $R_{EXT} = 2\text{ k}\Omega$	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT} = 1000\text{ pF}$ $R_{EXT} = 10\text{ k}\Omega$	10		μs

AC Electrical Characteristics $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
				Typ	Guaranteed Limits			
t _{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q		2.0V	77	169	194	210	ns
			4.5V	26	42	51	57	ns
			6.0V	21	32	39	44	ns
t _{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to \overline{Q}		2.0V	88	197	229	250	ns
			4.5V	29	48	60	67	ns
			6.0V	24	38	46	51	ns
t _{PHL}	Maximum Propagation Delay Clear to Q		2.0V	54	114	132	143	ns
			4.5V	23	34	41	45	ns
			6.0V	19	28	33	36	ns
t _{PLH}	Maximum Propagation Delay Clear to \overline{Q}		2.0V	56	116	135	147	ns
			4.5V	25	36	42	46	ns
			6.0V	20	29	34	37	ns
t _W	Minimum Pulse Width A, B, Clear		2.0V	57	123	144	157	ns
			4.5V	17	30	37	42	ns
			6.0V	12	21	27	30	ns
t _{REM}	Minimum Clear Removal Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t _{WQ(MIN)}	Minimum Output Pulse Width	C _{EXT} = 28 pF R _{EXT} = 2 kΩ R _{EXT} = 6 kΩ (V _{CC} = 2V)	2.0V	1.5				μs
			4.5V	450				ns
			6.0V	380				ns
t _{WQ}	Output Pulse Width	C _{EXT} = 0.1 μF R _{EXT} = 10 kΩ	Mn	5.0V	1	0.9	0.86	ms
			Mx	5.0V	1	1.1	1.14	1.15
C _{IN}	Maximum Input Capacitance (Pins 7 & 15)			12	20	20	20	pF
C _{IN}	Maximum Input Capacitance (other inputs)			6	10	10	10	pF
C _{PD}	Power Dissipation Capacitance	(Note 5)		70				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Theory of Operation

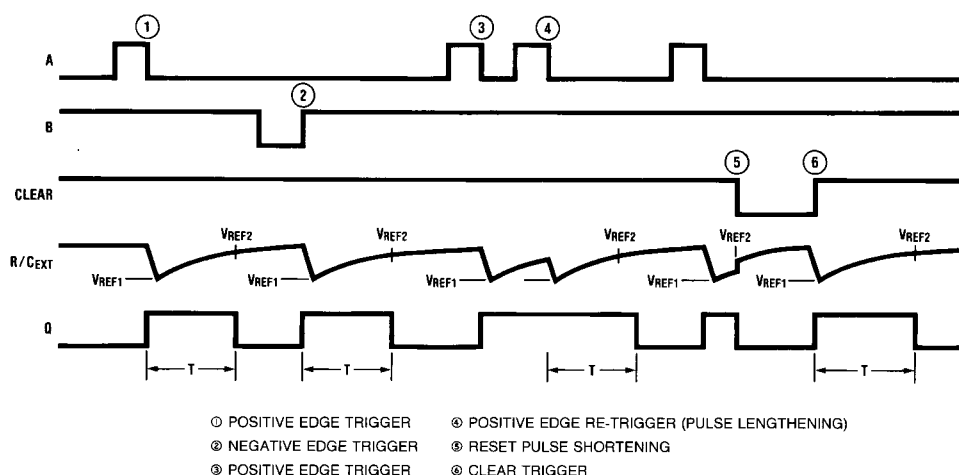


FIGURE 1.

Trigger Operation

As shown in Figure 1 and the logic diagram, before an input trigger occurs, the one shot is in the quiescent state with the Q output LOW, and the timing capacitor C_{EXT} completely charged to V_{CC} . When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N11. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT} , toward V_{CC} . When the voltage across C_{EXT} equals V_{REF2} , comparator C2 changes state causing the output latch to reset (Q goes LOW) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}). The MM74HC123A can also be triggered when clear goes from GND to V_{CC} (while A is at GND and B is at V_{CC}).

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the MM74HC123A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT} , R_{EXT} , or the duty cycle of the input waveform.

Retrigger Operation

The MM74HC123A is retriggered if a valid trigger occurs 3 followed by another trigger 4 before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at the R/C_{EXT} pin has begun to rise from V_{REF1} , but has not yet reached V_{REF2} , will cause an increase in output pulse width T. When a valid retrigger is initiated 4, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC} . The Q output will remain HIGH until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X :

$$t_{rr} \approx 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256 V_{CC}) C_X}{[V_{CC} - 0.7]^2}$$

Another removal/retrigger time occurs when a short clear pulse is used. Upon receipt of a clear, the one shot must charge the capacitor up to the upper trip point before the one shot is ready to receive the next trigger. This time is dependent on the capacitor used and is approximately:

$$t_{rr} = 196 + \frac{640}{V_{CC} - 0.7} + \frac{522 + (0.3 V_{CC}) C_X}{(V_{CC} - 0.7)^2} \text{ ns}$$

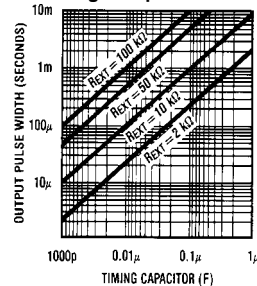
Theory of Operation (Continued)

Reset Operation

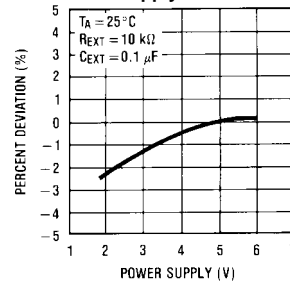
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 5. When the voltage on the capacitor reaches V_{REF2} , the reset latch will clear and then be ready to accept another pulse. If the

clear input is held low, any trigger inputs that occur will be inhibited and the Q and \bar{Q} outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

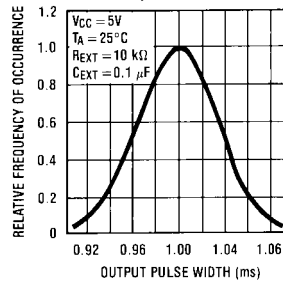
Typical Output Pulse Width vs. Timing Components



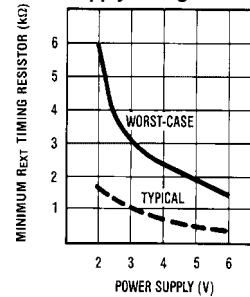
Typical 1ms Pulse Width Variation vs. Supply



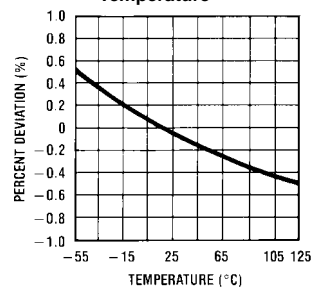
Typical Distribution of Output Pulse Width, Part to Part



Minimum R_{EXT} vs. Supply Voltage



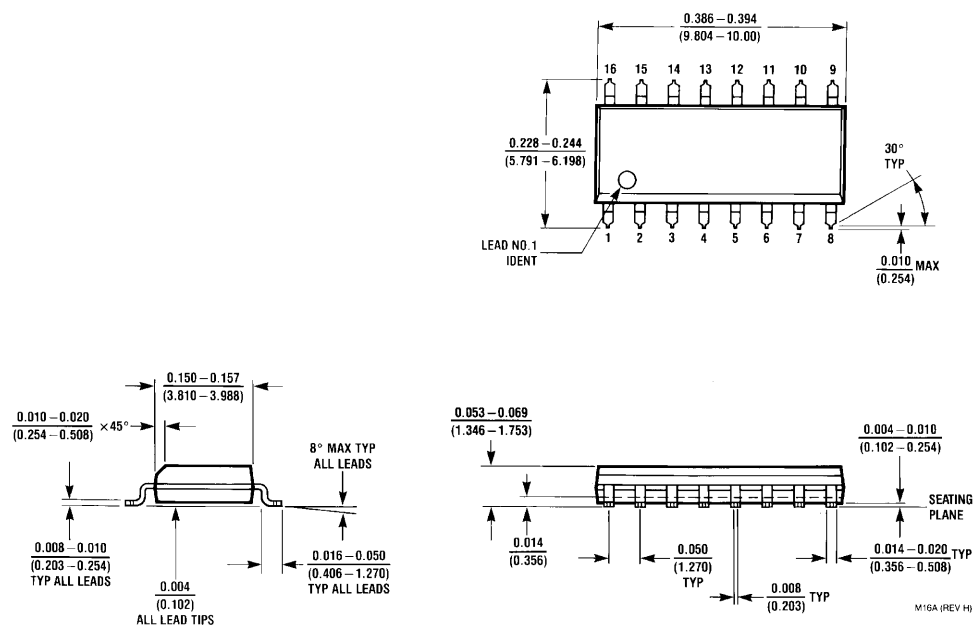
Typical 1ms Pulse Width Variation vs. Temperature



Note: R and C are not subjected to temperature. The C is polypropylene.

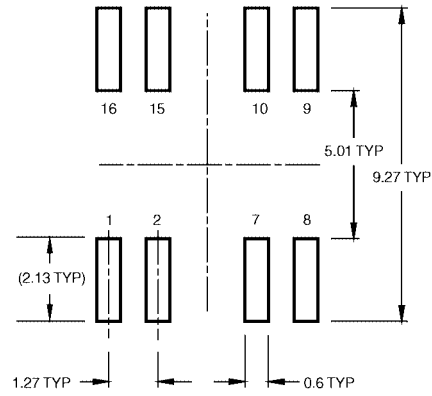
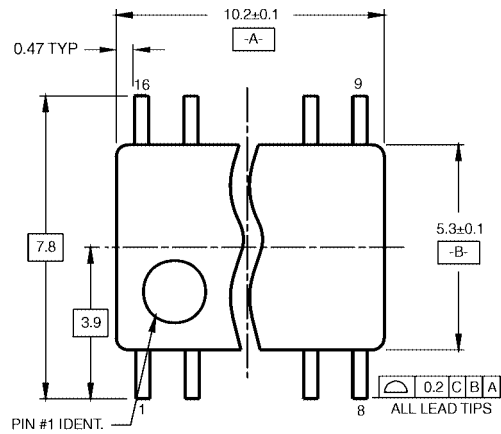
Physical Dimensions

inches (millimeters) unless otherwise noted

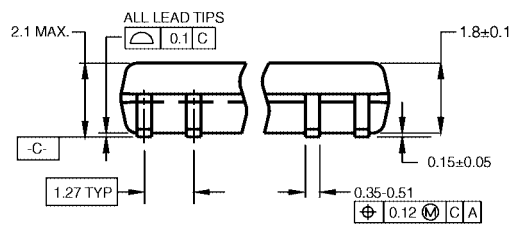


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

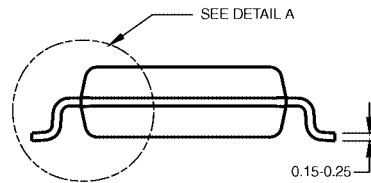
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



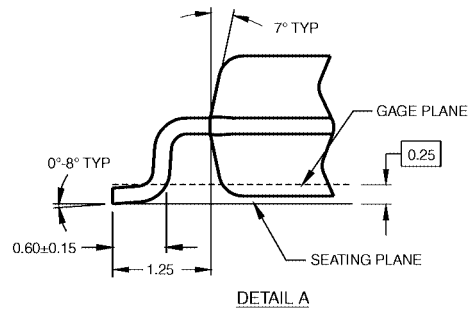
DIMENSIONS ARE IN MILLIMETERS



NOTES:

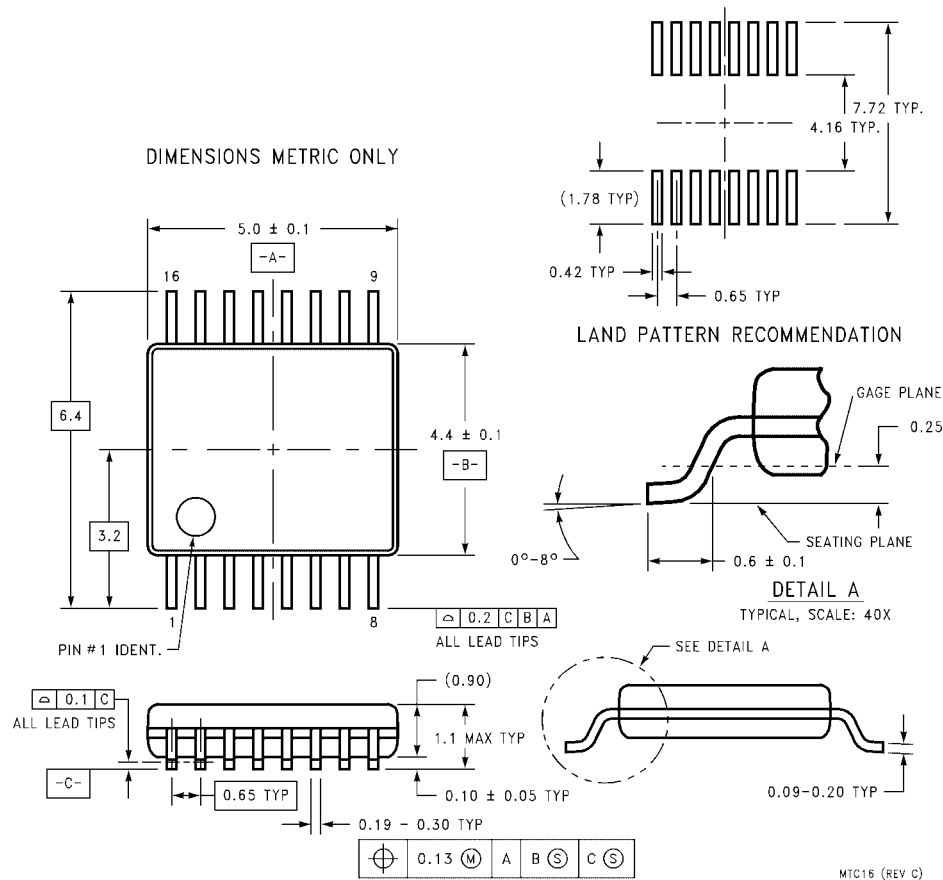
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



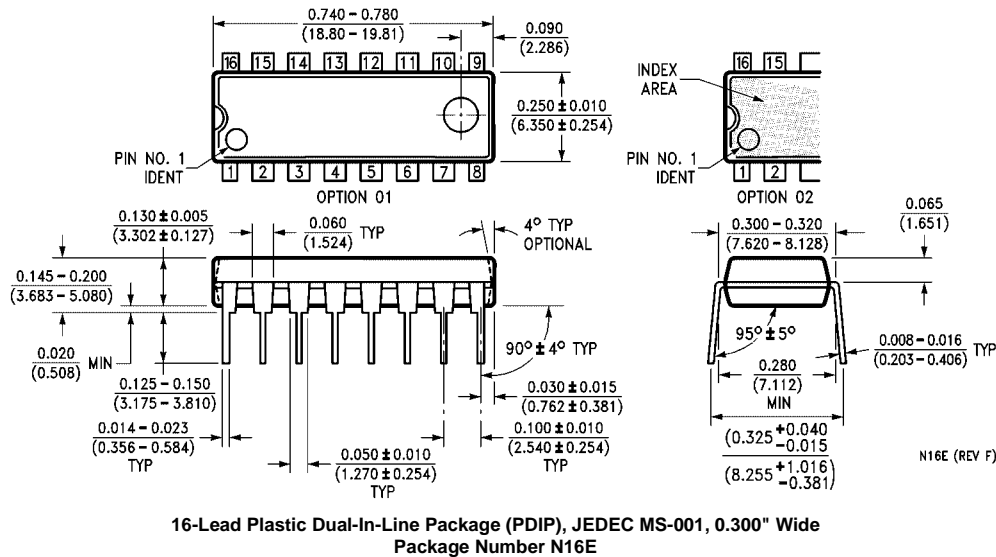
DETAIL A

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative