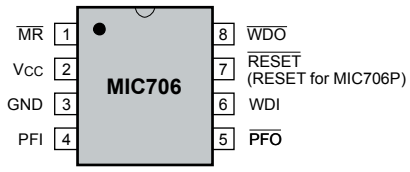
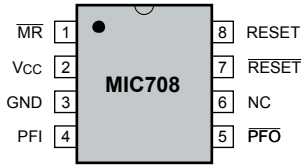
Pin Configuration





8-Pin PDIP Package
8-Pin SOIC Package

Pin Description

Pin Number MIC705/6	Pin Number MIC707/8	Pin Name	Pin Function
1	1	/MR	Manual Reset Input forces /RESET to assert when pulled below 0.8V. An internal pull-up current of 250µA on this input forces it high when left floating. this input can also be driven from TTL or CMOS logic.
2	2	VCC	Primary supply input, +5V
3	3	GND	IC ground pin, 0V reference
4	4	PFI	Power Fail Input. Internally connected to the power fail comparator which is referenced to 1.25V. The Power Fail Output (/PFO) remains high if PFI is above 1.25V. PFI should be connected to GND or V_{OUT} if the power fail comparator is not used.
5	5	/PFO	Power Fail Output. The power fail comparator is independent of all other function on this device.
6	N/A	WDI	Watch Dog Input. The WDI input monitors microprcessor activity, an internal watchdog timer resets itself with each transition on the watchdog input. If the WDIpin is held high or low for longer than the watchog timeout period, /WDO is forced to active low. the watchdog function can be diabled by floating the WDI pin.
N/A	6	N/C	Not Internally Connected
7	7	/RESET	/RESET is asserted if either V_{CC}goes below the reset threshold voltage or by low signal on the manual reset input (/MR). /RESET remains asserted for one reset timeout period (200ms) after V_{CC} exceeds the reset threshold voltage or after the manual reset pin transition from low to high. The watchdog timer will not assert /RESET unless /WDO is connected to /MR
8	N/A	/WDO	Output for the Watchdog Timer. The watchdog timer resets itself with each transition o the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, /WDO is forced low. /WDO will also be forced low id V_{CC} is below the reset threshold voltageand will remain low until V_{CC} returns to a valid level.
N/A	8	RESET	RESET is the compliment of /RESET and is asserted if either V_{CC} goes below the reset threshold voltage or by a low signal on the manual reset input (/MR). RESET is suitable for microprocessor systems that use active high reset.

Absolute Maximum Ratings[1]

Terminal Voltage
- V_{CC} .....–0.3V to +6.0V
- All other inputs.....–0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC}, Gnd 25mA

Output Current (all outputs)..... 20mA

Lead Temperature (soldering, 10 sec.)..... 300°C

Storage Temperature..... –65°C to +150°C

Operating Ratings[2]

Operating Temperature Range
- MIC70_N ..... –40°C to +85°C
- MIC70_M ..... –40°C to +85°C

Power Dissipation (PDIP).....475mW

Power Dissipation (SOP).....400mW

Electrical Characteristics[3]

V_{CC} = 2.70V to 5.5V for MIC70_P/R; V_{CC} = 3.00V to 5.5V for MIC70_S; V_{CC} = 3.15V to 5.5V for MIC70_T;
T_A = Operating Temperature Range, **bold** values indicate –40°C ≤ T_A ≤ +85°C; unless noted

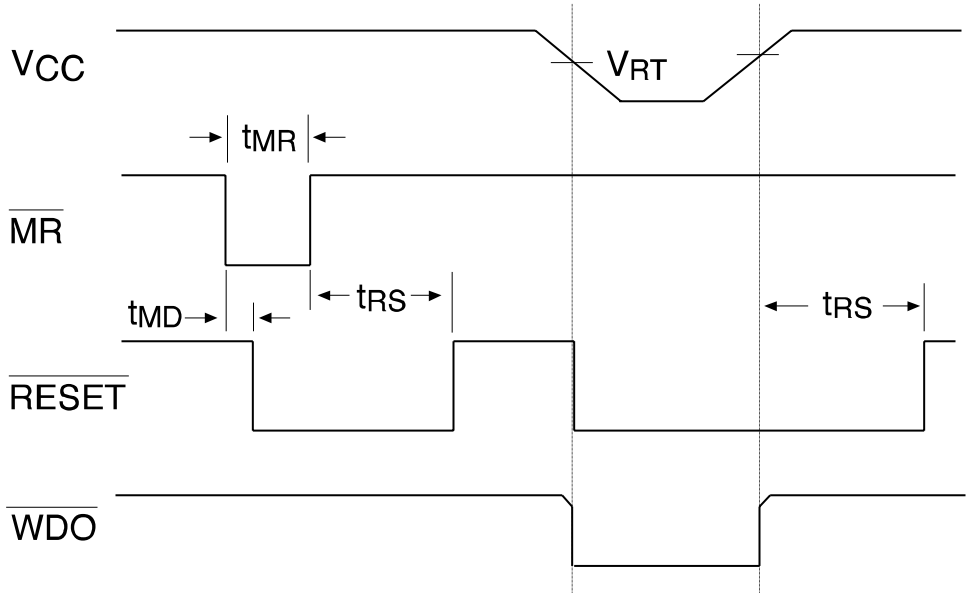
Parameter	Conditions	Min.	Typ.	Max	Units
Operating Voltage Range, V_{CC}		1.4		5.5	V
Supply Current				30	µA
Reset Voltage Threshold	MIC70_P/R MIC70_S MIC70_T	2.55 2.85 3.00	2.63 2.93 3.08	2.70 3.00 3.15	V V V
Reset Threshold Hysteresis			20		mV
Reset Pulse Width, t_{RS}		140	200	280	ms
/RESET Output Voltage (MIC70_R/S/T)	I_{Source} = 200µA I_{Sink} = 1.2mA I_{Sink} = 50µA, V_{CC} = 1.4V	0.8 × V_{CC}		 0.3 0.3	V V V
RESET Output Voltage (MIC706P)	I_{Source} = 200µA I_{Sink} = 1.2mA	0.8 × V_{CC}		 0.3	V V
RESET Output Voltage (MIC708R/S/T)	I_{Source} = 200µA I_{Sink} = 500µA	0.8 × V_{CC}		 0.3	V V
Watchdog Timeout Period, t_{WD}		1.0	1.6	2.25	sec
WDI Minimum Input Pulse, t_{WP}	V_{IL} = 0.4V, V_{IH} = 80% of V_{CC} V_{IL} = 0.4V, V_{IH} = 80% of V_{CC} > 4.5V	100 50			ns ns
WDI Threshold Voltage	V_{IH} V_{IL}	0.7 × V_{CC}		 0.6	V V
WDI Input Current	WDI = 0V or V_{CC}	-1		1	µA
WDO Output Voltage	I_{Source} = 200µA I_{Sink} = 500µA	0.8 × V_{CC}		 0.3	V V
/MR Pull-Up Current	/MR = 0V	20	250	600	µA
/MR Pulse Width, t_{MR}	V_{CC} = 4.5V	500 150			ns ns
/MR Input Threshold	V_{IL} V_{IH}	0.7 × V_{CC}		0.6	V V
/MR to Reset Output Delay, t_{MD}				750	ns
PFI Input Threshold		1.2	1.25	1.3	V
PFI Input Current		-25	0.01	+25	nA
/PFO Output Voltage	I_{Sink} = 1.2mA I_{Source} = 200µA	 0.8 × V_{CC}		0.3	V V

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

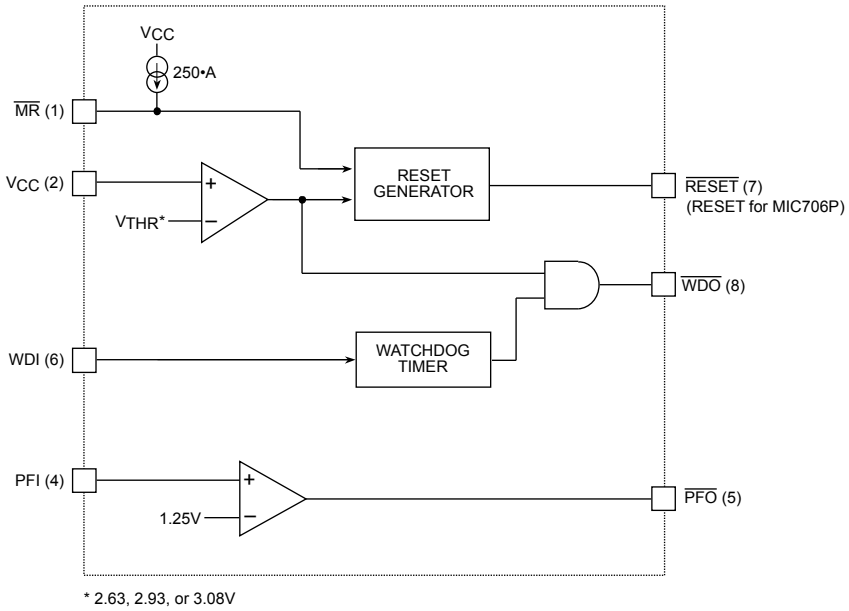
Note 3. Specification for packaged product only.

Timing Diagram

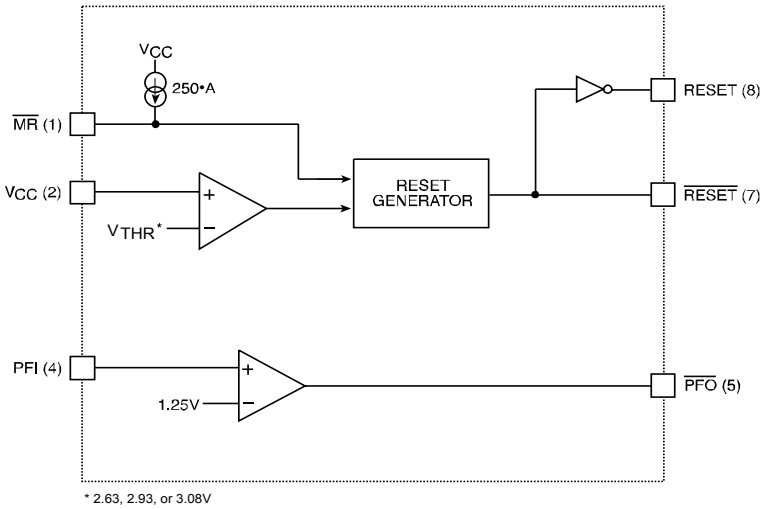


Timing Diagram for Reset

Block Diagram



MIC705/MIC706 Block diagram



MIC707/MIC708 Block Diagram

Applications Information

Power Fail Warning

An additional comparator which is independent of the other functions on the MIC706P/R/S/T is provided for early warning of power failure. An external voltage divider can be used to compare unregulated DC to an internal 1.25V reference. The voltage divider ratio on the input of the power-fail comparator (PFI) can be chosen so as to trip the power fail comparator a few milliseconds before V_{CC} falls below the maximum reset threshold voltage. The output of the power-fail comparator (/PFO) can be used to interrupt the microprocessor when used in this mode and execute shut-down procedures prior to power loss. Hysteresis can be added to this comparator with external resistors, as is commonly done with any comparator. When VCC < VBATT - 1.2V (typ.), the power-fail comparator is turned off and /PFO is pulled low in order to conserve power.

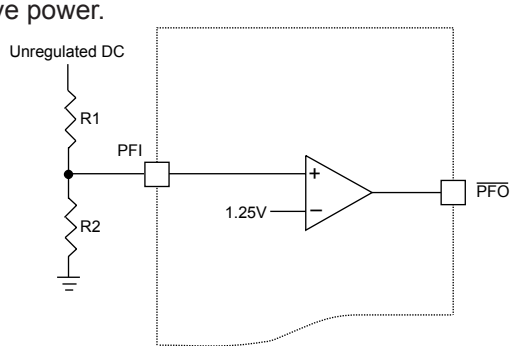


Figure 1. Power Fail Comparator

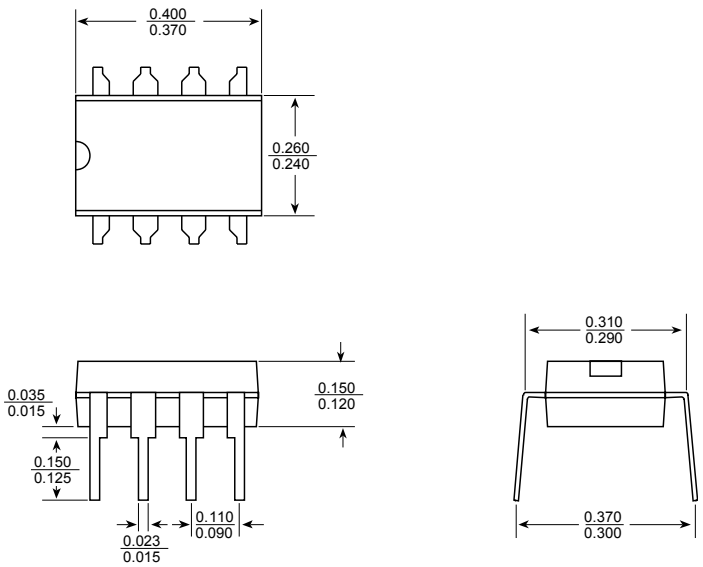
Watchdog Timer

The microprocessor can be monitored by connecting the WDI pin (watchdog input) to a bus line or an I/O line. If a transition doesn't occur on the WDI pin with in the watchdog timeout (Table 1.), the microprocessor is reset. /RESET will remain asserted for 200ms when this occurs. A minimum pulse of 100ns or any transition low-to-high or high-to-low on the WDI pin will reset the watchdog timer. The output of the watchdog timer (WDO) will remain high, if WDI sees a valid transition within the watchdog period or if VCC falls below the reset threshold as the watchdog timer is disabled when this happens.

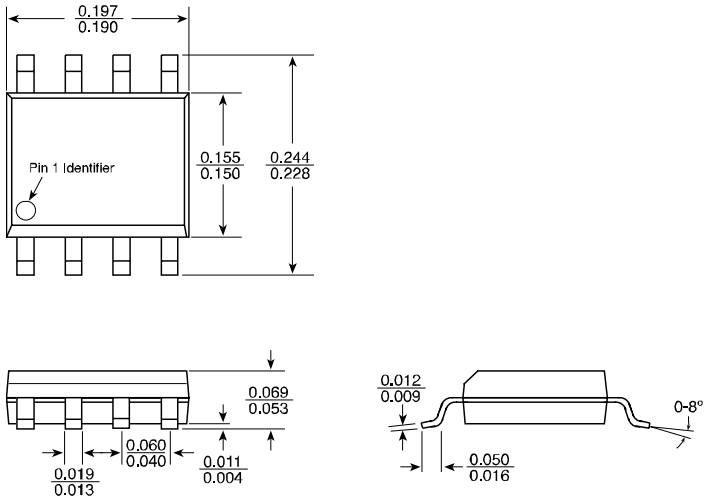
Microprocessor Reset

The /RESET pin is asserted whenever V_{CC} falls below the reset threshold voltage. The reset pin remains asserted for a period of 200ms after VCC has risen above the reset threshold voltage. The reset timeout period can also be selected by the end user, see Table 1. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. /RESET will remain valid with VCC as low as 1.4V and when auxiliary power is connected to VBATT (VBATT > 2.0V), the reset pin will remain valid with VCC from 0V to 5.5V.

Package Information



8-Pin PDIP (N)



8-Pin SOIC (M)

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