Absolute Maximum Ratings

(All voltages referenced to GND.)

Supply Voltage V+ ..... -0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{RST}$, $\overline{INT}$, P2–P5 ..... -0.3V to +6V
O0, O1, O6–O15 ..... -0.3V to V+ + 0.3V
O0, O1, O6–O15 Output Current ..... ±25mA
P2–P5 Sink Current 25mA
SDA Sink Current 10mA
INT Sink Current 10mA
Total V+ Current 50mA
Total GND Current 100mA
Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.5mW/°C over +70°C) 761.9mW
24-Pin TQFN (derate 20.8mW/°C over +70°C) 1666.7mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+	T_A = -40°C to +125°C		1.71		5.50	V
Power-On Reset Voltage	V_{POR}	V+ falling				1.6	V
Standby Current (Interface Idle)	I_{STB}	SCL and SDA and other digital inputs at V+	T_A = -40°C to +125°C		0.6	1.9	µA
Supply Current (Interface Running)	I+	f_{SCL} = 400kHz; other digital inputs at V+	T_A = -40°C to +125°C		23	55	µA
Input High-Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, P2–P5	V_{IH}	V+ < 1.8V		0.8 x V+			V
		V+ ≥ 1.8 V		0.7 x V+			
Input Low-Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, P2–P5	V_{IL}	V+ < 1.8V				0.2 x V+	V
		V+ ≥ 1.8 V				0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{RST}$, P2–P5	I_{IH}, I_{IL}	SDA, SCL, AD0, AD2, $\overline{RST}$, P0–P7 at V+ or GND, internal pullup disabled		-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{RST}$, P2–P5					10		pF
Output Low Voltage O8–O15, P0, P7	V_{OL}	V+ = 1.71V, I_{SINK} = 5mA (QSOP)			90	180	mV
		V+ = 1.71V, I_{SINK} = 5mA (TQFN)			90	230	
		V+ = 2.5V, I_{SINK} = 10mA (QSOP)			110	210	
		V+ = 2.5V, I_{SINK} = 10mA (TQFN)			110	260	
		V+ = 3.3V, I_{SINK} = 15mA (QSOP)			130	230	
		V+ = 3.3V, I_{SINK} = 15mA (TQFN)			130	280	
		V+ = 5V, I_{SINK} = 20mA (QSOP)			140	250	
		V+ = 5V, I_{SINK} = 20mA (TQFN)			140	300	
Output High Voltage O0, O1, O6–O15, P2–P5	V_{OH}	V+ = +1.71V, I_{SOURCE} = 2mA		V+ - 250	V+ - 30		mV
		V+ = +2.5V, I_{SOURCE} = 5mA		V+ - 360	V+ - 70		
		V+ = +3.3V, I_{SOURCE} = 5mA		V+ - 260	V+ - 100		
		V+ = +5V, I_{SOURCE} = 10mA		V+ - 360	V+ - 120		
Output Low-Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA				250	mV
Output Low-Voltage $\overline{INT}$	V_{OLINT}	I_{SINK} = 5mA			130	250	mV
Port Input Pullup Resistor	R_{PU}			25	40	55	kΩ

Port and Interrupt $\overline{INT}$ Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t_{PPV}	C_L ≤ 100pF			4	µs
Port Input Setup Time	t_{PSU}	C_L ≤ 100pF	0			µs
Port Input Hold Time	t_{PH}	C_L ≤ 100pF	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	C_L ≤ 100pF			4	µs
$\overline{INT}$ Reset Delay Time from STOP	t_{IP}	C_L ≤ 100pF			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	C_L ≤ 100pF			4	µs

Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

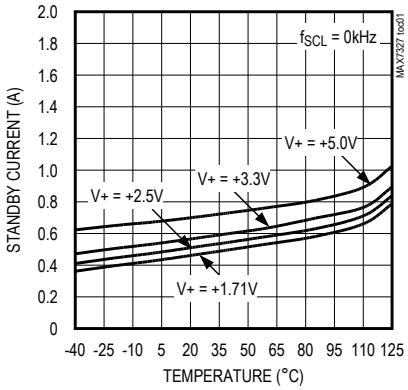
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 2)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		20 + 0.1C_b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		20 + 0.1C_b	300	ns
Fall Time of SDA Transmitting	$t_{F,TX}$	(Notes 3, 4)		20 + 0.1C_b	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF
$\overline{RST}$ Pulse Width	t_W		500			ns
$\overline{RST}$ Rising to START Condition Setup Time	$t_{\overline{RST}}$		1			µs

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 3: Guaranteed by design.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V+ and 0.7 x V+ with I_{SINK} ≤ 6mA.
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

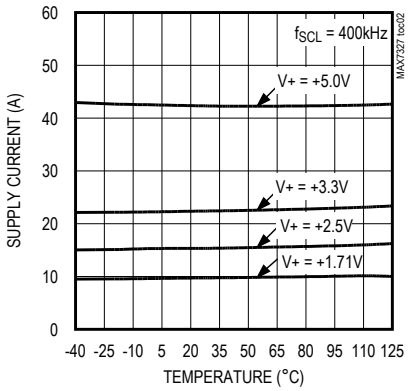
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

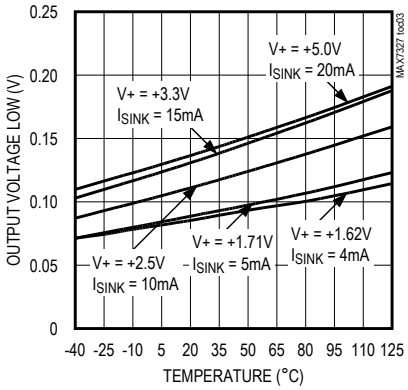
STANDBY CURRENT vs. TEMPERATURE



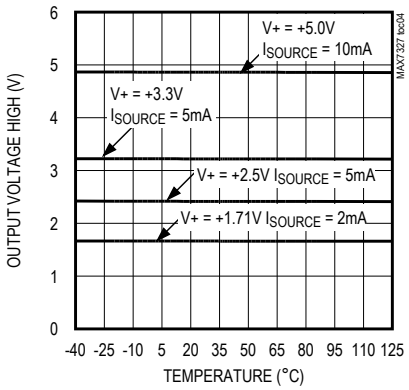
SUPPLY CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE LOW vs. TEMPERATURE



OUTPUT VOLTAGE HIGH vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1	22	$\overline{INT}$	Active-Low Interrupt Output. $\overline{INT}$ is an open-drain output.
2	23	$\overline{RST}$	Active-Low Reset Input. Drive $\overline{RST}$ low to clear the 2-wire interface.
3, 21	24, 18	AD2, AD0	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V+, SCL, or SDA to give four logic combinations (see Tables 2 and 3).
4, 5, 10, 11, 13–20	1, 2, 7, 8, 10–17	O0, O1, O6–O15	Output Ports. O0, O1, O6–O15 are push-pull outputs rated at 20mA.
6–9	3–6	P2–P5	P2–P5 Open-Drain I/Os
12	9	GND	Ground
22	19	SCL	I²C-Compatible Serial Clock Input
23	20	SDA	I²C-Compatible Serial Data I/O
24	21	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047µF ceramic capacitor.
—	EP	EP	Exposed Pad. Connect exposed pad to GND.

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7327 is a general-purpose port expander operating from a +1.71V to +5.5V supply that provides 12 push-pull output ports with a 20mA sink, 10mA source drive capability, and four open-drain I/O ports with a 20mA sink capability. The four open-drain outputs are overvoltage protected to +6V.

The MAX7327 is set to two of 32 I²C slave addresses (see Tables 2 and 3) using address inputs AD2 and AD0, and is accessed over an I²C serial interface up to 400kHz. Eight push-pull outputs use a different slave address from the other four push-pull outputs and the open-drain I/Os. The eight push-pull outputs (O8–O15) use the 101xxxx addresses while the four outputs (O0, O1, O6, and O7) and the open-drain I/Os (P2–P5) use addresses with 110xxxx. The $\overline{RST}$ input clears the serial interface in case of a bus lockup, terminating any serial transaction to or from the MAX7327.

Any of the four open-drain ports can be configured as a logic input by setting the port output logic-high (logic-high for an open-drain output is high impedance). When the MAX7327 is read through the serial interface, the actual logic levels at the ports are read back.

Table 1. MAX7319–MAX7329 Family Comparison

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	CONFIGURATION
16-PORT EXPANDERS						
MAX7324	101xxxx and 110xxxx	8	Yes	—	8	8 inputs and 8 push-pull outputs version: 8 input ports with programmable latching transition detection interrupt and selectable pullups. 8 push-pull outputs with selectable default logic levels. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even if only for a transient) since the ports were last read.
MAX7325		Up to 8	—	Up to 8	8	8 I/O and 8 push-pull outputs version: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 8 push-pull outputs with selectable default logic levels. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors, but pullups draw current when output is low. Any open-drain port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which open-drain port inputs have changed (even if only for a transient) since the ports were last read.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	CONFIGURATION
MAX7326	101xxxx and 110xxxx	4	Yes	—	12	4 input-only, 12 push-pull output versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups. 12 push-pull outputs with selectable default logic levels. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even if only for a transient) since the ports were last read.
MAX7327		Up to 4	—	Up to 4	12	4 I/O, 12 push-pull output versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 12 push-pull outputs with selectable default logic levels. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors, but pullups draw current when output is low. Any open-drain port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which open-drain port inputs have changed (even if only for a transient) since the ports were last read.
8-PORT EXPANDERS						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: 8 input ports with programmable latching transition detection interrupt and selectable pullups.
MAX7320	101xxxx	—	—	—	8	Output-only versions: 8 push-pull outputs with selectable power-up default levels.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups.
MAX7322	110xxxx	4	Yes	—	4	4 input-only, 4 output-only versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	CONFIGURATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	4 I/O, 4 output-only versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	PCF8574-, PCF8574A-compatible versions: 8 open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports.

The four open-drain ports offer latching transition detection functionality when used as inputs. All input ports are continuously monitored for changes. An input change sets 1 of 4 flag bits that identify the changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7327.

A latching interrupt output ($\overline{INT}$) automatically flags data changes on any of the I/O ports used as inputs through an interrupt mask register. Data changes on any input port forces $\overline{INT}$ to a logic-low. Interrupt output $\overline{INT}$ is deasserted when the MAX7327 is next accessed through the serial interface.

Internal pullup resistors to V+ are selected by the address select inputs, AD0 and AD2. Pullups are enabled on the input ports in groups of two (see Table 2). Use the slave address selection to ensure that I/O ports used as inputs are logic-high on power-up. I/O ports with internal pullups enabled default to a logic-high output state. I/O ports with internal pullups disabled default to a logic-low output state.

Output port power-up logic levels are selected by the address select inputs (AD0 and AD2). Ports default to logic-high or logic-low on power-up in groups of two (see Tables 2 and 3).

Initial Power-Up

On power-up, the default states of the 12 push-pull output ports and the four open-drain I/O ports are set according to the I²C slave address selection inputs, AD0 and AD2 (see Tables 2 and 3). For I/O ports used as inputs, ensure that the default states are logic-high; therefore, the I/O ports power up in the high-impedance state. All I/O ports configured with pullups enabled also have a logic-high default state. On power-up, the transition detection logic is reset, and $\overline{INT}$ is deasserted. The transition flags are cleared, indicating no data changes.

Power-On Reset (POR)

The MAX7327 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. When V+ rises above V_{POR} (1.6V max), the POR circuit releases the registers and 2-wire interface for normal operation. When V+ drops to less than V_{POR}, the MAX7327 resets all register contents to the POR defaults (Tables 2 and 3).

$\overline{RST}$ Input

The active-low reset input ($\overline{RST}$) operates as a hardware reset that voids any I²C transaction involving the MAX7327, forcing the MAX7327 into the I²C STOP condition. A reset does not affect the interrupt output ($\overline{INT}$).

Standby Mode

When the serial interface is idle, the MAX7327 automatically enters standby mode, drawing minimal supply current.

Slave Address, Power-Up Default Logic Levels, and Input Pullup Selection

Address inputs AD0 and AD2 determine the MAX7327 slave address and select which inputs have pullup resistors. Pullups are enabled on the input ports in groups of two (see Table 2).

The MAX7327 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7327. The MAX7327 distinguishes whether address inputs AD0 and AD2 are connected to SDA or SCL instead of fixed-logic levels V+ or GND during the transmission. The MAX7327 slave

address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7327 cannot decode the address inputs AD0 and AD2 fully until the first I²C transmission. AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection is used to determine the power-up default states of the output ports, I/O port initial logic state, and whether pullups are enabled. At power-up, the I²C SDA and SCL bus interface lines are high impedance at the I/O pins of every device (master or slave) connected to the bus, including the MAX7327. This is guaranteed as part of the I²C specification. Therefore, when address inputs AD0 and AD2 are connected to SDA or SCL during power-up, they appear to be connected to V+. The pullup selection logic uses AD0 to select whether pullups are enabled for ports P2 and P3, and uses AD2 to select whether pullups are enabled for ports P4 and P5. The rule is that a logic-high, SDA, or SCL connection selects the pullups and sets the logic state to high. A logic-low deselects the pullups and sets the default logic state to low. The pullup configuration is correct on power-up for a standard I²C configuration, where SDA or SCL are pulled up to V+ by the external I²C pullup resistors.

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true; for example, in applications in which there is legitimate bus activity during power-up. If SDA and SCL are terminated with pullup resistors to a different supply voltage to the MAX7327's supply voltage, and if that pullup supply rises later than the MAX7327's supply, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD0 and AD2 to V+ or GND (shown in **bold** in Tables 2 and 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, an unexpected combination of pullups might be asserted until the first I²C transmission (to any device, not necessarily the MAX7327) is put on the bus.

Table 2. MAX7327 Address Map for Outputs O0, O1, O6, O7, and Ports P2–P5

PIN CONNECTION		DEVICE ADDRESS							PORTS POWER-UP DEFAULT								40kΩ INPUT PULLUPS ENABLED							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**O7**	**O6**	**P5**	**P4**	**P3**	**P2**	**O1**	**O0**	**O7**	**O6**	**P5**	**P4**	**P3**	**P2**	**O1**	**O0**
SCL	GND	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	Pullups are not enabled for push-pull outputs		Y	Y	—	—	Pullups are not enabled for push-pull outputs	
SCL	V+	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
SCL	SCL	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
SCL	SDA	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
SDA	GND	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0			Y	Y	—	—		
SDA	V+	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
SDA	SCL	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
SDA	SDA	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
GND	**GND**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**			**—**	**—**	**—**	**—**		
GND	V+	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**			**—**	**—**	**Y**	**Y**		
GND	SCL	1	1	0	1	0	1	0	0	0	0	0	1	1	1	1			—	—	Y	Y		
GND	SDA	1	1	0	1	0	1	1	0	0	0	0	1	1	1	1			—	—	Y	Y		
V+	**GND**	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**			**Y**	**Y**	**—**	**—**		
V+	V+	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**			**Y**	**Y**	**Y**	**Y**		
V+	SCL	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1			Y	Y	Y	Y		
V+	SDA	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1			Y	Y	Y	Y		

Table 3. MAX7327 Address Map for Outputs O8–O15

PIN CONNECTION		DEVICE ADDRESS							OUTPUTS POWER-UP DEFAULT							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**O15**	**O14**	**O13**	**O12**	**O11**	**O10**	**O9**	**O8**
SCL	GND	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0
SCL	V+	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1
SCL	SCL	1	0	1	0	0	1	0	1	1	1	1	1	1	1	1
SCL	SDA	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
SDA	GND	1	0	1	0	1	0	0	1	1	1	1	0	0	0	0
SDA	V+	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1
SDA	SCL	1	0	1	0	1	1	0	1	1	1	1	1	1	1	1
SDA	SDA	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
GND	GND	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
GND	**V+**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
GND	**SCL**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
GND	SDA	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1
V+	**GND**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
V+	**V+**	1	**0**	1	1	1	**0**	1	**1**	**1**	**1**	**1**	**1**	1	1	1
V+	SCL	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1
V+	SDA	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

I/O Port Inputs

I/O port inputs switch at CMOS logic levels as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

I/O Port Input Transition Detection

All I/O ports configured as inputs are monitored for changes since the expander was last accessed through the serial interface. The state of the ports is stored in an internal "snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port input, $\overline{INT}$ is asserted to signal a state change. The input ports are sampled (internally latched into the snapshot register) and the old transition flags cleared during the I²C acknowledge of every MAX7327 read and write access. The previous port-transition flags are read through the serial interface as the second byte of a 2-byte read sequence.

A long read sequence (more than 2 bytes) can be used to poll the expander continuously without the overhead of resending the slave address. If more than 2 bytes are read from the expander, the expander repeatedly returns the 2 bytes of input port data followed by the transition flags. The inputs are repeatedly resampled and the transition flags repeatedly reset for each pair of bytes read. All changes that occur during a long read sequence are detected and reported.

The $\overline{INT}$ output is not reasserted during a read sequence to avoid recursive reentry into an interrupt service routine. Instead, if a data change occurs that would normally cause the $\overline{INT}$ output to be set, the $\overline{INT}$ assertion is delayed until the STOP condition. $\overline{INT}$ is not reasserted upon a STOP condition if the changed input data is read before the STOP occurs. The $\overline{INT}$ logic ensures that unnecessary interrupts are not asserted, yet data changes are detected and reported no matter when the change occurs.

Serial Interface

Serial Addressing

The MAX7327 operates as a slave that sends and receives data through an I2C interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7327 and generates the SCL clock that synchronizes the data transfer (Figure 1).

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7327's 7-bit slave addresses plus R/$\overline{W}$ bits, one or more data bytes, and finally a STOP condition (Figure 2).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

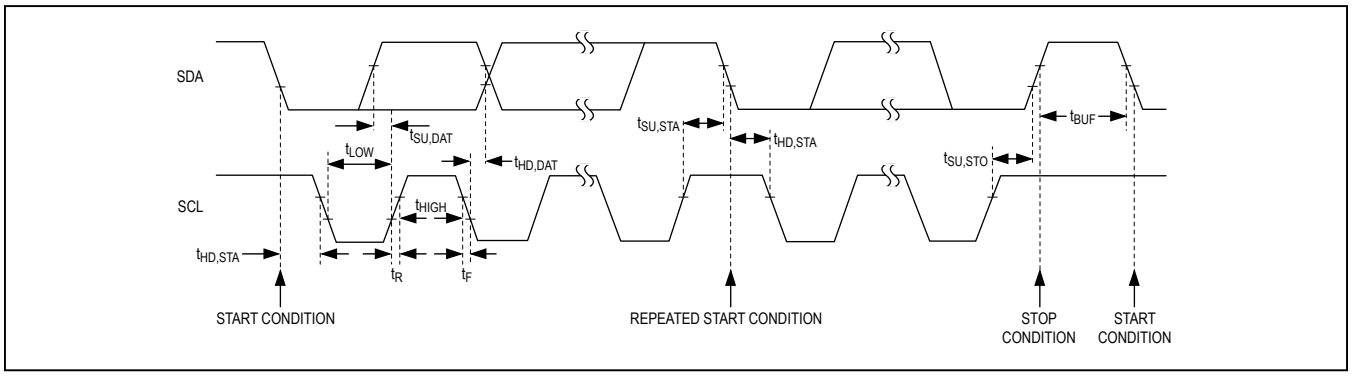


Figure 1. 2-Wire Serial Interface Timing Details

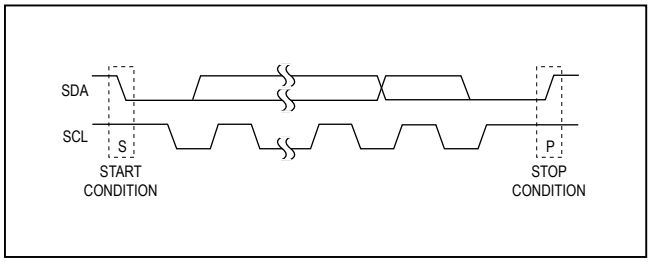


Figure 2. Start and Stop Conditions

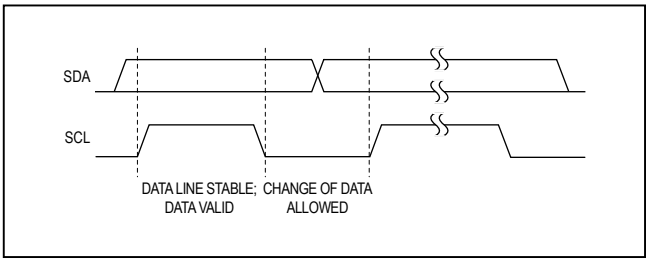


Figure 3. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7327, the MAX7327 generates the acknowledge bit because the device is the recipient. When the MAX7327 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7327 has two different 7-bit slave addresses (Figure 5). The addresses are different to communicate to the eight push-pull outputs (O8–O15) or the other eight I/Os. The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command and high for a read command.

The first (A6), second (A5), and third (A4) bits of the MAX7327 slave address are always 1, 1, and 0 (O0, O1, P2–P5, O6, O7) or 1, 0, and 1 (O8–O15). Connect AD0 and AD2 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7327 has 16 possible slave addresses (Tables 2 and 3), allowing up to 16 MAX7327 devices on an I²C bus.

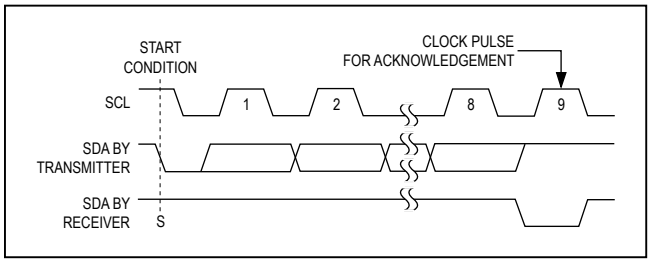


Figure 4. Acknowledge

Accessing the MAX7327

The MAX7327 is a combination of MAX7320 and MAX7323. The group A of eight ports (O0, O1, P2–P5, O6, and O7) corresponding to those of the MAX7323 and the group B of eight ports (O8–O15) corresponding to those of the MAX7320 are read/write separately through their own addresses, as shown by Tables 2 and 3, respectively.

A **single-byte read** from the group A ports of the MAX7327 returns the status of the four I/O ports and the four output ports (read back as inputs), and clear both the internal transition flags and the $\overline{INT}$ output when the master acknowledges the slave address byte.

A 2-byte read from the group A ports of the MAX7327 returns the status of the four I/O ports and the four output ports (as for a single byte read), followed by the four transition flags for the four I/O ports. The internal transition flags and the $\overline{INT}$ output are cleared automatically when the master acknowledges the slave address byte (but the previous transition flag data is sent as the second byte).

A multibyte read (more than 2 bytes before the I²C STOP bit) from the group A ports of the MAX7327 repeatedly returns the port data, alternating with the transition flags. As the port data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing I/O ports.

If a port input data change occurs during the read sequence, then $\overline{INT}$ is reasserted during the I²C STOP bit. The MAX7327 does not generate another interrupt during a single-byte or multibyte MAX7327 read routine.

Input port data is sampled during the preceding I²C acknowledge bit (the acknowledge bit for the I²C slave address in the case of a single-byte or 2-byte read).

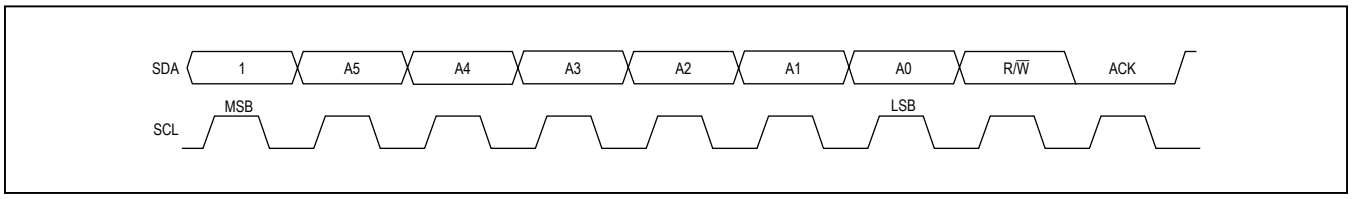


Figure 5. Slave Address

A **single-byte read** from the group B ports of the MAX7327 returns the status of the eight output ports, read back as inputs.

A **2-byte read** from the group B ports of the MAX7327 repeatedly returns the status of the eight output ports, read back as inputs.

A **multibyte read** (more than 2 bytes before the I²C STOP bit) from the group B ports of the MAX7327 repeatedly returns the status of the eight output ports, read back as inputs.

A **single-byte write** to the group A or B ports of the MAX7327 sets the logic state of all eight ports.

A **multibyte write** to the group A or B ports of the MAX7327 repeatedly sets the logic state of all eight ports.

Reading the MAX7327

A read from the group A ports of the MAX7327 starts with the master transmitting the port group's slave address with the R/$\overline{W}$ bit set to high. The MAX7327 acknowledges the slave address, and samples the status of the ports during the acknowledge bit. $\overline{INT}$ goes high during the slave address acknowledge. The master can then issue a STOP condition after the acknowledge. The snapshot is taken, and the $\overline{INT}$ status remains unchanged, if the master terminates the serial transition with a no-acknowledge.

When the master reads one byte from the group A ports of the MAX7327 and subsequently issues a STOP condition (Figure 6), the MAX7327 transmits the current port data, clears the change flags, and resets the tran-

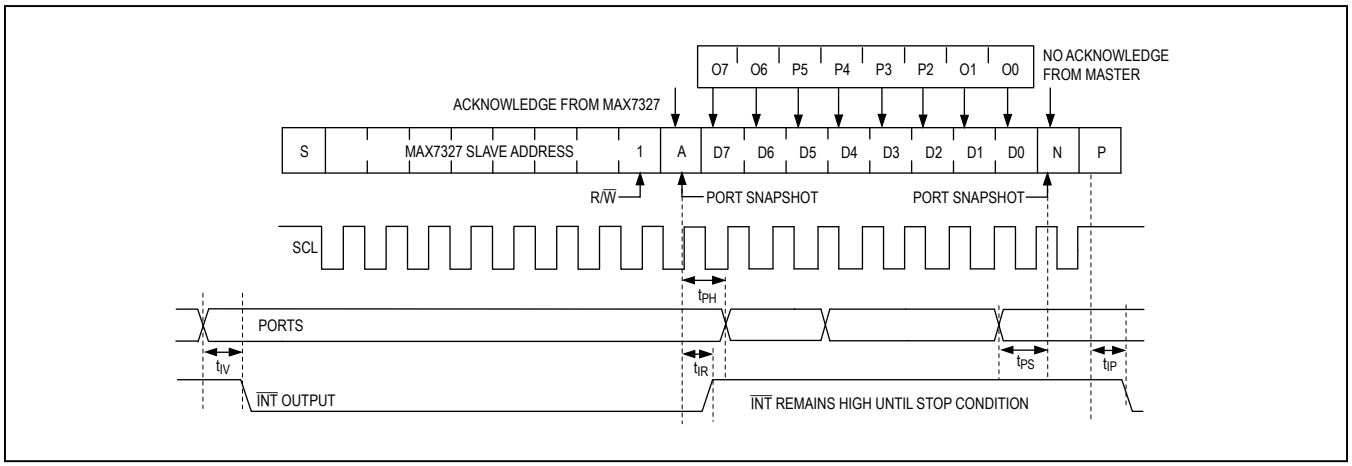


Figure 6. Reading Group A Ports of the MAX7327 (1 Data Byte)

sition detection. $\overline{INT}$ deasserts during the slave acknowledge. The new snapshot data is the current port data transmitted to the master, and therefore, port changes occuring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

When the master reads 2 bytes from the group A ports of the MAX7327 and subsequently issues a STOP condition (Figure 7), the MAX7327 transmits the current port data, followed by the change flags. The change flags are then cleared, and transition detection is reset. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge. The new snapshot data is the current port data transmitted to the master, and therefore, port changes occuring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

A read from the group B ports of the MAX7327 starts with the master transmitting the group's slave address with the R/$\overline{W}$ bit set high. The MAX7327 acknowledges the slave address, and samples the logic state of the output ports during the acknowledge bit. The master can read one or more bytes from the group B ports of the MAX7327 and then issue a STOP condition (Figure 8). The MAX7327 transmits the current port data, read back from the actual port outputs (not the port output latches) during the acknowledge. If a port is forced to a logic state other than its programmed state, the readback reflects this. If driving a capacitive load, the readback port-level verification algorithms may need to take the RC rise/fall time into account.

Typically, the master reads one byte from the group B ports of the MAX7327, then issues a STOP condition (Figure 8). However, the master can read two or more

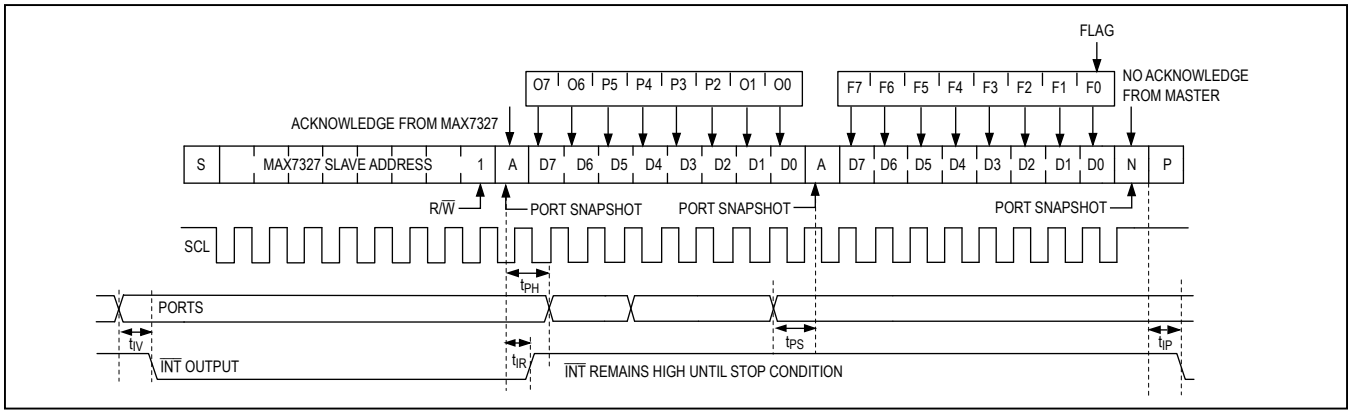


Figure 7. Reading Group A Ports of the MAX7327 (2 Data Bytes)

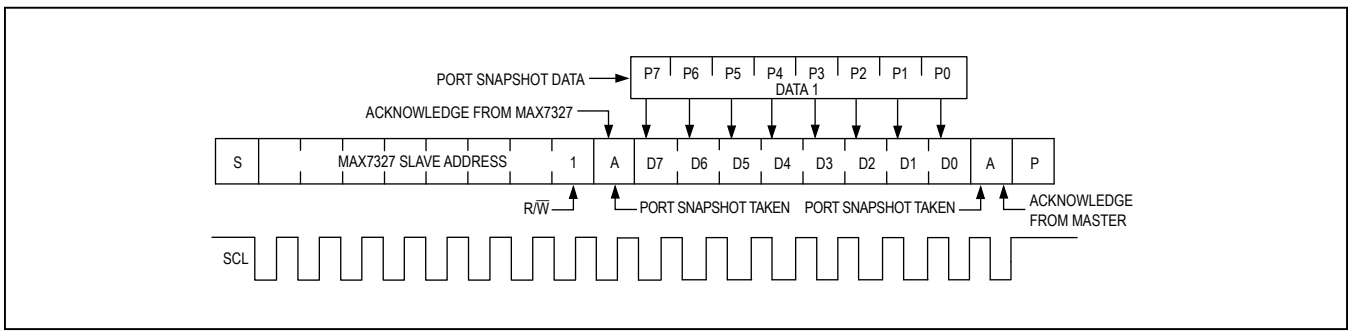


Figure 8. Reading Group B Ports of MAX7327

bytes from the group B ports of the MAX7327, then issue a STOP condition. In this case, the MAX7327 resamples the port outputs during each acknowledge and transmits the new data each time.

Writing to the MAX7327

A write to the group A or B ports of the MAX7327 starts with the master transmitting the group's slave address with the R/$\overline{W}$ bit set low. The MAX7327 acknowledges the slave address and samples the ports during the acknowledge bit. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge only when it writes to the group A ports. The master can now transmit one or more bytes of data. The MAX7327 acknowledges these subsequent bytes of data and updates the corresponding group's ports with each new byte until the master issues a STOP condition (Figure 9).

Applications Information

Port Input and I²C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7327's SDA, SCL, AD0, AD2, $\overline{RST}$, $\overline{INT}$, and the four I/O ports (P2–P5) are overvoltage protected to +6V, independent of V+. This allows the MAX7327 to operate from a lower supply voltage, such as +3.3V, while the I²C interface and/or some of the four I/O ports are driven from a higher logic level, such as +5V.

The MAX7327 can operate from a higher supply voltage, such as +3V, while the I²C interface and/or some of the four I/O ports (P2–P5) are driven from a lower logic level, such as +2.5V. For V+ < 1.8V, apply a minimum voltage of 0.8 x V+ to assert a logic-high on any input. For a V+ ≥ 1.8V, apply a voltage of 0.7 x V+ to assert a logic-high. For example, a MAX7327 operating from a +5V supply may not recognize a +3.3V nominal logic-high. One solution for input-level translation is to drive MAX7327 inputs from open-drain outputs. Use a pullup resistor to V+ or a higher supply to ensure a high logic voltage greater than 0.7 x V+.

Port Output Signal Level Translation

The open-drain output architecture allows for level translation to higher or lower voltages than the MAX7327's supply. Use an external pullup resistor on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to +6V, and the resistor value chosen to ensure no more than 20mA to be sunk in logic-low condition. For interfacing CMOS inputs, a pullup resistor value of 220kΩ is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Each of the 12 push-pull output ports has protection diodes to V+ and GND. When a port output is driven to a voltage higher than V+ or lower than GND, the appropriate protection diode clamps the output to a diode drop above V+ or below GND. When the MAX7327 is powered down (V+ = 0V), every output port's protection diodes to

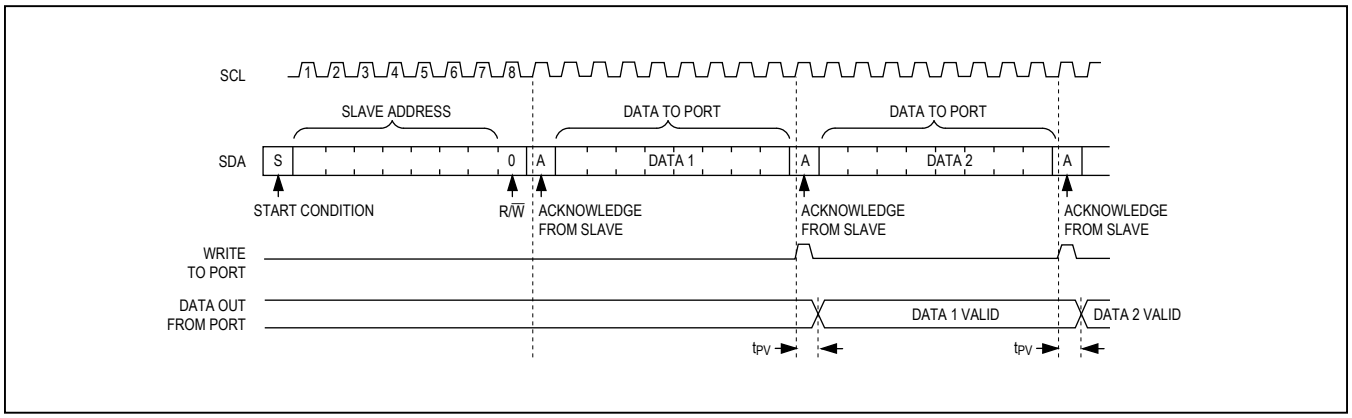


Figure 9. Writing the MAX7327

V+ and GND continue to appear as a diode clamp from each output to GND (Figure 10).

Each of the four P2–P5 I/O ports has a protection diode to GND (Figure 11). When a port output is driven to a voltage lower than GND, the protection diode clamps the output to a diode drop below GND.

Each of the four P2–P5 I/O ports also has a 40kΩ (typ) pullup resistor that can be enabled or disabled. When a port input is driven to a voltage higher than V+, the body diode of the pullup enable switch conducts and the 40kΩ pullup resistor is enabled. When the MAX7327 is powered down (V+ = 0V), each I/O port appears as a 40kΩ resistor in series with a diode connected to 0V. Input ports are protected to +6V under any of these circumstances (Figure 11).

Driving LED Loads

When driving LEDs from one of the 12 push-pull outputs, a resistor must be fitted in series with the LED to limit the LED current to no more than 20mA. Connect the LED cathode to the MAX7327 port, and the LED anode to V+ through the series current-limiting resistor, R_{LED}. Set the port output low to light the LED. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).

V_{SUPPLY} is the supply voltage used to drive the LED (V).

V_{LED} is the forward voltage of the LED (V).

V_{OL} is the output low voltage of the MAX7327 when sinking I_{LED} (V).

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 10mA from a +5V supply:

$$R_{LED} = (5 - 2.2 - 0.1) / 0.01 = 270\Omega$$

Driving Load Currents Higher than 20mA

The MAX7327 can be used to drive loads such as relays that draw more than 20mA by paralleling outputs. Use at least one output per 20mA of load current; for example, a 5V 330mW relay draws 66mA, and therefore, requires four paralleled outputs. Any combination of outputs can be used as part of a load-sharing design because any combination of ports can be set or cleared at the same time by writing to the MAX7327. Do not exceed a total sink current of 100mA for the device.

The MAX7327 must be protected from the negative voltage transient generated when switching off inductive loads (such as relays), by connecting a reverse-biased diode across the inductive load. Choose the peak current for the diode to be greater than the inductive load's operating current.

Power-Supply Considerations

The MAX7327 operates with a supply voltage of +1.71V to +5.5V. Bypass the supply to GND with a ceramic capacitor of at least 0.047µF as close as possible to the device. For the TQFN version, additionally connect the exposed pad to GND.

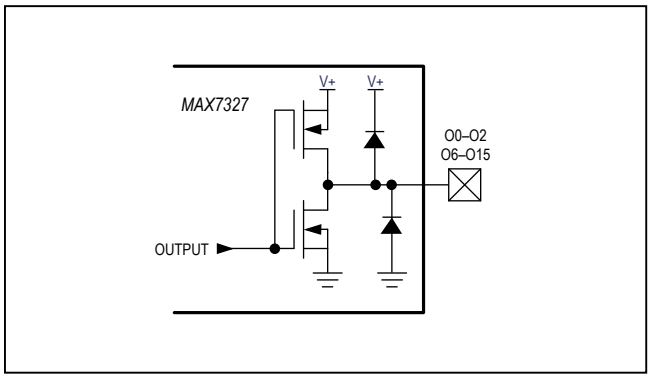


Figure 10. MAX7327 Push-Pull Output Port Structure

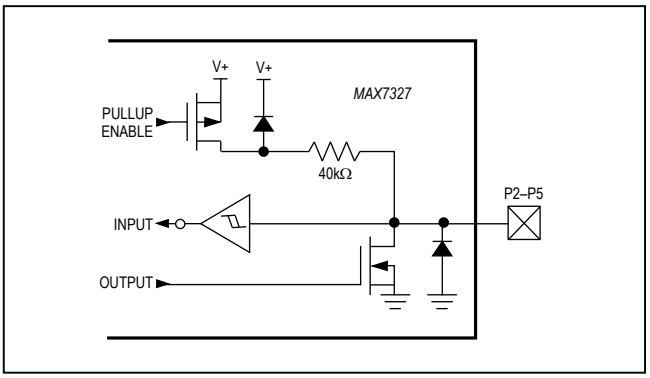
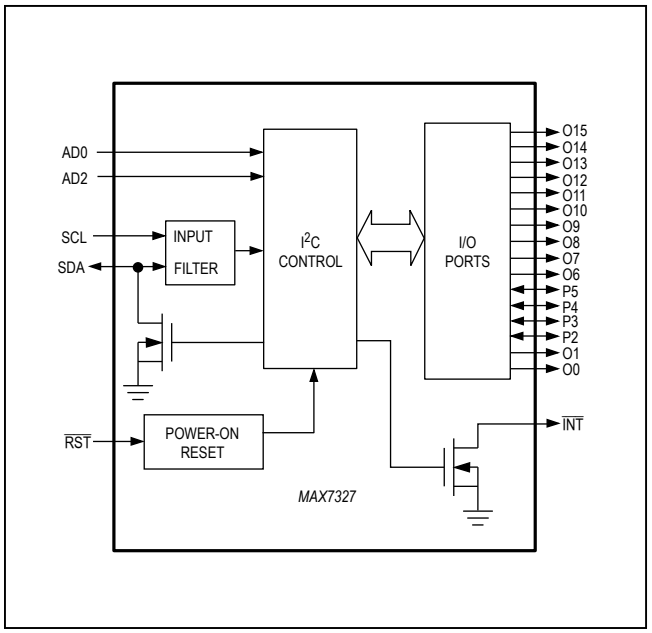
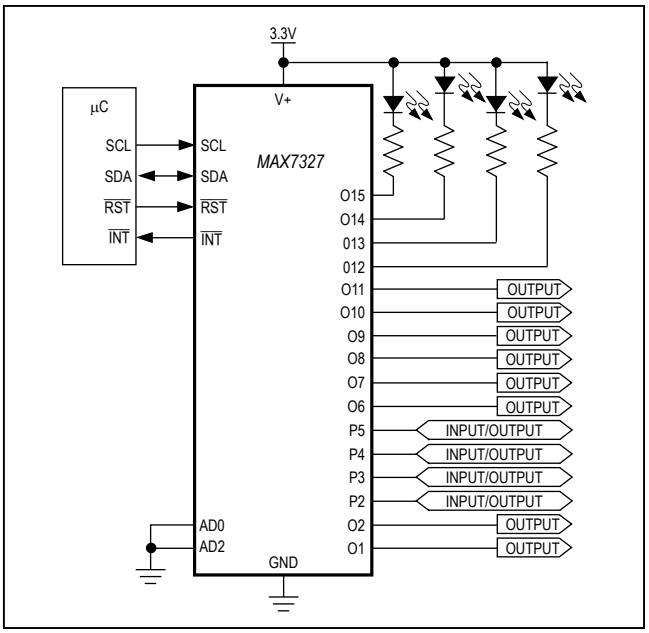


Figure 11. MAX7327 Open-Drain I/O Port Structure

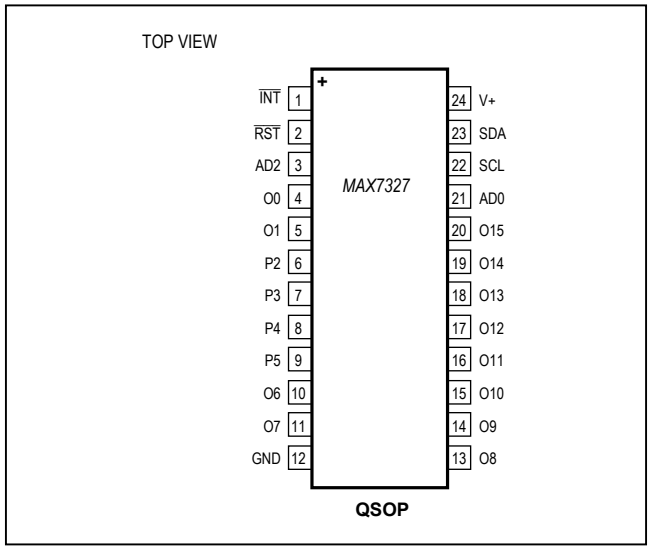
Functional Diagram



Typical Application Circuit



Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 QSOP	E24+1	21-0055	90-0172
24 TQFN (4mm x 4mm)	T2444+3	21-0139	—
24 TQFN (3.5mm x 3.5mm)	T243A3+1	21-0188	90-0122

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/06	Initial release	—
1	7/14	No /V OPNs; removed automotive reference from *Applications* section; updated *Package Information*	1, 18–20

