

2-Wire-Interfaced 16-Bit I/O Port Expander with Interrupt and Hot-Insertion Protection

ABSOLUTE MAXIMUM RATINGS

V⁺ to GND-0.3V to +6V
 I/O0–I/O15 as Inputs(GND - 0.3V) to +6V
 SCL, SDA, AD0, AD1, AD2, $\overline{\text{INT}}$ (GND - 0.3V) to +6V
 Maximum V⁺ Current+250mA
 Maximum GND Current-250mA
 DC Input Current on I/O0–I/O15±20mA
 DC Output Current on I/O0–I/O15±80mA

Continuous Power Dissipation (T_A = +70°C)

24-Pin Wide SO (derate 11.8mW/°C above +70°C)941mW
 24-Pin SSOP (derate 8.0mW/°C above +70°C)640mW
 24-Pin TSSOP (derate 12.2mW/°C above +70°C)975mW
 24-Pin Thin QFN (derate 20.8mW/°C above +70°C) .1668mW
 Operating Temperature Range-40°C to +125°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V⁺ = 2V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V⁺ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V ⁺			2		5.5	V
Supply Current	I ⁺	All I/Os unloaded, f _{SCL} = 400kHz	V ⁺ = 2V		23	35	μA
			V ⁺ = 3.3V		43	60	
			V ⁺ = 5.5V		80	120	
Standby Current	I _{STBY}	All I/Os unloaded, f _{SCL} = 0	V ⁺ = 2V		2.3	11	μA
			V ⁺ = 3.3V		2.9	12	
			V ⁺ = 5.5V		3.8	15.5	
Power-On Reset Voltage	V _{POR}				1.4	1.7	V
SCL, SDA							
Input Voltage Low	V _{IL}			0.3 x V ⁺			V
Input Voltage High	V _{IH}			0.7 x V ⁺			V
Low-Level Output Voltage	V _{OL}	I _{SINK} = 6mA				0.4	V
Leakage Current	I _L			-1		+1	μA
Input Capacitance				10			pF
I/O₀							
Input Voltage Low	V _{IL}			0.8			V
Input Voltage High	V _{IH}			1.8			V
Input Leakage Current		T _A = -40°C to +85°C		-1		+1	μA
Low-Level Output Current	I _{SINK}	V ⁺ = 2V, V _{OL} = 0.5V		8.5	17		mA
		V ⁺ = 3.3V, V _{OL} = 0.5V		17	32		
		V ⁺ = 5V, V _{OL} = 0.5V			43		
High Output Current	I _{SOURCE}	V ⁺ = 3.3V, V _{OH} = 2.4V		29	41		mA
		V ⁺ = 5V, V _{OH} = 4.5V			31		
AD0, AD1, AD2							
Input Voltage Low	V _{IL}			0.3 x V ⁺			V
Input Voltage High	V _{IH}			0.7 x V ⁺			V

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DC ELECTRICAL CHARACTERISTICS (continued)

(V⁺ = 2V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V⁺ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current			-1		+1	μA
Input Capacitance				4		pF
INT						
Low-Level Output Current	I _{OL}	V _{OL} = 0.4V	6			mA

AC ELECTRICAL CHARACTERISTICS

(V⁺ = 2V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f _{SCL}	(Note 2)			400	kHz
Bus Timeout	t _{TIMEOUT}		29		61	ms
Bus Free Time Between STOP and START Conditions	t _{BUF}	Figure 2	1.3			μs
Hold Time (Repeated) START Condition	t _{HD,STA}	Figure 2	0.6			μs
Repeated START Condition Setup Time	t _{SU,STA}	Figure 2	0.6			μs
STOP Condition Setup Time	t _{SU,STO}	Figure 2	0.6			μs
Data Hold Time	t _{HD,DAT}	Figure 2 (Note 3)			0.9	μs
Data Setup Time	t _{SU,DAT}	Figure 2	100			ns
SCL Low Period	t _{LOW}	Figure 2	1.3			μs
SCL High Period	t _{HIGH}	Figure 2	0.7			μs
SDA Fall Time	t _F	Figure 2 (Notes 4, 5)	V ₊ < 3.3V		500	ns
			V ₊ ≥ 3.3V		250	
Pulse Width of Spike Suppressed	t _{SP}	(Note 6)		50		ns
PORT TIMING						
Output Data Valid	t _{PV}	Figure 7			3	μs
Input Data Setup Time			27			μs
Input Data Hold Time			0			μs
INTERRUPT TIMING						
Interrupt Valid	t _{IV}	Figure 9			30.5	μs
Interrupt Reset	t _{IR}	Figure 9			2	μs

Note 1: All parameters are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Minimum SCL clock frequency is limited by the MAX7312 bus timeout feature, which resets the serial bus interface if either SDA or SCL is held low for a minimum of 25ms. Disable bus timeout feature for DC operation.

Note 3: A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

Note 4: C_B = total capacitance of one bus line in pF.

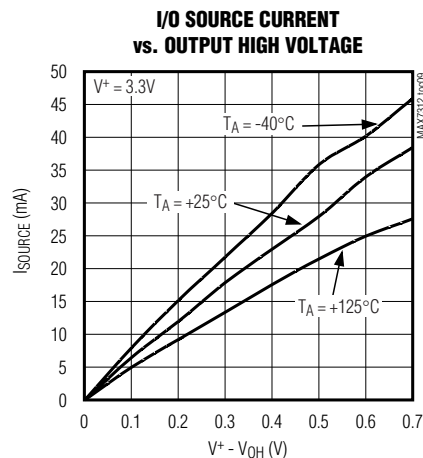
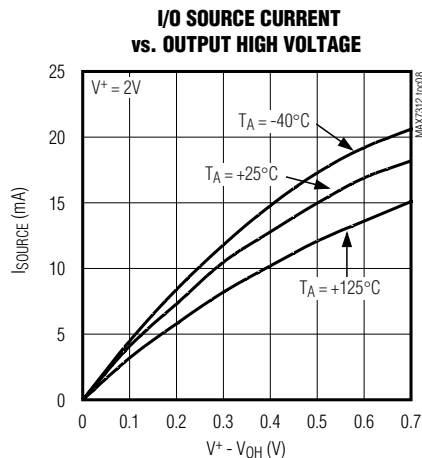
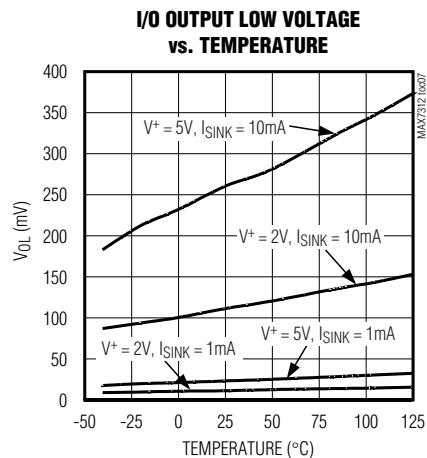
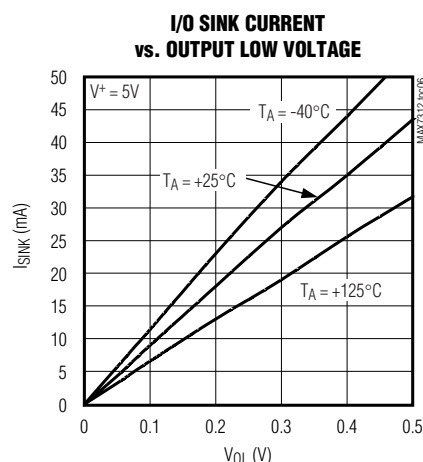
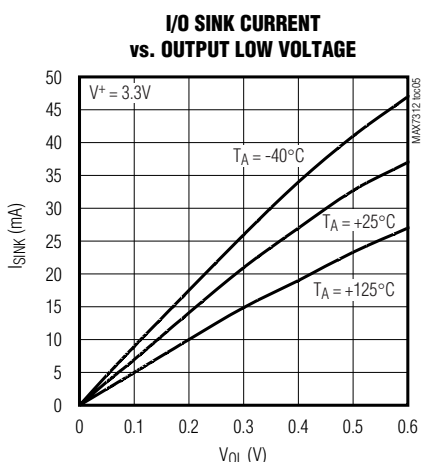
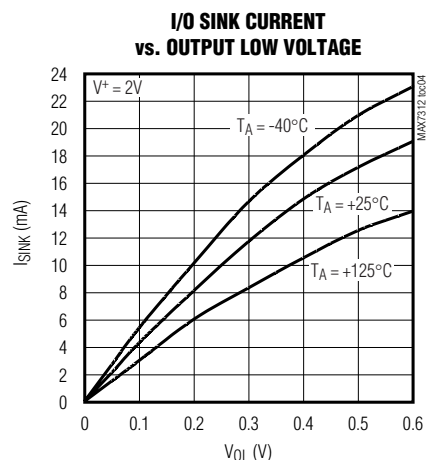
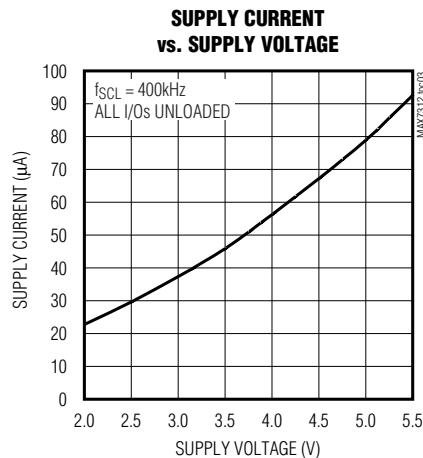
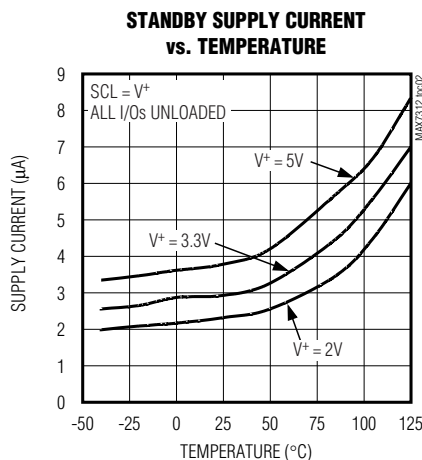
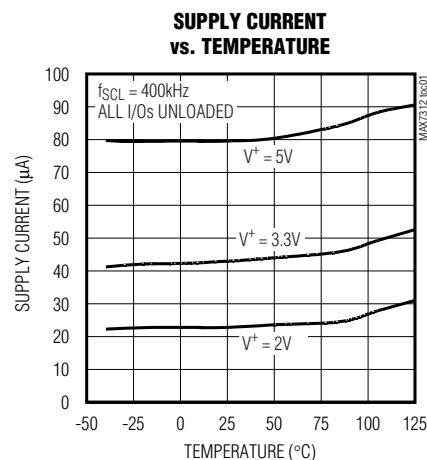
Note 5: The maximum t_F for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_F is specified at 250ns. This allows series protection resistors to be connected between the SDA and SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.

Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

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Typical Operating Characteristics

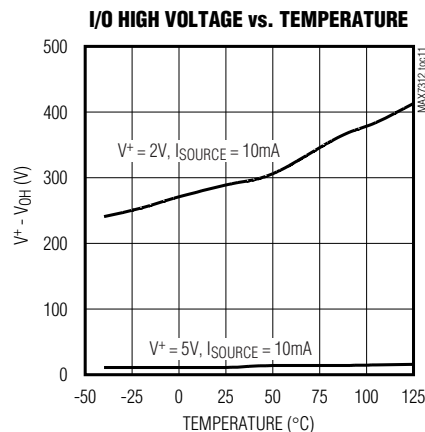
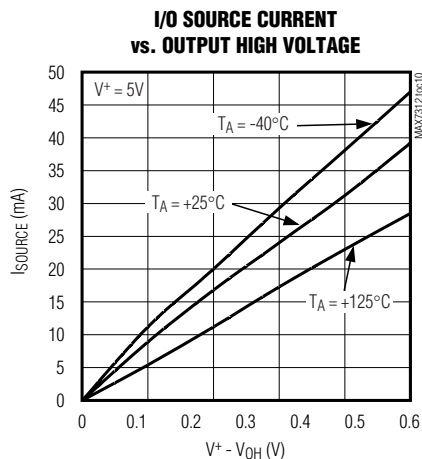
($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
TSSOP/ SSOP/SO	THIN QFN		
1	22	$\overline{\text{INT}}$	Interrupt Output (Open Drain)
2	23	AD1	Address Input 1
3	24	AD2	Address Input 2
4–11	1–8	I/O0–I/O7	Input/Output Port 1
12	9	GND	Supply Ground
13–20	10–17	I/O8–I/O15	Input/Output Port 2
21	18	AD0	Address Input 0
22	19	SCL	Serial Clock Line
23	20	SDA	Serial Data Line
24	21	V^+	Supply Voltage. Bypass with a $0.047\mu\text{F}$ capacitor to GND.
—	PAD	Exposed pad	Exposed Pad on Package Underside. Connect to GND.

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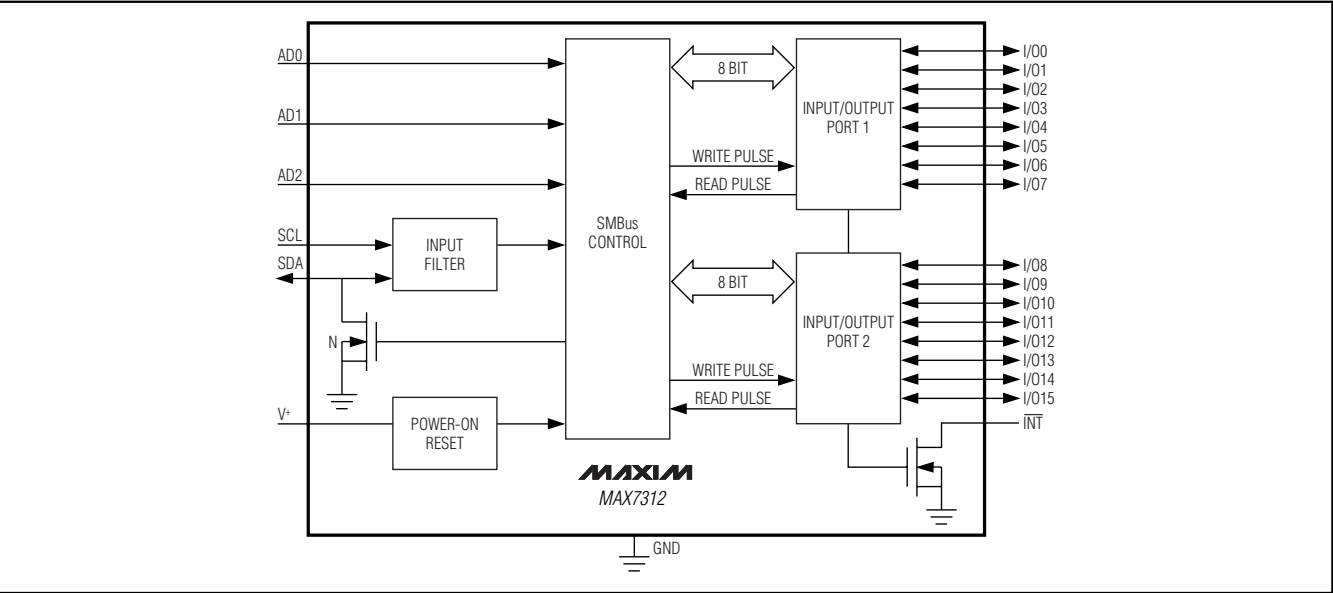


Figure 1. MAX7312 Block Diagram

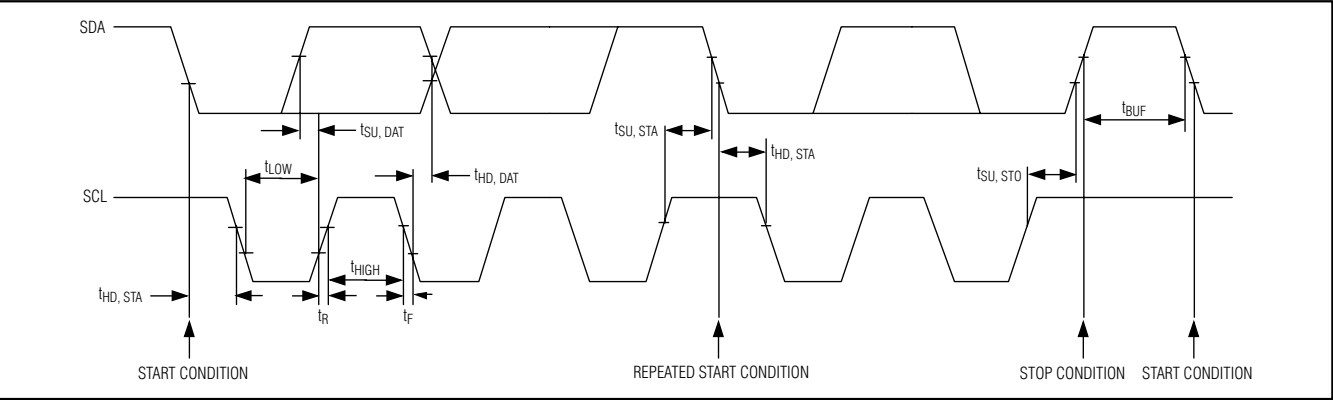


Figure 2. 2-Wire Serial Interface Timing Diagram

Detailed Description

The MAX7312 general-purpose input/output (GPIO) peripheral provides up to 16 I/O ports, controlled through an I²C-compatible serial interface. The MAX7312 consists of input port registers, output port registers, polarity inversion registers, configuration registers, and a bus-timeout register. Upon power-on, all I/O lines are set as inputs. Three slave ID address select pins, AD0, AD1, and AD2, choose one of 64 slave ID addresses, including the eight addresses supported by the Phillips PCA9555. Table 1 is the register address table. Tables 2–6 show detailed register information.

Serial Interface

Serial Addressing

The MAX7312 operates as a slave that sends and receives data through a 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to and from the MAX7312, and generates the SCL clock that synchronizes the data transfer (Figure 2).

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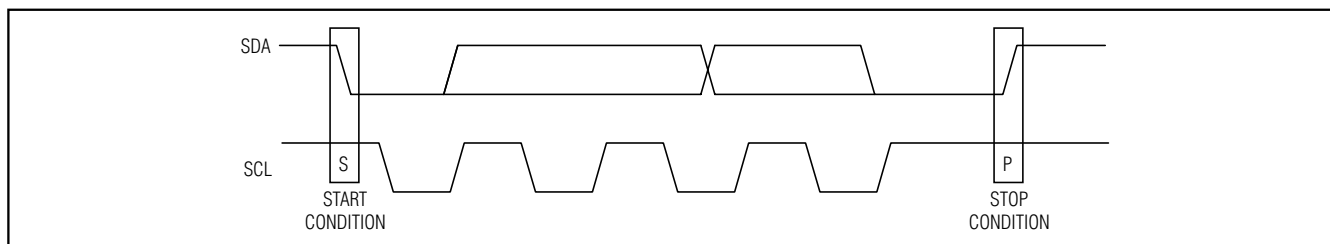


Figure 3. START and STOP Conditions

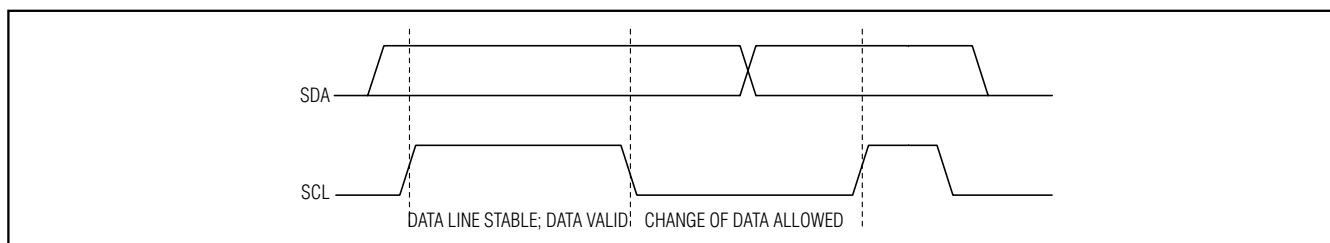


Figure 4. Bit Transfer

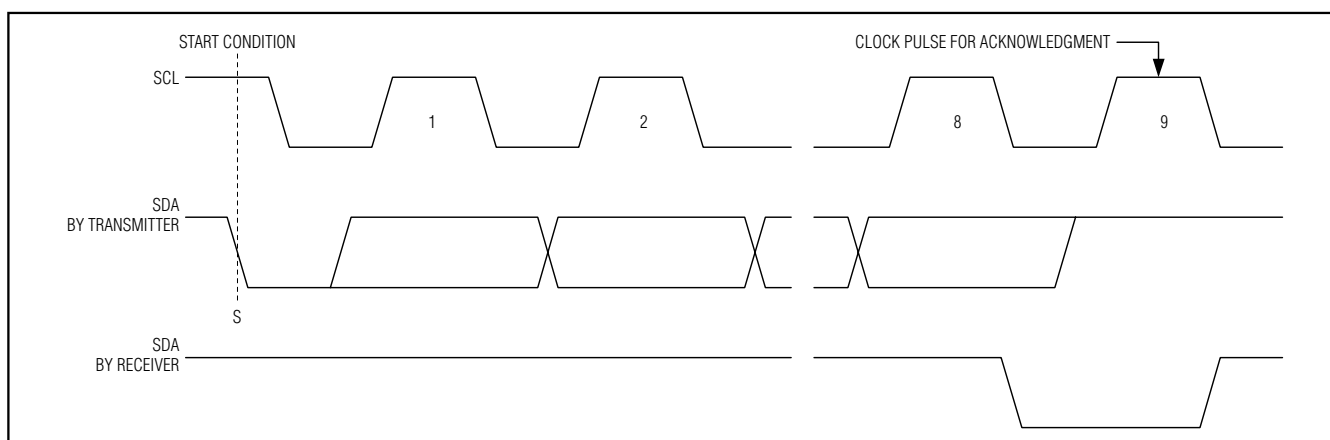


Figure 5. Acknowledge

Each transmission consists of a START condition sent by a master, followed by the MAX7312 7-bit slave address plus R/W bit, a register address byte, 1 or more data bytes, and finally a STOP condition (Figure 3).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit, which the recipient uses as a handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7312, the

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MAX7312 generates the acknowledge bit since the MAX7312 is the recipient. When the MAX7312 is transmitting to the master, the master generates the acknowledge bit.

Slave Address

The MAX7312 has a 7-bit-long slave address (Figure 6). The 8th bit following the 7-bit slave address is the $\overline{R}/\overline{W}$ bit. Set this bit low for a write command and high for a read command.

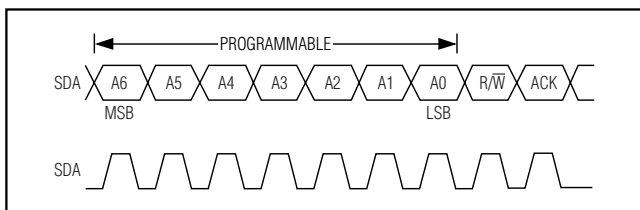


Figure 6. Slave Address

Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave ID addresses (Table 7).

Data Bus Transaction

The command byte is the first byte to follow the 8-bit device slave address during a write transmission (Table 1, Figure 7). The command byte is used to determine which of the following registers are written or read.

Writing to Port Registers

Transmit data to the MAX7312 by sending the device slave address and setting the LSB to a logic zero. The command byte is sent after the address and determines which registers receive the data following the command byte (Figure 7).

Table 1. Command Byte Register

COMMAND BYTE ADDRESS (HEX)	FUNCTION	PROTOCOL	POWER-UP DEFAULT
0x00	Input port 1	Read byte	XXXX XXXX
0x01	Input port 2	Read byte	XXXX XXXX
0x02	Output port 1	Read/write byte	1111 1111
0x03	Output port 2	Read/write byte	1111 1111
0x04	Port 1 polarity inversion	Read/write byte	0000 0000
0x05	Port 2 polarity inversion	Read/write byte	0000 0000
0x06	Port 1 configuration	Read/write byte	1111 1111
0x07	Port 2 configuration	Read/write byte	1111 1111
0x08	Timeout register	Read/write byte	0000 0001
0xFF	Factory reserved. (Do not write to this register.)	—	—

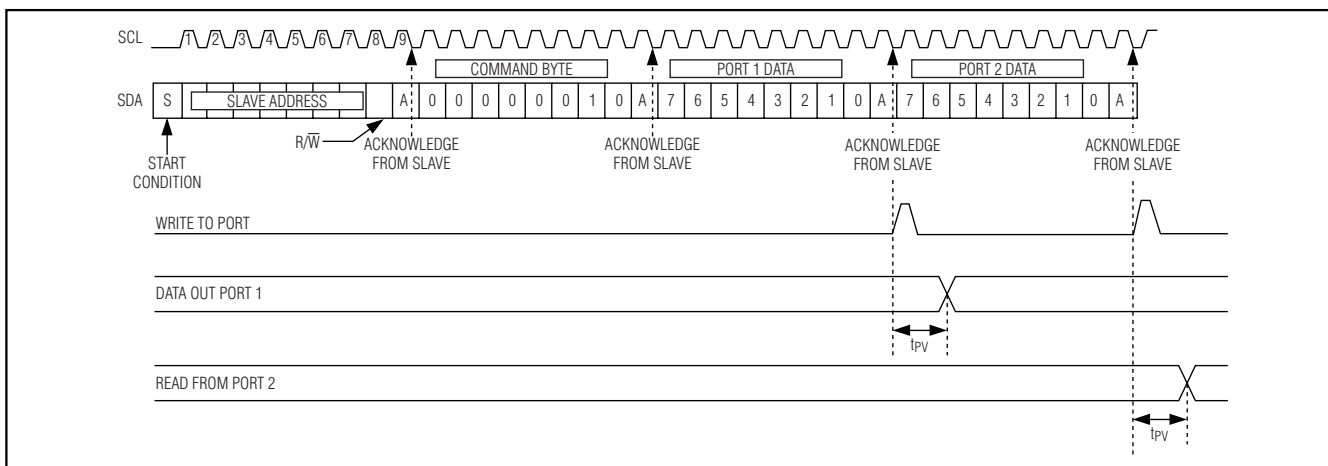


Figure 7. Writes to Output Registers Through Write Byte Protocol

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Eight of the MAX7312's nine registers are configured to operate as four register pairs: input ports, output ports, polarity inversion ports, and configuration ports. After sending 1 byte of data to one register, the next byte is sent to the other register in the pair. For example, if the first byte of data is sent to output port 2, then the next byte of data is stored in output port 1. An unlimited number of data bytes can be sent in one write transmission. This allows each 8-bit register to be updated independently of the other registers.

Reading Port Registers

To read the device data, the bus master must first send the MAX7312 address with the R/W bit set to zero, followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the MAX7312 address with the R/W bit set to 1. Data from the register defined by the command byte is then sent from the MAX7312 to the master (Figures 8, 9).

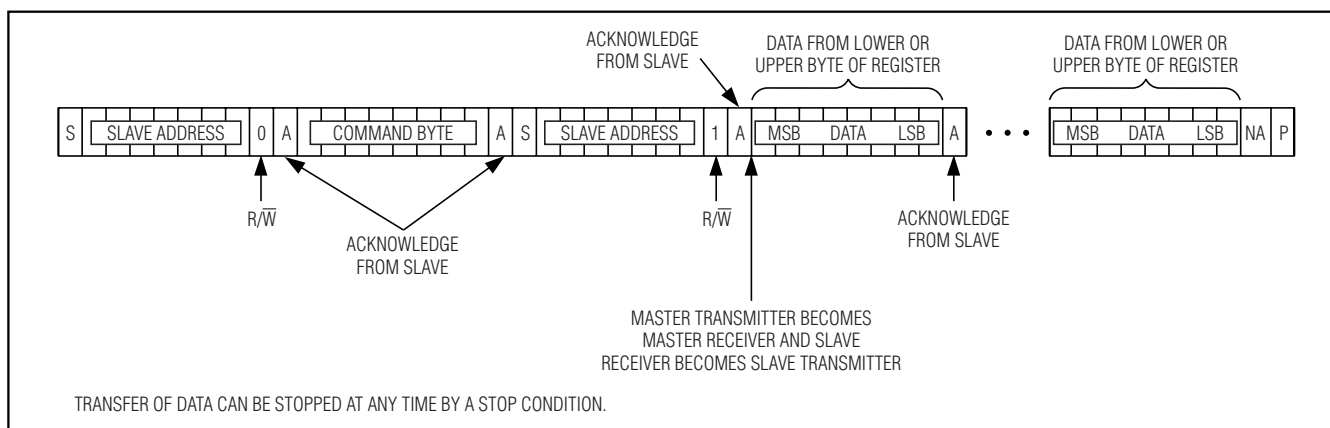


Figure 8. Read from Register

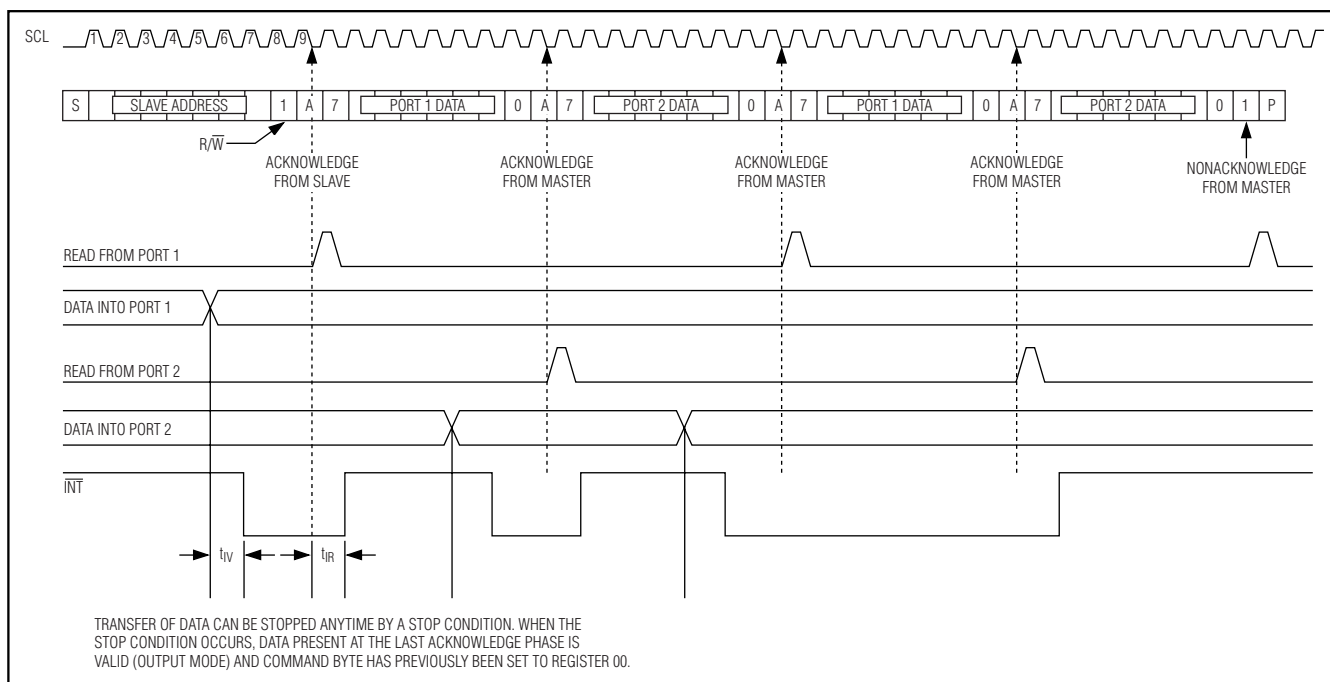


Figure 9. Read from Input Registers

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Data is clocked into a register on the falling edge of the acknowledge clock pulse. After reading the first byte, additional bytes may be read and reflect the content in the other register in the pair. For example, if input port 1 is read, the next byte read is input port 2. An unlimited number of data bytes can be read in one read transmission, but the final byte received must not be acknowledged by the bus master.

Interrupt ($\overline{\text{INT}}$)

The open-drain interrupt output, $\overline{\text{INT}}$, activates when one of the port pins changes states and only when the pin is configured as an input. The interrupt deactivates when the input returns to its previous state or the input register is read (Figure 9). A pin configured as an output does not cause an interrupt. Each 8-bit port register is read independently; therefore, an interrupt caused by port 1 is not cleared by a read of port 2's register.

Changing an I/O from an output to an input may cause a false interrupt to occur if the state of that I/O does not match the content of the input port register.

Input/Output Port

When an I/O is configured as an input, FETs Q1 and Q2 are off (Figure 10), creating a high-impedance input. All inputs are overvoltage protected to 5.5V, independent of supply voltage. When a port is configured as an output, either Q1 or Q2 is on, depending on the state of the output port register. When V^+ powers up, an internal power-on reset sets all registers to their respective defaults (Table 1).

Input Port Registers

The input port registers (Table 2) are read-only ports. They reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the respective configuration register. A read of the input port 1 register latches the current value of I/O0–I/O7. A read of the input port 2 register latches the current value of I/O8–I/O15. Writes to the input port registers are ignored.

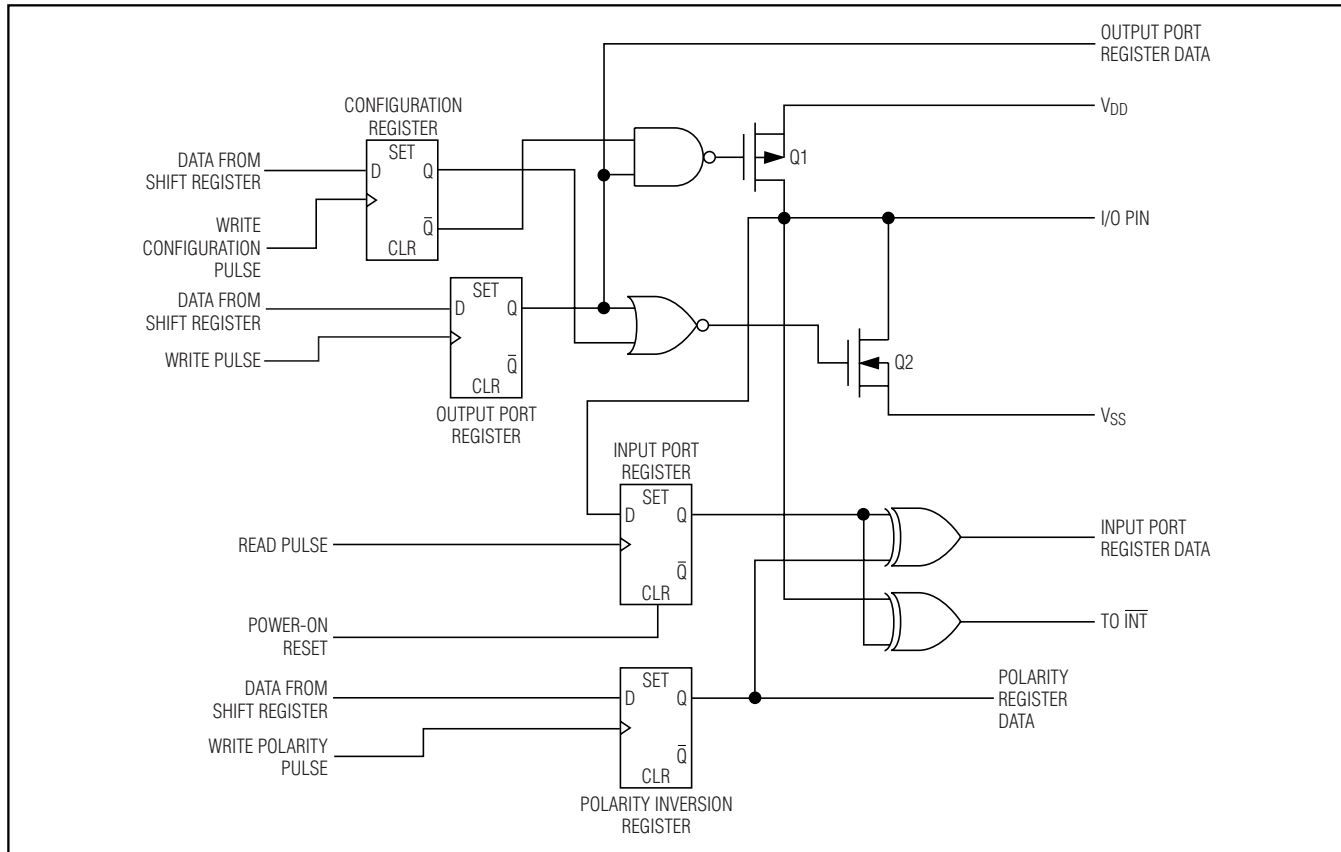


Figure 10. Simplified Schematic of I/Os

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Table 2. Registers 0x00, 0x01—Input Port Registers

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	I15	I14	I13	I12	I11	I10	I9	I8

Table 3. Registers 0x02, 0x03—Output Port Registers

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	O15	O14	O13	O12	O11	O10	O9	O8
Power-up default	1	1	1	1	1	1	1	1

Table 4. Registers 0x04, 0x05—Polarity Inversion Registers

BIT	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8
Power-up default	0	0	0	0	0	0	0	0

Table 5. Registers 0x06, 0x07—Configuration Registers

BIT	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8
Power-up default	1	1	1	1	1	1	1	1

Table 6. Register 0x08—Timeout Register

BIT	7	6	5	4	3	2	1	0
Power-up default	0	0	0	0	0	0	0	1

Output Port Registers

The output port registers (Table 3) set the outgoing logic levels of the I/Os defined as outputs by the respective configuration register. Reads from the output port registers reflect the value that is in the flip-flop controlling the output selection, not the actual I/O value.

Polarity Inversion Registers

The polarity inversion registers (Table 4) enable polarity inversion of pins defined as inputs by the respective port configuration registers. Set the bit in the polarity inversion register to invert the corresponding port pin's polarity. Clear the bit in the polarity inversion register to retain the corresponding port pin's original polarity.

Configuration Registers

The configuration registers (Table 5) configure the directions of the I/O pins. Set the bit in the respective configuration register to enable the corresponding port as an input. Clear the bit in the configuration register to enable the corresponding port as an output.

Bus Timeout

Set register 0x08 LSB (bit 0) to enable the bus timeout function (Table 6) or clear it to disable the bus timeout function. Enabling the timeout feature resets the MAX7312 serial bus interface when SCL stops either high or low during a read or write. If either SCL or SDA is low for more than 29ms after the start of a valid serial transfer, the interface resets itself and sets up SDA as an input. The MAX7312 then waits for another START condition.

Standby

The MAX7312 goes into standby when the I²C bus is idle. Standby supply current is typically 2.9μA.

Applications Information

Hot Insertion

The I/O ports I/O0–I/O15 interrupt output INT $\bar{1}$, and serial interfaces SDA, SCL, AD0-2 remain high impedance with up to 6V asserted on them when the MAX7312 is powered down ($V_+ = 0V$). The MAX7312 can therefore be used in hot-swap applications.

Power-Supply Consideration

The MAX7312 operates from a supply voltage of 2V to 5.5V. Bypass the power supply to GND with a 0.047μF capacitor as close to the device as possible. For the QFN version, connect the underside exposed pad to GND.

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Table 7. MAX7312 Address Map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	ADDRESS (HEX)
GND	SCL	GND	0	0	1	0	0	0	0	0x20
GND	SCL	V ⁺	0	0	1	0	0	0	1	0x22
GND	SDA	GND	0	0	1	0	0	1	0	0x24
GND	SDA	V ⁺	0	0	1	0	0	1	1	0x26
V ⁺	SCL	GND	0	0	1	0	1	0	0	0x28
V ⁺	SCL	V ⁺	0	0	1	0	1	0	1	0x2A
V ⁺	SDA	GND	0	0	1	0	1	1	0	0x2C
V ⁺	SDA	V ⁺	0	0	1	0	1	1	1	0x2E
GND	SCL	SCL	0	0	1	1	0	0	0	0x30
GND	SCL	SDA	0	0	1	1	0	0	1	0x32
GND	SDA	SCL	0	0	1	1	0	1	0	0x34
GND	SDA	SDA	0	0	1	1	0	1	1	0x36
V ⁺	SCL	SCL	0	0	1	1	1	0	0	0x38
V ⁺	SCL	SDA	0	0	1	1	1	0	1	0x3A
V ⁺	SDA	SCL	0	0	1	1	1	1	0	0x3C
V ⁺	SDA	SDA	0	0	1	1	1	1	1	0x3E
GND	GND	GND	0	1	0	0	0	0	0	0x40
GND	GND	V ⁺	0	1	0	0	0	0	1	0x42
GND	V ⁺	GND	0	1	0	0	0	1	0	0x44
GND	V ⁺	V ⁺	0	1	0	0	0	1	1	0x46
V ⁺	GND	GND	0	1	0	0	1	0	0	0x48
V ⁺	GND	V ⁺	0	1	0	0	1	0	1	0x4A
V ⁺	V ⁺	GND	0	1	0	0	1	1	0	0x4C
V ⁺	V ⁺	V ⁺	0	1	0	0	1	1	1	0x4E
GND	GND	SCL	0	1	0	1	0	0	0	0x50
GND	GND	SDA	0	1	0	1	0	0	1	0x52
GND	V ⁺	SCL	0	1	0	1	0	1	0	0x54
GND	V ⁺	SDA	0	1	0	1	0	1	1	0x56
V ⁺	GND	SCL	0	1	0	1	1	0	0	0x58
V ⁺	GND	SDA	0	1	0	1	1	0	1	0x5A
V ⁺	V ⁺	SCL	0	1	0	1	1	1	0	0x5C
V ⁺	V ⁺	SDA	0	1	0	1	1	1	1	0x5E

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MAX7312

Table 7. MAX7312 Address Map (continued)

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	ADDRESS (HEX)
SCL	SCL	GND	1	0	1	0	0	0	0	0xA0
SCL	SCL	V ⁺	1	0	1	0	0	0	1	0xA2
SCL	SDA	GND	1	0	1	0	0	1	0	0xA4
SCL	SDA	V ⁺	1	0	1	0	0	1	1	0xA6
SDA	SCL	GND	1	0	1	0	1	0	0	0xA8
SDA	SCL	V ⁺	1	0	1	0	1	0	1	0xAA
SDA	SDA	GND	1	0	1	0	1	1	0	0xAC
SDA	SDA	V ⁺	1	0	1	0	1	1	1	0xAE
SCL	SCL	SCL	1	0	1	1	0	0	0	0xB0
SCL	SCL	SDA	1	0	1	1	0	0	1	0xB2
SCL	SDA	SCL	1	0	1	1	0	1	0	0xB4
SCL	SDA	SDA	1	0	1	1	0	1	1	0xB6
SDA	SCL	SCL	1	0	1	1	1	0	0	0xB8
SDA	SCL	SDA	1	0	1	1	1	0	1	0xBA
SDA	SDA	SCL	1	0	1	1	1	1	0	0xBC
SDA	SDA	SDA	1	0	1	1	1	1	1	0xBE
SCL	GND	GND	1	1	0	0	0	0	0	0xC0
SCL	GND	V ⁺	1	1	0	0	0	0	1	0xC2
SCL	V ⁺	GND	1	1	0	0	0	1	0	0xC4
SCL	V ⁺	V ⁺	1	1	0	0	0	1	1	0xC6
SDA	GND	GND	1	1	0	0	1	0	0	0xC8
SDA	GND	V ⁺	1	1	0	0	1	0	1	0xCA
SDA	V ⁺	GND	1	1	0	0	1	1	0	0xCC
SDA	V ⁺	V ⁺	1	1	0	0	1	1	1	0xCE
SCL	GND	SCL	1	1	0	1	0	0	0	0xD0
SCL	GND	SDA	1	1	0	1	0	0	1	0xD2
SCL	V ⁺	SCL	1	1	0	1	0	1	0	0xD4
SCL	V ⁺	SDA	1	1	0	1	0	1	1	0xD6
SDA	GND	SCL	1	1	0	1	1	0	0	0xD8
SDA	GND	SDA	1	1	0	1	1	0	1	0xDA
SDA	V ⁺	SCL	1	1	0	1	1	1	0	0xDC
SDA	V ⁺	SDA	1	1	0	1	1	1	1	0xDE

Chip Information

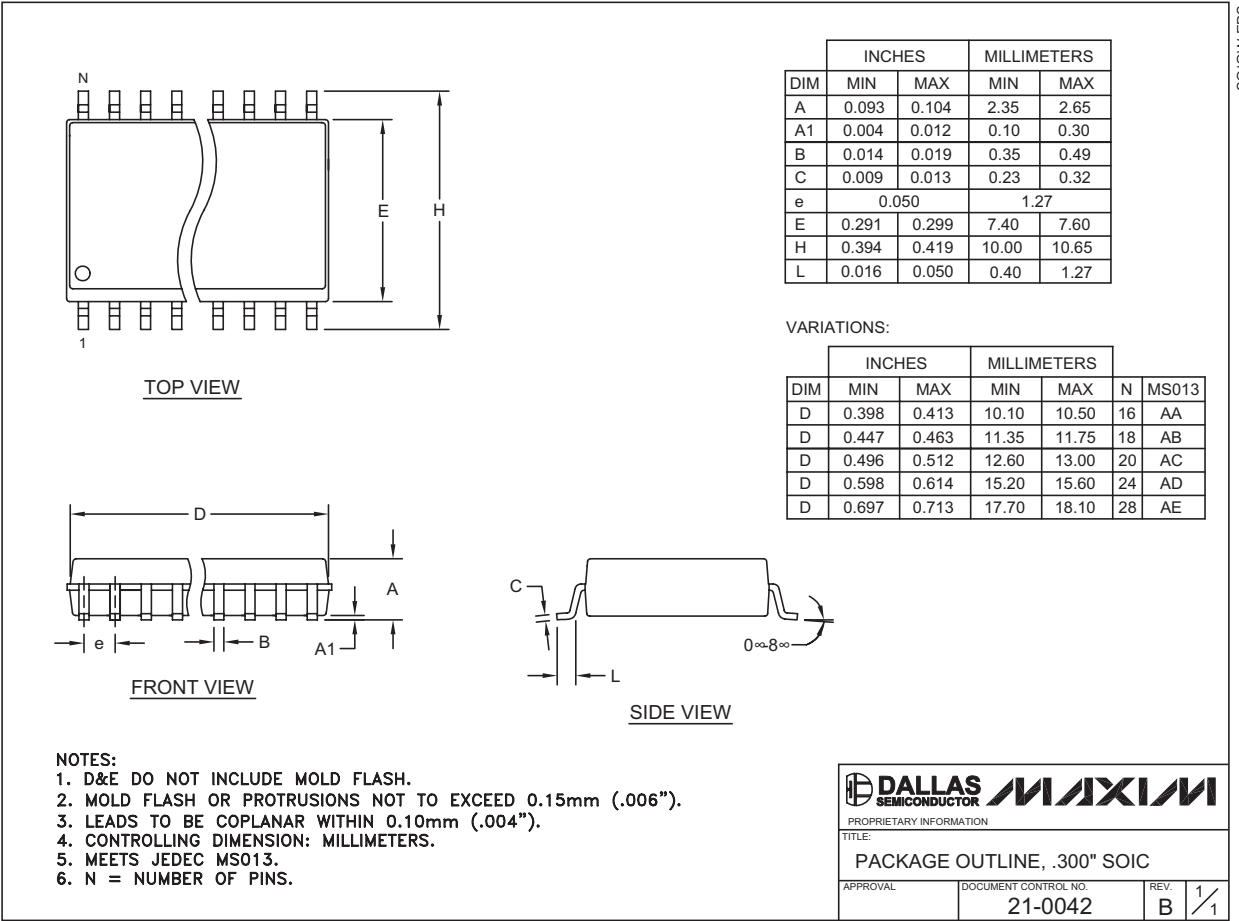
TRANSISTOR COUNT: 12,994

PROCESS: BiCMOS

2-Wire-Interfaced 16-Bit I/O Port Expander with Interrupt and Hot-Insertion Protection

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

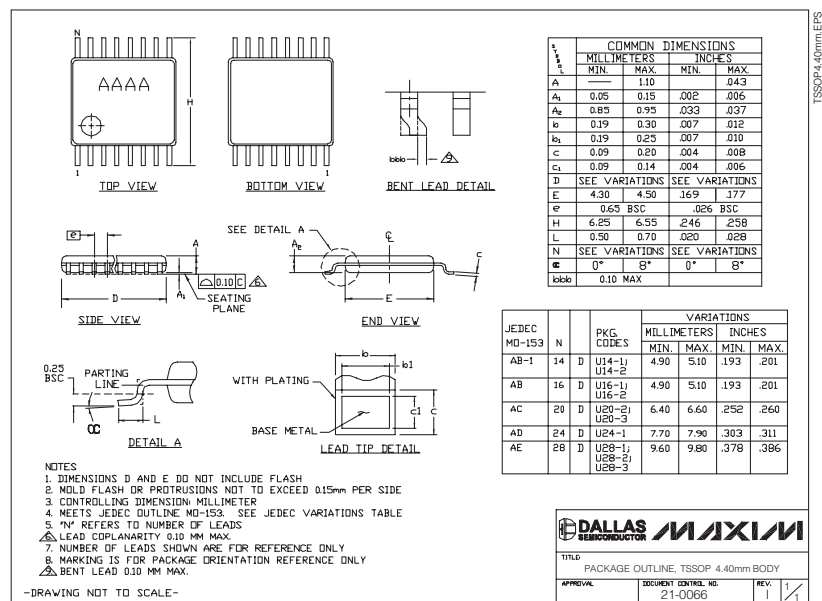
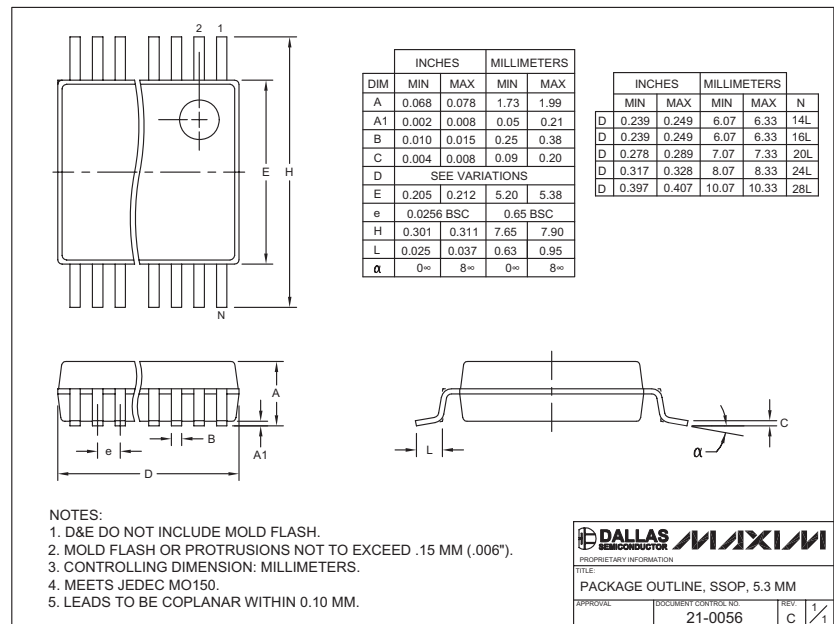


2-Wire-Interfaced 16-Bit I/O Port Expander with Interrupt and Hot-Insertion Protection

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

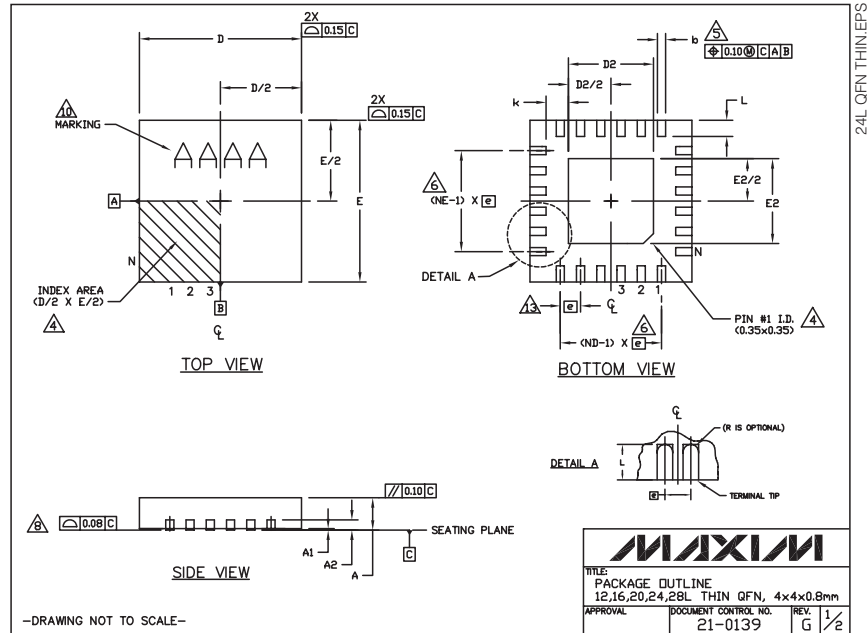
MAX7312



2-Wire-Interfaced 16-Bit I/O Port Expander with Interrupt and Hot-Insertion Protection

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20	REF.		0.20	REF.		0.20	REF.		0.20	REF.	
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.60	BSC.		0.65	BSC.		0.50	BSC.		0.50	BSC.	
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
WDEC	WGGB			WGGB			WGGB-1			WGGB-2		

EXPOSED PAD VARIATIONS								
PKG	D2			E2				
CODES	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.		
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25		
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25		
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25		
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25		
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25		
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25		
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25		
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63		
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63		
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70		

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC M0220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- COPLANARITY SHALL NOT EXCEED 0.08mm.
- VARRAGE SHALL NOT EXCEED 0.10mm.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PLEAD (+) PACKAGE CODES.

MAXIM

TITLE: PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.8mm

APPROVAL: 21-0139 REV: 1/2

—DRAWING NOT TO SCALE—

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