Ultra-Low-Voltage µP Reset Circuits and Voltage Detectors

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
V_{CC} .....-0.3V to +6V
$\overline{MR}$, RESET IN, $\overline{RESET}$ (open-drain).....-0.3V to +6V
Push-Pull $\overline{RESET}$ and RESET .....-0.3V to (V_{CC} + 0.3V)
Input Current (all pins).....20mA
Output Current (RESET, $\overline{RESET}$).....20mA

Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +0.55V to +1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	MAX6843/MAX6845	0.55		1.80	V
		MAX6841/MAX6842/MAX6844 (Note 2)	0.75		1.80	
Supply Current	I_{CC}	V_{CC} = 0.9V, no load, reset not asserted		5.7	20	µA
		V_{CC} = 1.5V, no load, reset not asserted		7.3	20	
		V_{CC} = 1.8V, no load, reset not asserted		8.1	20	
Reset Threshold (V_{CC} Falling)	V_{TH}	I	1.350	1.388	1.425	V
		H	1.275	1.313	1.350	
		G	1.080	1.110	1.140	
		F	1.020	1.050	1.080	
		E	0.810	0.833	0.855	
		D, T_A = 0°C to +85°C	0.765	0.788	0.810	
RESET IN Threshold	V_{RSTIN}	MAX6843/MAX6844/MAX6845 (Note 3)	181.2	187.4	191.5	mV
RESET IN Leakage Current	I_{RSTIN}		-25		+25	nA
Reset Threshold Hysteresis	V_{HYS}			0.75		$\%V_{TH}$
V_{CC} or RESET IN to Reset Delay		V_{CC} falling, step signal from (V_{TH} + 10%) to (V_{TH} - 10%) within 1µs		150		µs
Reset Active Timeout Period	t_{RP}	D0 (voltage detector)		0.15		ms
		D1	1	1.5	2	
		D2	20	30	40	
		D3	140	210	280	
		D4	1120	1680	2240	
$\overline{MR}$ Input Voltage (Note 3)	V_{IL}				0.3 × V_{CC}	V
	V_{IH}		0.7 × V_{CC}			
$\overline{MR}$ Minimum Input Pulse Width		$\overline{MR}$ driven from V_{CC} to 0 (Note 3)	1			µs
$\overline{MR}$ Glitch Rejection		$\overline{MR}$ driven from V_{CC} to 0 (Note 3)		150		ns
$\overline{MR}$ to Reset Delay		$\overline{MR}$ driven from V_{CC} to 0 (Note 3)		500		ns
$\overline{MR}$ Pullup Resistance to V_{CC}			10	20	26	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +0.55V to +1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

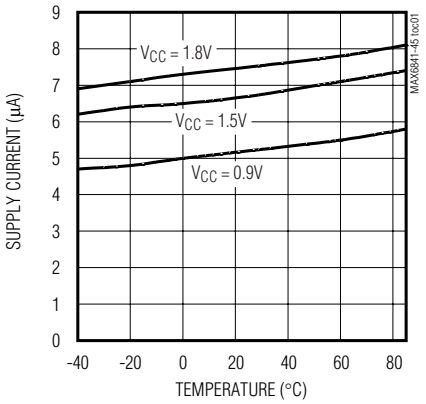
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Open-Drain $\overline{RESET}$ Output Voltage	V_{OL}	$V_{CC} \geq 0.55V$, I_{SINK} = 10µA, reset asserted			$0.2 \times V_{CC}$	V
		$V_{CC} \geq 0.83V$, I_{SINK} = 80µA, reset asserted			$0.2 \times V_{CC}$	
Open-Drain $\overline{RESET}$ Output Leakage Current	I_{LKG}	$V_{CC} > V_{TH}$, reset not asserted			1	µA
Push-Pull $\overline{RESET}$ Output Voltage	V_{OL}	$V_{CC} \geq 0.55V$, I_{SINK} = 10µA, reset asserted			$0.2 \times V_{CC}$	V
		$V_{CC} \geq 0.83V$, I_{SINK} = 80µA, reset asserted			$0.2 \times V_{CC}$	
	V_{OH}	$V_{CC} \geq 0.83V$, I_{SOURCE} = 40µA, reset not asserted	$0.8 \times V_{CC}$			
Push-Pull RESET Output Voltage	V_{OH}	$V_{CC} \geq 0.75V$, I_{SOURCE} = 10µA, reset asserted	$0.8 \times V_{CC}$			V
		$V_{CC} \geq 0.83V$, I_{SOURCE} = 40µA, reset asserted	$0.8 \times V_{CC}$			
	V_{OL}	$V_{CC} \geq 0.83V$, I_{SINK} = 80µA, reset not asserted			$0.2 \times V_{CC}$	

Note 1: 100% production tested at +25°C. Overtemperature limits are guaranteed by design.
Note 2: The active-low output $\overline{RESET}$ has $V_{CC(MIN)}$ = 0.55V (MAX6841/MAX6842).
Note 3: For V_{CC} > 0.788V, T_A = 0°C to +85°C, and for V_{CC} > 0.833V, T_A = -40°C to +85°C.

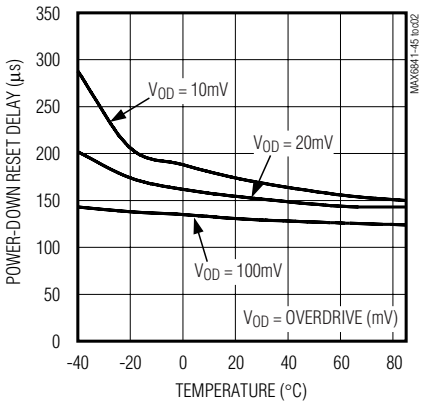
Typical Operating Characteristics

(V_{CC} = 1.5V, T_A = +25°C, unless otherwise noted.)

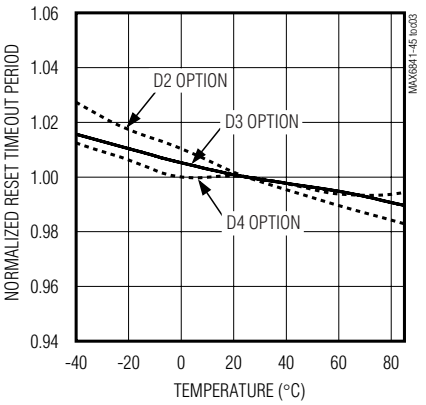
SUPPLY CURRENT vs. TEMPERATURE



POWER-DOWN RESET DELAY vs. TEMPERATURE



NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



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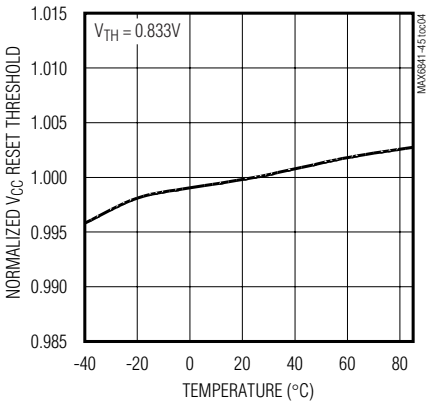
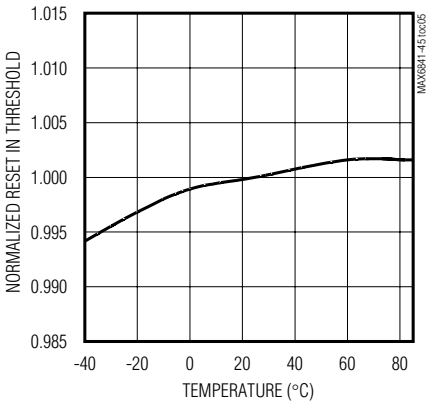
Typical Operating Characteristics (continued)

(V_{CC} = 1.5V, T_A = +25°C, unless otherwise noted.)

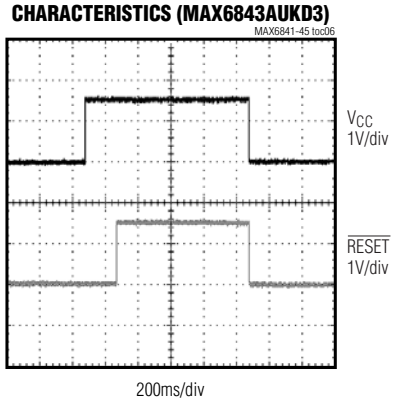
NORMALIZED V_{CC} RESET THRESHOLD vs. TEMPERATURE



NORMALIZED RESET IN THRESHOLD vs. TEMPERATURE



POWER-UP/POWER-DOWN CHARACTERISTICS (MAX6843AUKD3)



Pin Description

PIN			NAME	FUNCTION
MAX6841 MAX6842	MAX6843 MAX6845	MAX6844		
1	—	—	$\overline{\text{RESET}}$	Push-Pull (MAX6841) or Open-Drain (MAX6842) Active-Low Reset Output. $\overline{\text{RESET}}$ changes from high to low when V_{CC} drops below the selected reset threshold or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{\text{MR}}$ is released high.
—	1	—		Push-Pull (MAX6843) or Open-Drain (MAX6845) Active-Low Reset Output. $\overline{\text{RESET}}$ changes from high to low when RESET IN drops below the 187.4mV reset threshold (referenced to V_{CC}) or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after RESET IN exceeds the reset threshold and $\overline{\text{MR}}$ is released high.
2	2	2	GND	Ground
3	—	—	RESET	Push-Pull Active-High Reset Output. RESET changes from low to high when V_{CC} input drops below the selected reset threshold or $\overline{\text{MR}}$ is pulled low. RESET remains high for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{\text{MR}}$ is released high.
—	—	1		Push-Pull Active-High Reset Output. RESET changes from low to high when the RESET IN input drops below the 187.4mV reset threshold (referenced to V_{CC}). RESET remains high for the reset timeout period after RESET IN exceeds the reset threshold.
—	3	3	RESET IN	Adjustable Reset Input. High-impedance input for reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; the typical threshold is 187.4mV (referenced to V_{CC}). The MAX6843/MAX6844/ MAX6845 assert a reset signal when the V_{CC} to RESET IN differential falls below its threshold voltage.
4	4	4	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Internal 20kΩ pullup to V_{CC}. Pull low to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is low and for the reset timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V_{CC} if unused.
5	5	5	V_{CC}	Supply Voltage. Monitored supply for the MAX6841/MAX6842.

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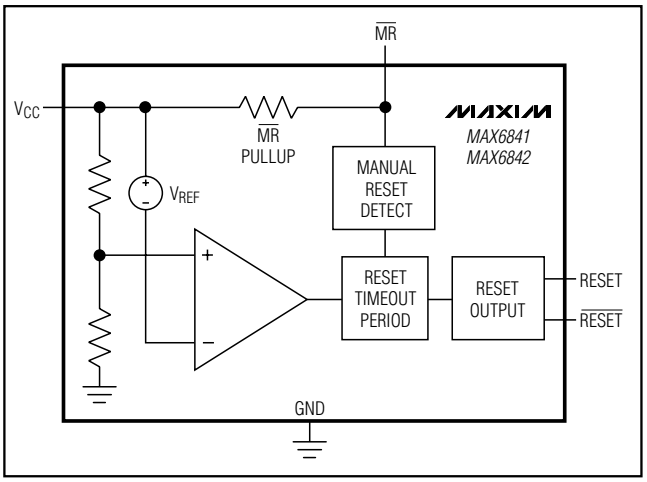
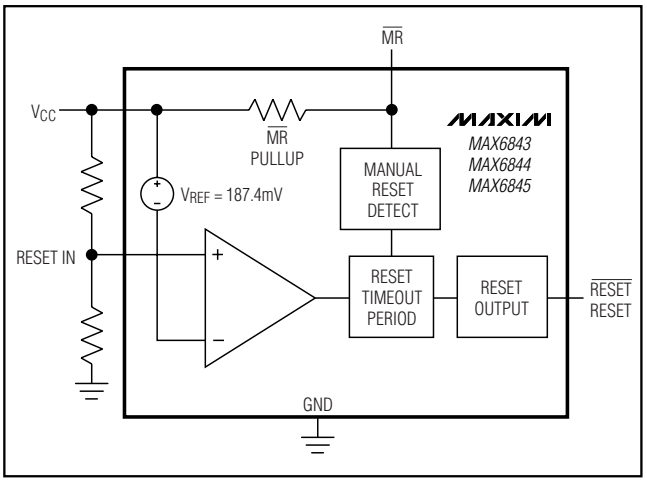
Functional Diagrams





Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. The MAX6841–MAX6845 assert a reset during power-up, power-down, and brownout conditions. When the V_{CC} supply voltage falls below a preset threshold (MAX6841/MAX6842) or RESET IN falls below the adjustable threshold (MAX6843/MAX6844/MAX6845), reset asserts and stays asserted for a fixed timeout delay (Table 2) after V_{CC} or RESET IN has risen above the reset threshold. The MAX6841–MAX6845 are available with five typical timeout options for each part: 150µs (voltage detector), 1.5ms, 30ms, 210ms, and 1.68s.

The MAX6841/MAX6842 have two reset outputs (RESET and $\overline{RESET}$); one is the inverse of the other. The MAX6841 has one active-high push-pull output and one active-low push-pull output. The MAX6842 has one active-high push-pull output and one active-low open-drain output. The MAX6843 features an active-low push-pull output. The MAX6844 features an active-high push-pull output, and the MAX6845 has an active-low open-drain output stage. Connect a pullup resistor from the open-drain $\overline{RESET}$ output to any voltage between 0 and 6V.

Manual Reset Input

Many µP-based systems require a manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. Reset remains asserted while $\overline{MR}$ is low, and for a fixed timeout delay after $\overline{MR}$ returns high. This input has an internal 20kΩ pullup resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with CMOS logic level or with open-drain/collector outputs. To create a manual reset function, connect a normally open momentary switch from $\overline{MR}$ to ground; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to ground to provide additional noise immunity.

RESET IN

The MAX6843/MAX6844/MAX6845 feature a RESET IN input, which allows users to adjust the reset threshold voltage. The internal reference voltage is 187.4mV with respect to V_{CC}. An external resistive-divider network can be used to set voltage monitoring thresholds, as shown in Figure 1. The resistive-divider network must be referenced to V_{CC}. As V_{CC} falls, the voltage at

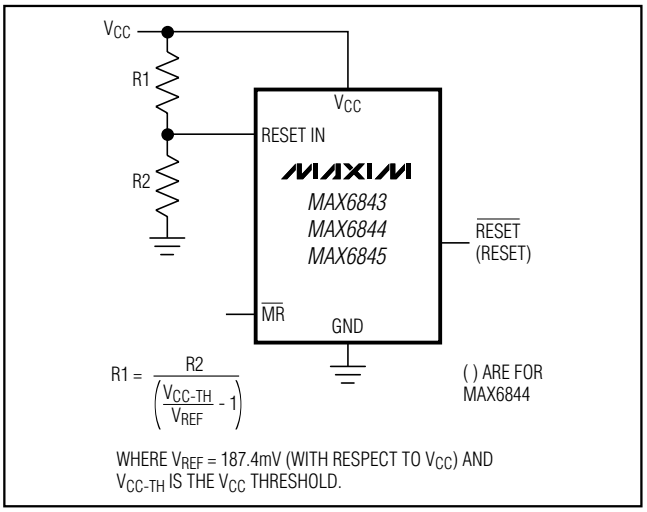


Figure 1. Setting the Adjustable Threshold Externally

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RESET IN decreases. The MAX6843/MAX6844/MAX6845 assert a reset when the voltage at RESET IN falls below the RESET IN threshold (V_{RSTIN}). The low-leakage current at RESET IN allows for relatively large-value resistors to be used, which reduces power consumption. For example, for V_{CC-TH} = 0.9V, if R2 = 100kΩ, then R1 = 26.3kΩ.

Applications Information

VCC Falling Transients

The MAX6841–MAX6845 are relatively immune to short-duration falling V_{CC} transients (glitches). Figure 2 shows typical transient duration vs. reset comparator overdrive, for which the MAX6841–MAX6845 do not generate a reset pulse. The graph was generated using a falling pulse applied to V_{CC}, starting 0.1V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width that a falling V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes further below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to VCC = 0

When V_{CC} falls below 0.55V, the MAX6841/MAX6843 push-pull $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, because most µP and other circuitry are inoperative with V_{CC} lower than 0.55V. However, in applications in which $\overline{RESET}$ must be valid down to 0, adding a pulldown resistor to $\overline{RESET}$ causes any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 3). R3's value is not critical; 200kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

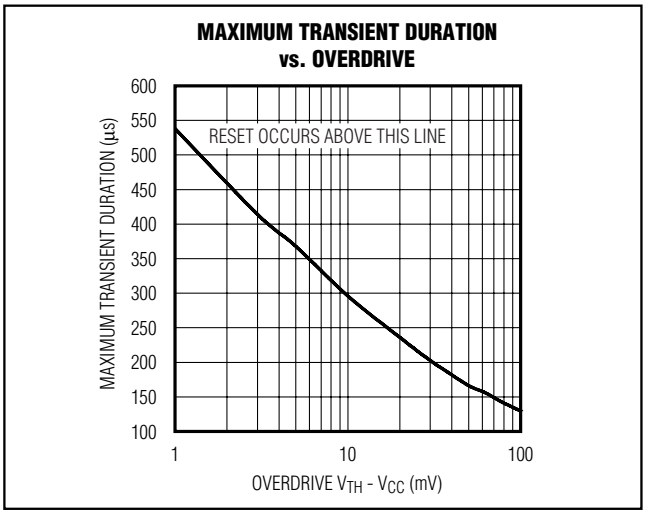

Figure 2. Maximum Transient Duration vs. Overdrive

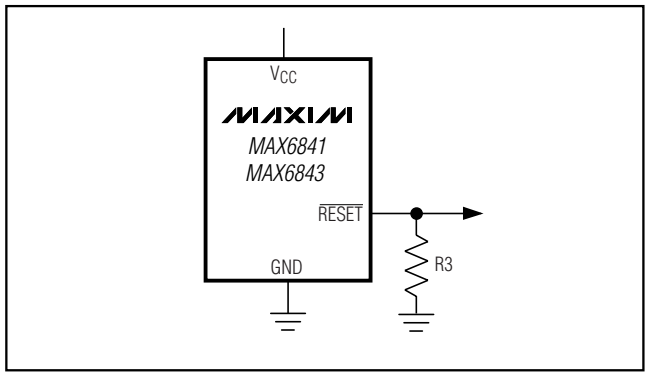

Figure 3. $\overline{RESET}$ Valid to V_{CC} = 0

A 200kΩ pullup resistor to V_{CC} is also recommended for the MAX6841/MAX6842/MAX6844 if push-pull RESET is required to remain valid for $V_{CC} \leq 0.75V$.

Interfacing to µPs with Bidirectional Reset Pins

Because the $\overline{RESET}$ output on the MAX6842/MAX6845 is open drain, these devices interface easily with µPs that have bidirectional reset pins. Connecting the µP supervisor's $\overline{RESET}$ output directly to the µP's $\overline{RESET}$ pin with a single pullup resistor allows either device to assert reset (Figure 4).

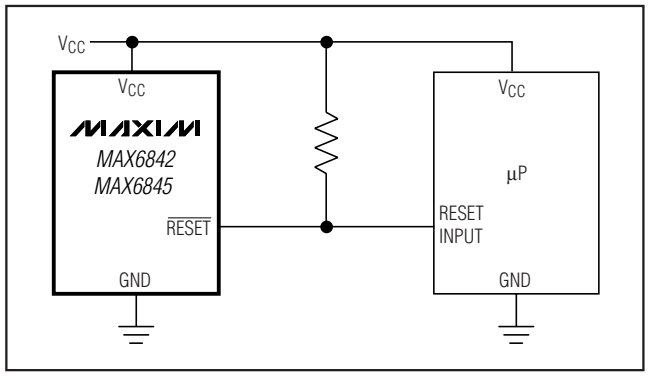

Figure 4. Interfacing to Microprocessors with Bidirectional Reset I/0

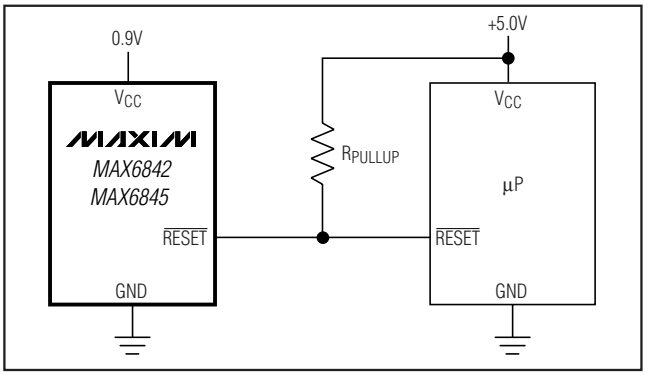

Figure 5. Using the MAX6842/MAX6845 Open-Drain RESET Output with Multiple Supplies

Using the MAX6842/MAX6845 Open-Drain RESET Output with Multiple Supplies

Generally, the pullup connected to the MAX6842/MAX6845 connects to the supply voltage being monitored at the IC's V_{CC} pin. However, some systems use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 5). Note that as the MAX6842/MAX6845's V_{CC} decreases, so does the IC's ability to sink current at RESET. Also, with any pullup, RESET is pulled high as V_{CC} decays toward 0. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

Chip Information

TRANSISTOR COUNT: 788

PROCESS: BiCMOS

Table 1. Threshold Suffix Guide

SUFFIX	RESET THRESHOLD (V)
I	1.388
H	1.313
G	1.110
F	1.050
E	0.833
D	0.788

Table 2. Active Timeout Period Guide

SUFFIX	RESET ACTIVE TIMEOUT PERIOD (ms)		
	MIN	TYP	MAX
D0	—	0.15	—
D1	1	1.5	2
D2	20	30	40
D3	140	210	280
D4	1120	1680	2240

Table 3. Standard Versions

DEVICE	TOP MARK
MAX6841HUKD0	AEDR
MAX6841HUKD3	AEDS
MAX6841FUKD0	AEDP
MAX6841FUKD3	AEDQ
MAX6841DUKD0	AEDN
MAX6841DUKD3	AEDO
MAX6842HUKD0	AEDX
MAX6842HUKD3	AEDY
MAX6842FUKD0	AEDV
MAX6842FUKD3	AEDW
MAX6842DUKD0	AEDT
MAX6842DUKD3	AEDU
MAX6843UKD0	AEDZ
MAX6843UKD3	AEAV
MAX6844UKD0	AEEB
MAX6844UKD3	AEEC
MAX6845UKD0	AEAX
MAX6845UKD3	AEAY

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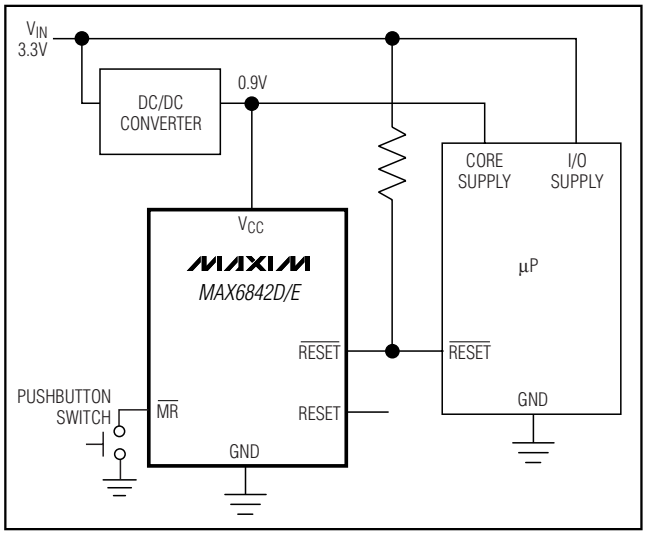
Selector Guide

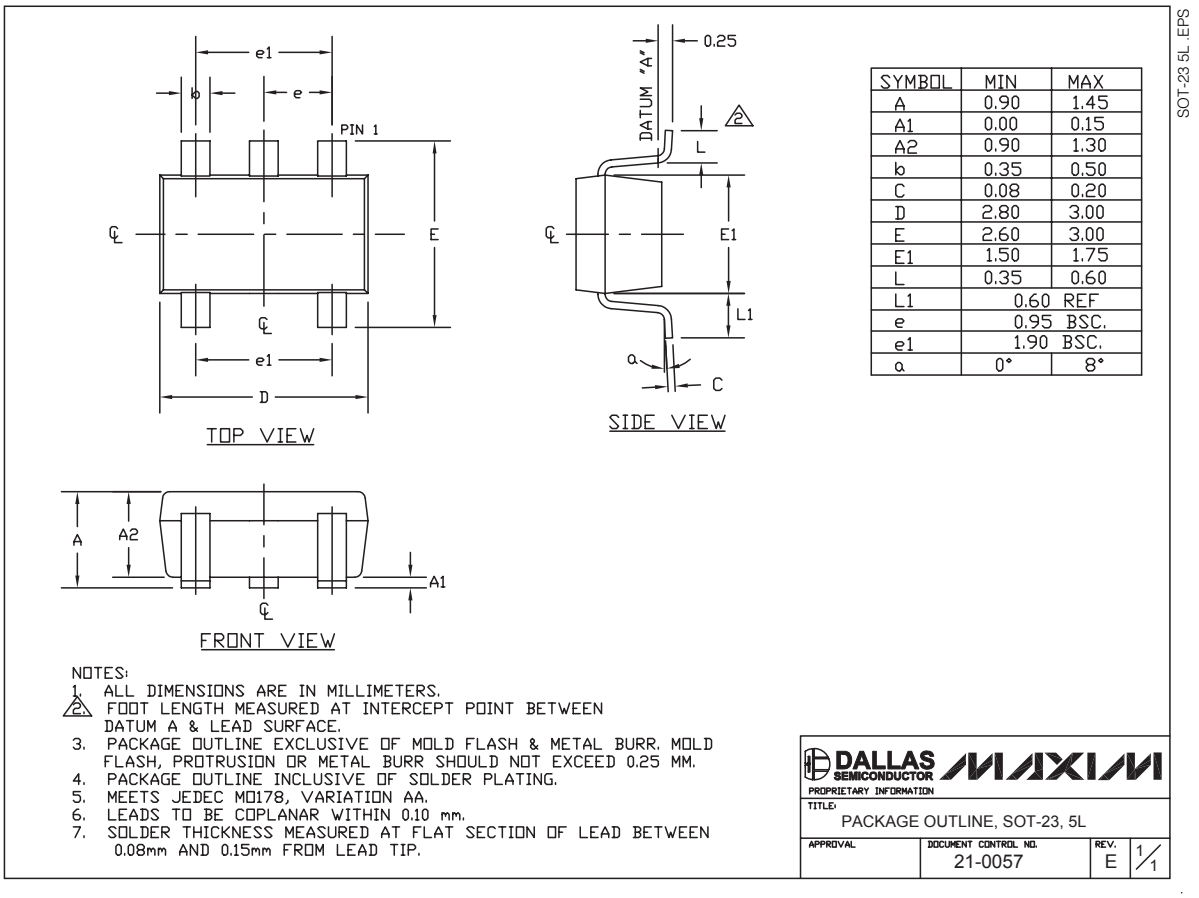
PART	MANUAL RESET	ADJUSTABLE RESET INPUT	PUSH-PULL $\overline{\text{RESET}}$	PUSH-PULL RESET	OPEN-DRAIN $\overline{\text{RESET}}$
MAX6841	✔	—	✔	✔	—
MAX6842	✔	—	—	✔	✔
MAX6843	✔	✔	✔	—	—
MAX6844	✔	✔	—	✔	—
MAX6845	✔	✔	—	—	✔

Typical Operating Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF	
e	0.95 BSC.	
e1	1.90 BSC.	
α	0°	8°