Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

$V_{CC}1$, $V_{CC}2$, POK1 to GND .....-0.3V to +6V
Open-Drain $\overline{RESET}$, $\overline{PFO}$ to GND.....-0.3V to +6V
Push-Pull $\overline{RESET}$ to GND.....-0.3V to ($V_{CC}1$ + 0.3V)
$\overline{MR}$, RSTIN, PFI to GND.....-0.3V to ($V_{CC}1$ + 0.3V)
Input/Output Current, All Pins 20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C).....247mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	$V_{CC}1$, $V_{CC}2$	T_A = -40°C to 0°C		1.2		5.5	V
		T_A = 0°C to +85°C		1.0		5.5	
$V_{CC}1$ Supply Current	$I_{CC}1$	$V_{CC}1$ = 3.3V, $V_{CC}1$ > $V_{CC}2$, no load, reset not asserted			5	10	µA
		$V_{CC}1$ = 1.8V, $V_{CC}1$ < $V_{CC}2$, no load, reset not asserted			5	10	
$V_{CC}2$ Supply Current	$I_{CC}2$	$V_{CC}2$ = 1.8V, $V_{CC}2$ < $V_{CC}1$, no load, reset not asserted			1	2	µA
		$V_{CC}2$ = 3.3V, $V_{CC}2$ > $V_{CC}1$, no load, reset not asserted			10	20	
Reset Threshold for $V_{CC}1$	$V_{TH}1$	MAX67_ _L	T_A = 0°C to +85°C	4.500	4.625	4.750	V
			T_A = -40°C to +85°C	4.425		4.825	
		MAX67_ _M	T_A = 0°C to +85°C	4.250	4.375	4.500	
			T_A = -40°C to +85°C	4.175		4.575	
		MAX67_ _T	T_A = 0°C to +85°C	3.000	3.075	3.150	
			T_A = -40°C to +85°C	2.950		3.200	
		MAX67_ _S	T_A = 0°C to +85°C	2.850	2.925	3.000	
			T_A = -40°C to +85°C	2.800		3.050	
		MAX67_ _R	T_A = 0°C to +85°C	2.550	2.625	2.700	
			T_A = -40°C to +85°C	2.505		2.745	
		MAX67_ _Z	T_A = 0°C to +85°C	2.250	2.313	2.375	
			T_A = -40°C to +85°C	2.213		2.413	
		MAX67_ _Y	T_A = 0°C to +85°C	2.125	2.188	2.250	
			T_A = -40°C to +85°C	2.088		2.288	
		MAX67_ _W	T_A = 0°C to +85°C	1.620	1.665	1.710	
			T_A = -40°C to +85°C	1.593		1.737	
		MAX67_ _V	T_A = 0°C to +85°C	1.530	1.575	1.620	
			T_A = -40°C to +85°C	1.503		1.647	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Threshold for $V_{CC}2$	$V_{TH}2$	MAX67_ _T	T_A = 0°C to +85°C	3.000	3.075	3.150	V
			T_A = -40°C to +85°C	2.905		3.050	
		MAX67_ _S	T_A = 0°C to +85°C	2.850	2.925	3.000	
			T_A = -40°C to +85°C	2.800		3.050	
		MAX67_ _R	T_A = 0°C to +85°C	2.550	2.625	2.700	
			T_A = -40°C to +85°C	2.505		2.745	
		MAX67_ _Z	T_A = 0°C to +85°C	2.250	2.313	2.375	
			T_A = -40°C to +85°C	2.213		2.413	
		MAX67_ _Y	T_A = 0°C to +85°C	2.125	2.188	2.250	
			T_A = -40°C to +85°C	2.088		2.288	
		MAX67_ _W	T_A = 0°C to +85°C	1.620	1.665	1.710	
			T_A = -40°C to +85°C	1.593		1.737	
		MAX67_ _V	T_A = 0°C to +85°C	1.530	1.575	1.620	
			T_A = -40°C to +85°C	1.503		1.647	
		MAX67_ _I	T_A = 0°C to +85°C	1.350	1.388	1.425	
			T_A = -40°C to +85°C	1.328		1.448	
		MAX67_ _H	T_A = 0°C to +85°C	1.275	1.313	1.350	
			T_A = -40°C to +85°C	1.253		1.373	
		MAX67_ _G	T_A = 0°C to +85°C	1.080	1.110	1.140	
			T_A = -40°C to +85°C	1.062		1.158	
		MAX67_ _F	T_A = 0°C to +85°C	1.020	1.050	1.080	
			T_A = -40°C to +85°C	1.002		1.098	
		MAX67_ _E	T_A = 0°C to +85°C	0.810	0.833	0.855	
			T_A = -40°C to +85°C	0.797		0.869	
		MAX67_ _D	T_A = 0°C to + 85°C	0.765	0.788	0.810	
			T_A = -40°C to +85°C	0.752		0.824	
RSTIN Threshold (MAX6738/ MAX6739/MAX6740/MAX6743)	$V_{TH-RSTIN}$	T_A = 0°C to +85°C		0.476	0.488	0.500	V
		T_A = -40°C to +85°C		0.468		0.507	
RSTIN Input Current		V_{RSTIN} ≥ 0.1V (Note 2)		-10		+10	nA
Reset Threshold Hysteresis		$V_{TH}1$, $V_{TH}2$, RSTIN, PFI			0.5		%
$\overline{RESET}$, POK1 Output Low	V_{OL}	$V_{CC}1$ ≥ 1.0V, I_{SINK} = 50µA, T_A = 0°C to +85°C				0.3	V
		$V_{CC}1$ ≥ 1.2V, I_{SINK} = 100µA				0.3	
		$V_{CC}1$ ≥ 2.13V, I_{SINK} = 1.2mA				0.3	
		$V_{CC}1$ ≥ 4.25V, I_{SINK} = 3.2mA,				0.4	
$\overline{RESET}$ Output High (Push-Pull)	V_{OH}	$V_{CC}1$ ≥ 2.38V, I_{SOURCE} = 500µA, output deasserted		0.8 × V_{CC}			V
		$V_{CC}1$ ≥ 4.75V, I_{SOURCE} = 800µA, output deasserted		0.8 × V_{CC}			

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ Output Open-Drain Leakage Current (MAX6736/MAX6738)	I_{LKG}	Output not asserted low (Note 2)			500	nA
POK1 Output Open-Drain Leakage		Output not asserted low (Note 2)			500	nA
V_{CC} Reset Delay	t_{RD}	$V_{CC}1$, $V_{CC}2$, or RSTIN falling at 10mV/µs from V_{TH} + 100mV to V_{TH} - 100mV		35		µs
V_{CC} Reset Timeout Period (Note 3)	t_{RP}	MAX67_ _ _ _ XK_ _D3	150	225	300	ms
		MAX67_ _ _ _ XK_ _ D7	1200	1800	2400	
MANUAL RESET (MAX6736–MAX6739 only)						
$\overline{MR}$ to $V_{CC}1$ Internal Pullup Impedance			0.75	1.5	3.00	kΩ
$\overline{MR}$ Timeout Period	t_{MRP}	Both D3 and D7 timing options	150	225	300	ms
$\overline{MR}$ Minimum Input Pulse Width	t_{MPW}		1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ Input Voltage	V_{IL}				0.3 × $V_{CC}1$	V
	V_{IH}		0.8 × $V_{CC}1$			
$\overline{MR}$ to $\overline{RESET}$ Delay				300		ns
$V_{CC}1$ POWER-OK OUTPUT (MAX6741/MAX6744 only)						
POK1 Timeout Period	t_{POKP}		37.5	56.25	75.0	ms
PUSHBUTTON RESET (MAX6740/MAX6741/MAX6742 only)						
$\overline{RESET}$ to $V_{CC}1$ Internal Pullup Impedance			25	50	100	kΩ
Manual Reset Detect Debounce Period	t_{DEB}	(Note 4)	37.5	56.25	75.0	ms
Manual Reset Timeout Period (Note 3)	t_{MRP}	MAX67_ _ _ _ XK_ _D3	150	225	300	ms
		MAX67_ _ _ _ XK_ _ D7	1200	1800	2400	
Manual Reset Minimum Input Pulse Width	t_{MPW}	(Note 4)	1			µs
Manual Reset Release Detect Threshold		(Note 4)		0.5 × $V_{CC}1$		V
Manual Reset Glitch Rejection		(Note 4)		100		ns
Manual Reset to $\overline{RESET}$ Delay				300		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

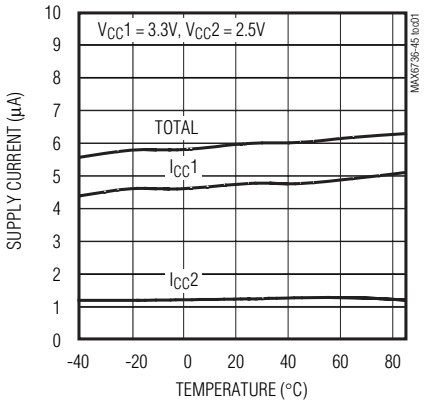
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-FAIL COMPARATOR (MAX6742/MAX6745 only)						
Power Fail In Threshold (Note 5)	V_{TH-PFI}	T_A = 0°C to +85°C	0.476	0.488	0.500	V
		T_A = -40°C to +85°C	0.468		0.507	
Power Fail In Current	I_{PFI}	V_{PFI} ≥ 0.1V (Note 2)	-10		+10	nA
$\overline{PFO}$ Output Low	V_{OL}	$V_{CC}1$ ≥ 1.53V, I_{SINK} = 500µA			0.3	V
		$V_{CC}1$ ≥ 2.03V, I_{SINK} = 1.2mA			0.3	
		$V_{CC}1$ ≥ 4.25V, I_{SINK} = 3.2mA			0.4	
PFI to $\overline{PFO}$ Propagation Delay	t_P	PFI falling at 10mV/µs from V_{TH-PFI} + 100mV to V_{TH-PFI} - 100mV or rising at 10mV/µs from V_{TH-PFI} - 100mV to V_{TH-PFI} + 100mV (Note 5)		35		µs
$\overline{PFO}$ Startup Delay		To output valid (Note 5)		5		ms

Note 1: All devices are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: t_{RD} timeout period begins after POK1 timeout period (t_{POKP}) and $V_{CC}2 \geq V_{TH}2$ (max) (MAX6741/MAX6744).
Note 4: Refers to the manual reset function obtained by forcing the RESET output low.
Note 5: $V_{CC}1 \geq 1.6V$.

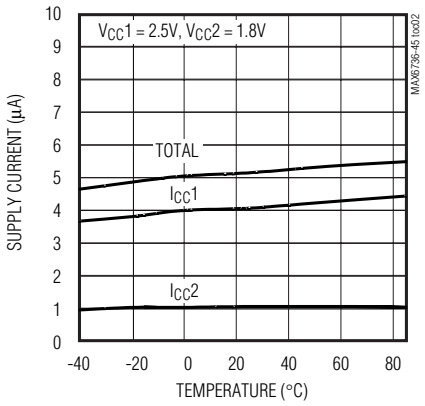
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

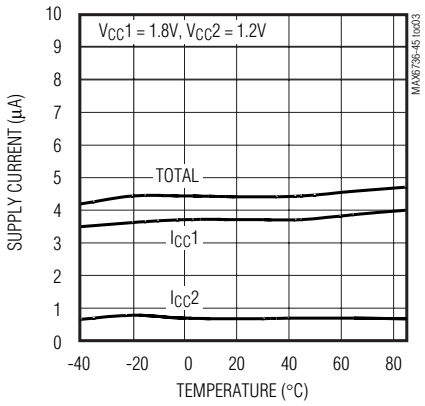
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE

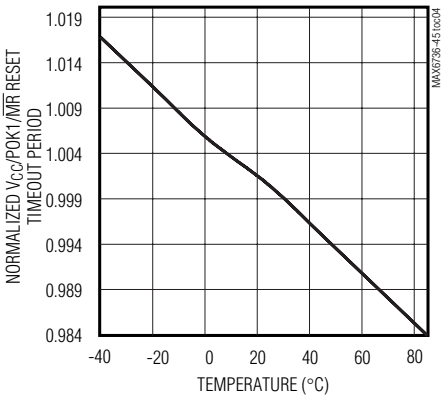


Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

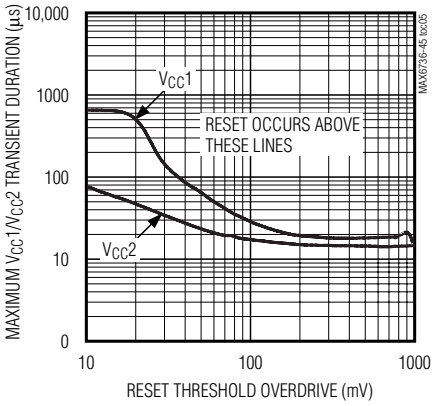
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

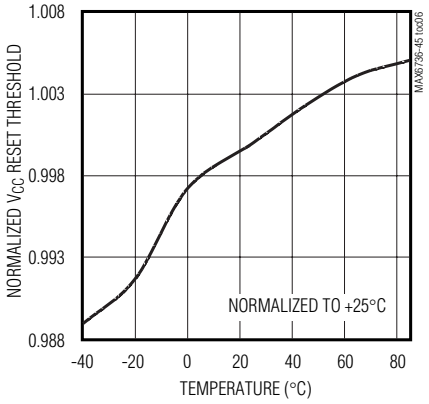
NORMALIZED V_{CC}/POK1/$\overline{MR}$ TIMEOUT PERIOD vs. TEMPERATURE



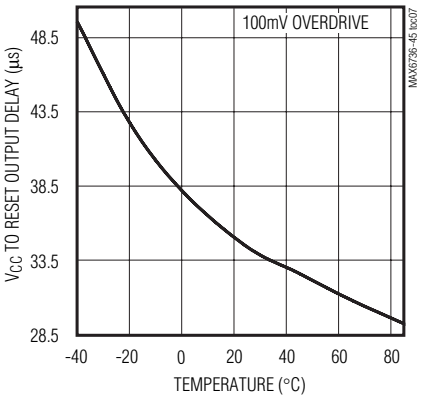
MAXIMUM $V_{CC}1$/$V_{CC}2$ TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



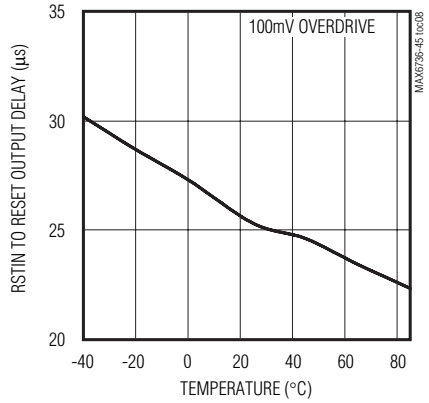
NORMALIZED V_{CC} RESET THRESHOLD vs. TEMPERATURE



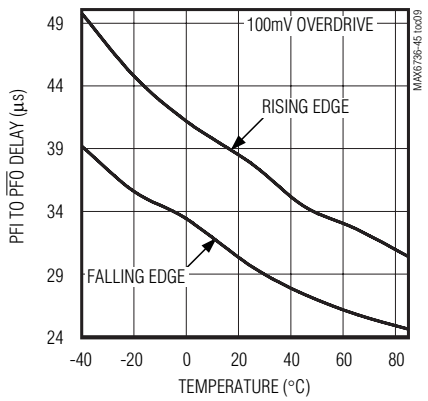
V_{CC} TO RESET OUTPUT DELAY vs. TEMPERATURE



RESET INPUT TO RESET OUTPUT DELAY vs. TEMPERATURE



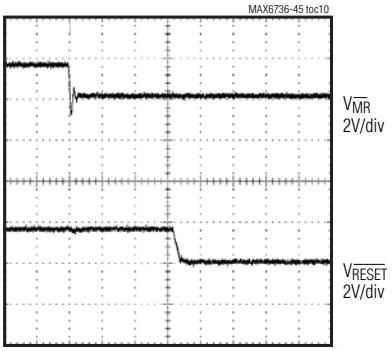
POWER-FAIL INPUT TO POWER-FAIL OUTPUT DELAY vs. TEMPERATURE



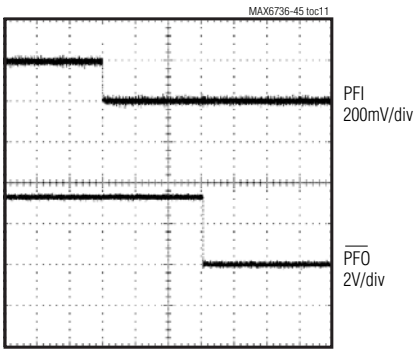
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

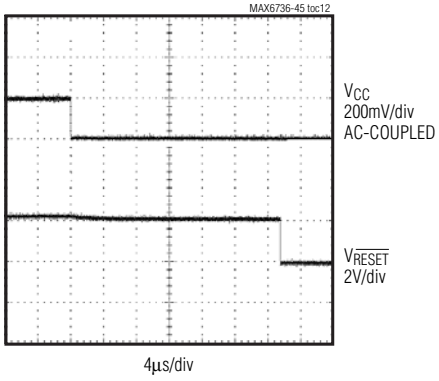
$\overline{MR}$ TO RESET OUTPUT DELAY



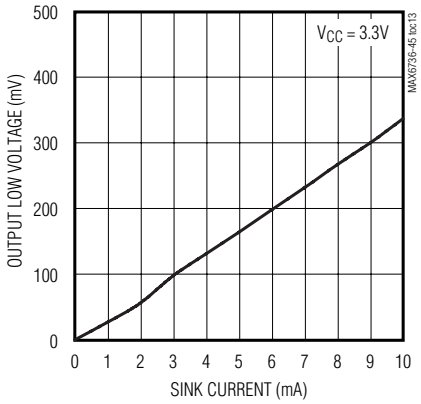
POWER-FAIL INPUT TO POWER-FAIL OUTPUT DELAY



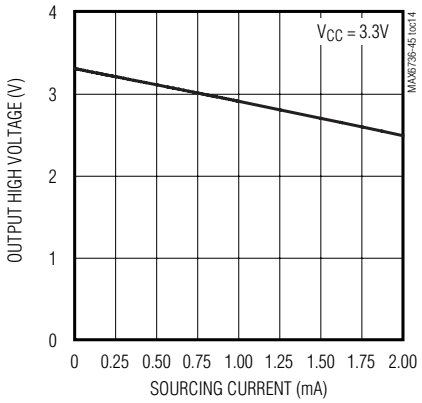
V_{CC} TO RESET OUTPUT DELAY



OUTPUT LOW VOLTAGE vs. SINK CURRENT



OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

Pin Description

PIN					NAME	FUNCTION
MAX6736 MAX6737	MAX6738 MAX6739	MAX6740 MAX6743	MAX6741 MAX6744	MAX6742 MAX6745		
1	1	1	1	1	$\overline{RESET}$	Reset Output, Push-Pull or Open Drain Active Low. $\overline{RESET}$ changes from high to low when any monitored power-supply input ($V_{CC}1$, $V_{CC}2$, RSTIN) drops below its selected reset threshold. It remains low until all monitored power-supply inputs exceed their selected reset thresholds for the V_{CC} reset timeout period. $\overline{RESET}$ is forced low if $\overline{MR}$ is low for at least the $\overline{MR}$ minimum input pulse width. It remains low for the $\overline{MR}$ reset timeout period after $\overline{MR}$ goes high. The push-pull output is referenced to $V_{CC}1$. The MAX6736/MAX6738 open-drain outputs require an external pullup resistor. The MAX6740/MAX6741/MAX6742 open-drain outputs have an internal 50kΩ pullup resistor to $V_{CC}1$ and provide a manual reset function.
2	2	2	2	2	GND	Ground
3	3	—	—	—	$\overline{MR}$	Manual Reset, Active Low. Pull low for at least $\overline{MR}$ minimum input pulse width to force $\overline{RESET}$ low. Reset remains active as long as $\overline{MR}$ is low and for the $\overline{MR}$ reset timeout period after $\overline{MR}$ goes high. There is an internal 1.5kΩ pullup resistor to $V_{CC}1$.
4	—	4	4	—	$V_{CC}2$	Voltage Input 1. Power supply and input for the secondary µP voltage reset monitor.
—	4	3	—	—	RSTIN	Adjustable Reset Threshold Input. $\overline{RESET}$ is asserted when RSTIN is below the internal 0.488V reference level. Set the adjustable reset threshold with an external resistor-divider network. Connect RSTIN to $V_{CC}1$ if unused.
5	5	5	5	5	$V_{CC}1$	Voltage Input 2. Power supply and input for the primary µP voltage reset monitor.
—	—	—	—	4	PFI	Power-Fail Comparator Input. $\overline{PFO}$ is asserted when PFI is below 0.488V. $\overline{PFO}$ is deasserted without any reset timeout period when PFI goes above 0.488V. Connect PFI to an external resistor network to set the desired monitor threshold.
—	—	—	—	3	$\overline{PFO}$	Power-Fail Comparator Output, Open Drain Active Low. $\overline{PFO}$ is asserted when PFI is below 0.488V.
—	—	—	3	—	POK1	$V_{CC}1$ Power-OK Output, Open Drain Active High. POK1 remains low as long as $V_{CC}1$ is below $V_{TH}1$. POK1 output goes high after $V_{CC}1$ exceeds $V_{TH}1$ for the POK1 timeout period. POK1 logic is independent of the $\overline{MR}$ or $V_{CC}2$ inputs. The output can be used to control $V_{CC}1$-to-$V_{CC}2$ supply sequencing.

Table 1. Reset Voltage Threshold Suffix Guide for MAX6736/MAX6737/MAX6740/MAX6741/MAX6743/MAX6744

PART NO. SUFFIX (_ _)	$V_{CC}1$ NOMINAL VOLTAGE THRESHOLD (V)	$V_{CC}2$ NOMINAL VOLTAGE THRESHOLD (V)
LT	**4.625**	**3.075**
MS	4.375	2.925
MR	4.375	2.625
TZ	3.075	2.313
TW	3.075	1.665
TI	3.075	1.388
TG	**3.075**	**1.110**
TE	3.075	0.833
SY	**2.925**	**2.188**
SV	**2.925**	**1.575**
SH	**2.925**	**1.313**
SF	2.925	1.050
SD	**2.925**	**0.788**
RY	2.625	2.188
RV	**2.625**	**1.575**
RH	2.625	1.313
RF	2.625	1.050
RD	2.625	0.788
ZW	**2.313**	**1.665**
ZI	2.313	1.388
ZG	**2.313**	**1.110**
ZE	2.313	0.833
YV	2.188	1.575
YH	**2.188**	**1.313**
YF	2.188	1.050
YD	**2.188**	**0.788**
WT	**1.665**	**3.075**
WI	1.665	1.388
WG	**1.665**	**1.110**
WE	1.665	0.833
VR	**1.575**	**2.625**
VH	**1.575**	**1.313**
VF	1.575	1.050
VD	**1.575**	**0.788**

Note: *Standard versions, shown in bold, are available in the D3 timeout option only. Samples are typically held on standard versions only. There is a 10,000-piece order increment on nonstandard versions.* ***Other threshold voltage combinations may be available; contact factory for availability.***

Table 2. Reset Voltage Threshold Suffix Guide for MAX6738/MAX6739/MAX6742/MAX6745

PART NO. SUFFIX (_)	$V_{CC}1$ NOMINAL VOLTAGE THRESHOLD (V)
L	**4.625**
M	4.375
T	3.075
S	**2.925**
R	**2.625**
Z	**2.313**
Y	2.188
W	1.665
V	**1.575**

Note: *Standard versions, shown in bold, are available in the D3 timeout option only. Samples are typically held on standard versions only. There is a 10,000-piece order increment on nonstandard versions.* ***Other threshold voltages may be available; contact factory for availability****.*

Table 3. V_{CC} Timeout Period Suffix Guide

TIMEOUT PERIOD SUFFIX	ACTIVE TIMEOUT PERIOD	
	MIN (ms)	MAX (ms)
D3	150	300
D7	1200	2400

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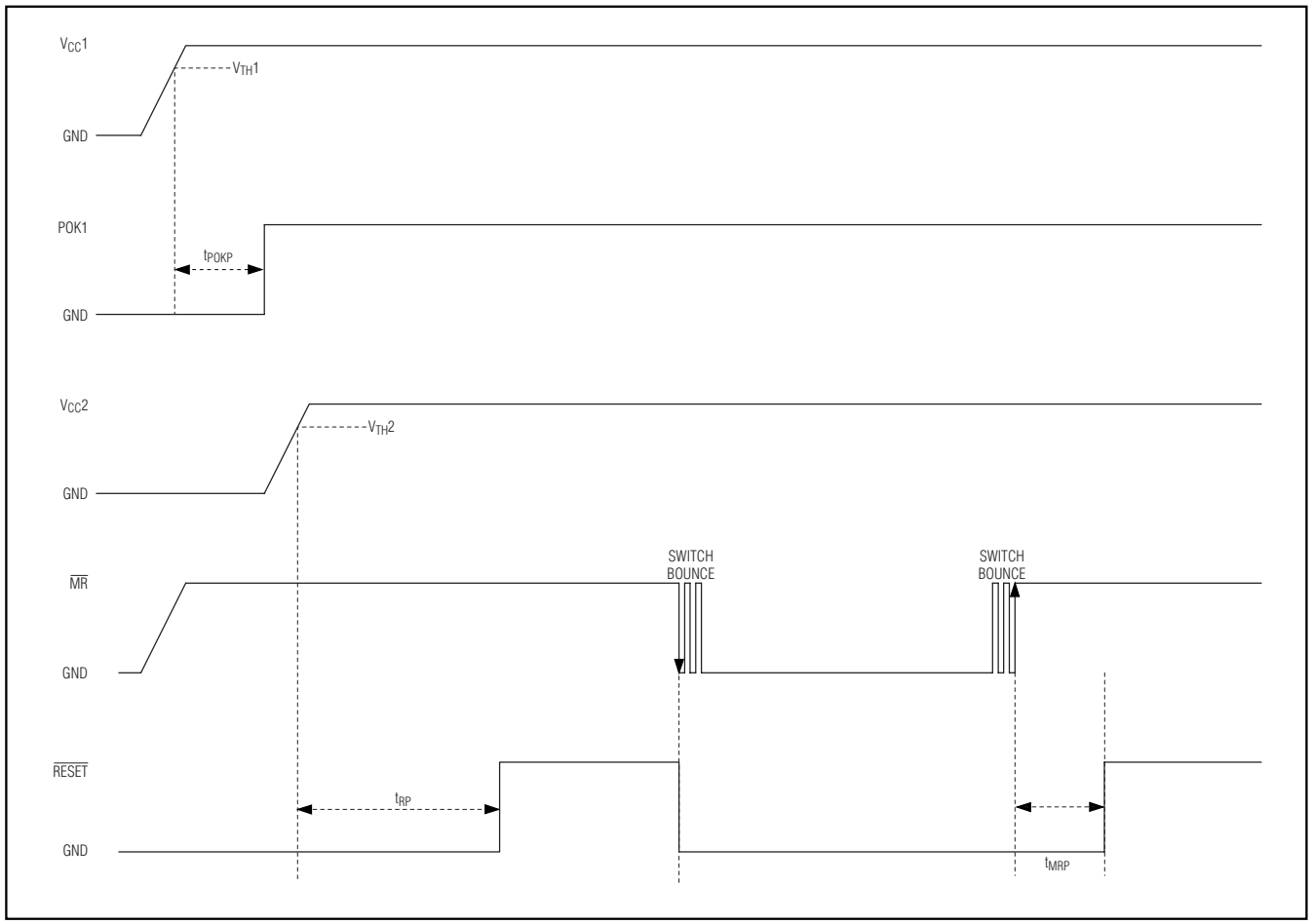


Figure 1. Timing Diagram

Detailed Description

Supply Voltages

The MAX6736–MAX6745 µP supervisory circuits maintain system integrity by alerting the µP to fault conditions. These devices are optimized for systems that monitor two or three supply voltages. The reset output state is guaranteed to remain valid while either $V_{CC}1$ or $V_{CC}2$ is above 1.2V.

Threshold Levels

The MAX6736/MAX6737/MAX6740/MAX6741/MAX6743/MAX6744 input voltage threshold combinations are indicated by a two-letter code in Table 1. The MAX6738/MAX6739/MAX6742/MAX6745 input voltage thresholds are indicated by a one-letter code in Table 2. Contact the factory for the availability of other voltage thresholds.

Reset Output

The MAX6736–MAX6745 provide an active-low reset output ($\overline{RESET}$). $\overline{RESET}$ is asserted when the voltage at either $V_{CC}1$ or $V_{CC}2$ falls below the voltage threshold level, RSTIN drops below the threshold, or $\overline{MR}$ is pulled low. Once reset is asserted, it stays low for the reset timeout period. If $V_{CC}1$, $V_{CC}2$, or RSTIN goes below the reset threshold before the reset timeout period is completed, the internal timer restarts. The MAX6736/MAX6738/MAX6740/MAX6741/MAX6742 have open-drain reset outputs, while the MAX6737/MAX6739/MAX6743/MAX6744/MAX6745 have push-pull reset outputs (Figure 1).

The MAX6740/MAX6741/MAX6742 include a $\overline{RESET}$ output with a manual reset detect function. The open-drain $\overline{RESET}$ output has an internal 50kΩ pullup to $V_{CC}1$. The $\overline{RESET}$ output is low while the output is pulled to GND and remains low for at least the manual reset timeout period after the external GND pulldown is

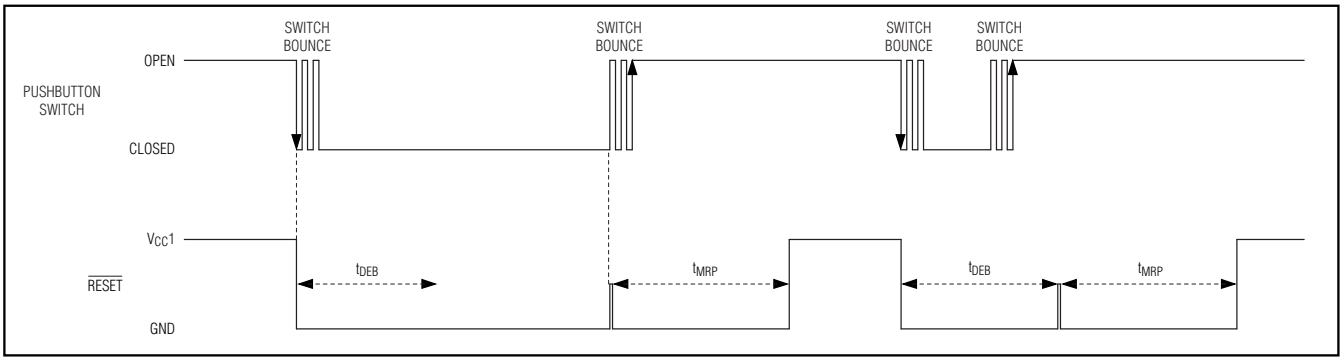


Figure 2. MAX6740/MAX6741/MAX6742 Manual Reset Timing Diagram

released. The manual reset detect function is internally debounced for the t_{DEB} timeout period, so the output can be connected directly to a momentary pushbutton switch, if desired (Figure 2).

Manual Reset Input

Many microprocessor-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset while the monitored supplies remain above their reset thresholds. The MAX6736–MAX6739 have a dedicated active-low $\overline{MR}$ input. The $\overline{RESET}$ is asserted low while $\overline{MR}$ is held low and remains asserted for the manual reset timeout period after $\overline{MR}$ returns high. The $\overline{MR}$ input has an internal 1.5kΩ pullup resistor to $V_{CC}1$ and can be left unconnected if not used. $\overline{MR}$ can be driven with CMOS logic levels, open-drain/open-collector outputs, or a momentary pushbutton switch to GND to create a manual reset function.

Adjustable Input Voltage

The MAX6738/MAX6739 and MAX6740/MAX6743 provide an additional input to monitor a second or third system voltage. The threshold voltage at RSTIN is typically 488mV. Connect a resistor-divider network to the circuit as shown in Figure 3 to establish an externally controlled threshold voltage, V_{EXT_TH}.

$$V_{EXT\_TH} = 0.488V((R1 + R2) / R2)$$

Low leakage current at RSTIN allows the use of large-valued resistors, resulting in reduced power consumption of the system.

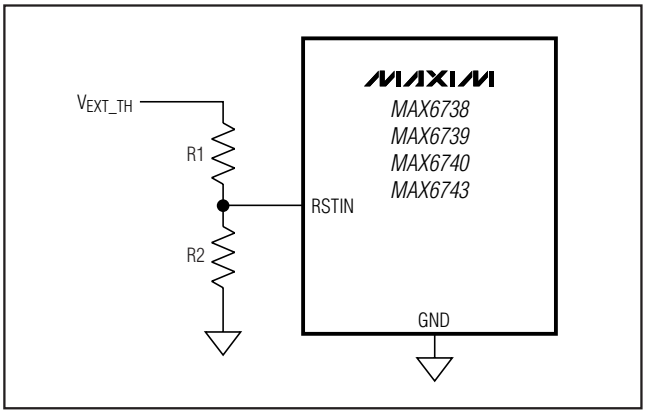


Figure 3. Monitoring an Additional Voltage

Power-Fail Comparator

PFI is the noninverting input to an auxiliary comparator. A 488mV internal reference (V_{TH-PFI}) is connected to the inverting input of the comparator. If PFI is less than 488mV, $\overline{PFO}$ is asserted low. $\overline{PFO}$ deasserts without a timeout period when PFI rises above the externally set threshold. Common uses for the power-fail comparator include monitoring for low battery conditions or a failing DC-DC converter input voltage (see the *Typical Application Circuits*). The asserted $\overline{PFO}$ output can place a system in a low-power suspend mode or support an orderly system shutdown before monitored V_{CC} voltages drop below the reset thresholds. Connect PFI to an external resistor-divider network as shown in Figure 4 to set the desired trip threshold. Connect PFI to $V_{CC}1$ if unused.

Applications Information

Interfacing to the µP with Bidirectional Reset Pins

Most microprocessors with bidirectional reset pins can interface directly to open-drain $\overline{RESET}$ output options. Systems simultaneously requiring a push-pull RESET output and a bidirectional reset interface can be in logic contention. To prevent contention, connect a 4.7kΩ resistor between $\overline{RESET}$ and the µP's reset I/O port as shown in Figure 5.

Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

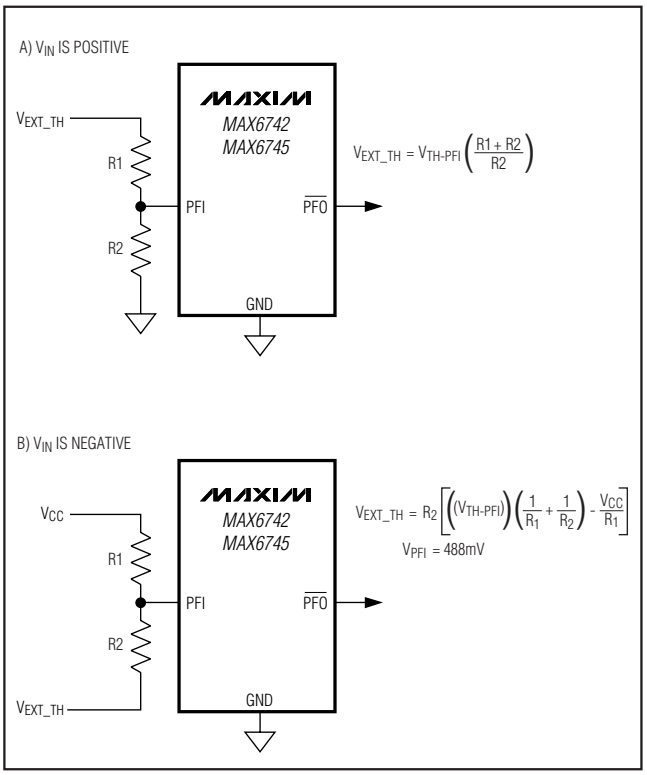


Figure 4. Using Power-Fail Input to Monitor an Additional Power Supply

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 2.5mV. This is sufficient for most applications in which a power-supply line is being monitored through an external voltage-divider. If additional noise margin is desired, connect a resistor between $\overline{PFO}$ and PFI, as shown in Figure 6. Select the values of R1, R2, and R3 such that PFI sees V_{TH-PFI} (488mV) when V_{EXT} falls to its power-fail trip point (V_{FAIL}) and when V_{EXT} rises to its power-good trip point (V_{GOOD}). The hysteresis window extends between the specified V_{FAIL} and V_{GOOD} thresholds. R3 adds the additional hysteresis by sinking current from the R1/R2 divider network when the $\overline{PFO}$ output is logic low and sourcing current into the network when $\overline{PFO}$ is logic high. R3 is typically an order of magnitude greater than R1 or R2.

The current through R2 should be at least 1µA to ensure that the 10nA (max) PFI input current does not significantly shift the trip points. Therefore, for most applications:

$$R2 < V_{TH-PFI} / 1mA < 0.488V / 1mA < 488k\Omega$$

$\overline{PFO}$ is an open-drain output requiring an external pullup resistor, R4. Select R4 to be less than 1% of R3.

V_{GOOD} = DESIRED V_{EXT} GOOD VOLTAGE THRESHOLD

V_{FAIL} = DESIRED V_{EXT} FAIL VOLTAGE THRESHOLD

V_{PU} = V_{PULLUP} (FOR OPEN-DRAIN $\overline{PFO}$)

R2 = 488kΩ (FOR >1µA R2 CURRENT)

$$R1 = R2 \frac{\left(V_{GOOD} - V_{TH-PFI}\right) - \frac{\left(V_{TH-PFI}(V_{GOOD} - V_{FAIL}\right)}{V_{PU}}}{V_{TH-PFI}}$$

$$R3 = (R1 \times V_{PU}) / (V_{GOOD} - V_{FAIL})$$

$$R4 \le 0.01 \times R3$$

Power Sequencing Applications

Many dual-voltage processors/ASICs require specific power-up/power-down sequences for the I/O and core supplies.

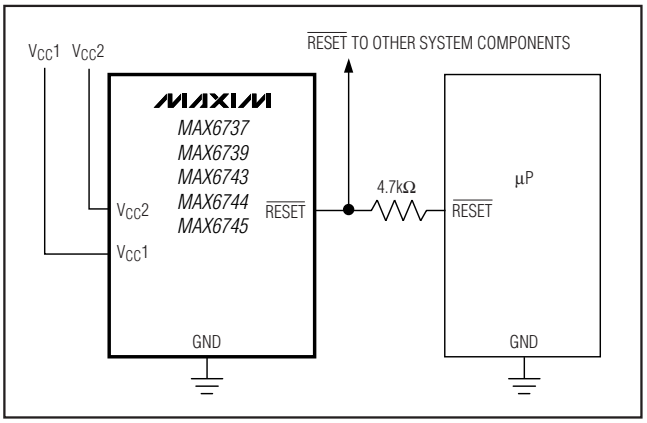


Figure 5. Interfacing to µPs with Bidirectional Reset I/O

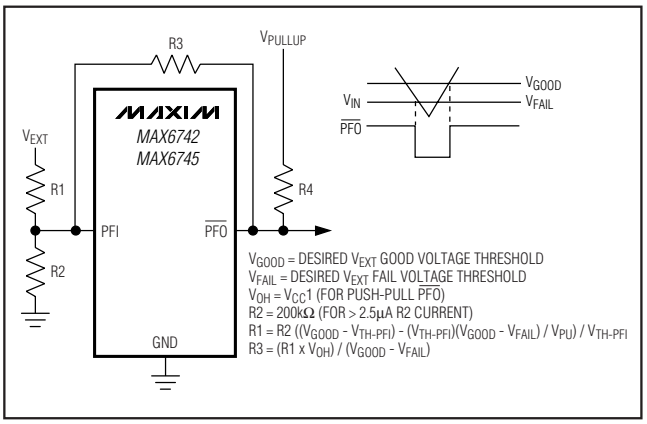


Figure 6. Adding Hysteresis to Power Fail for Push-Pull $\overline{PFO}$

The MAX6741/MAX6744 offer a $V_{CC}1$ POK (POK1) ideal for $V_{CC}1$-to-$V_{CC}2$ sequencing. POK1 remains low as long as $V_{CC}1$ is below its $V_{TH}1$ threshold. When $V_{CC}1$ exceeds $V_{TH}1$ for the POK1 timeout period (t_{POKP}), the open-drain POK1 output is deasserted. The POK1 output can then enable the $V_{CC}2$ power supply (use an external POK1 pullup resistor). $\overline{RESET}$ is deasserted when both $V_{CC}1$ and $V_{CC}2$ remain above their selected thresholds for the reset timeout period (t_{RP}). The POK1 output can be used for I/O before core or core before I/O sequencing, depending on the selected $V_{CC}1$/$V_{CC}2$ thresholds. See the *Typical Application Circuit* and Figure 1.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit shown in Figure 4. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. The circuit's accuracy is affected by the PFI threshold tolerance, V_{CC}, R1, and R2.

Transient Immunity

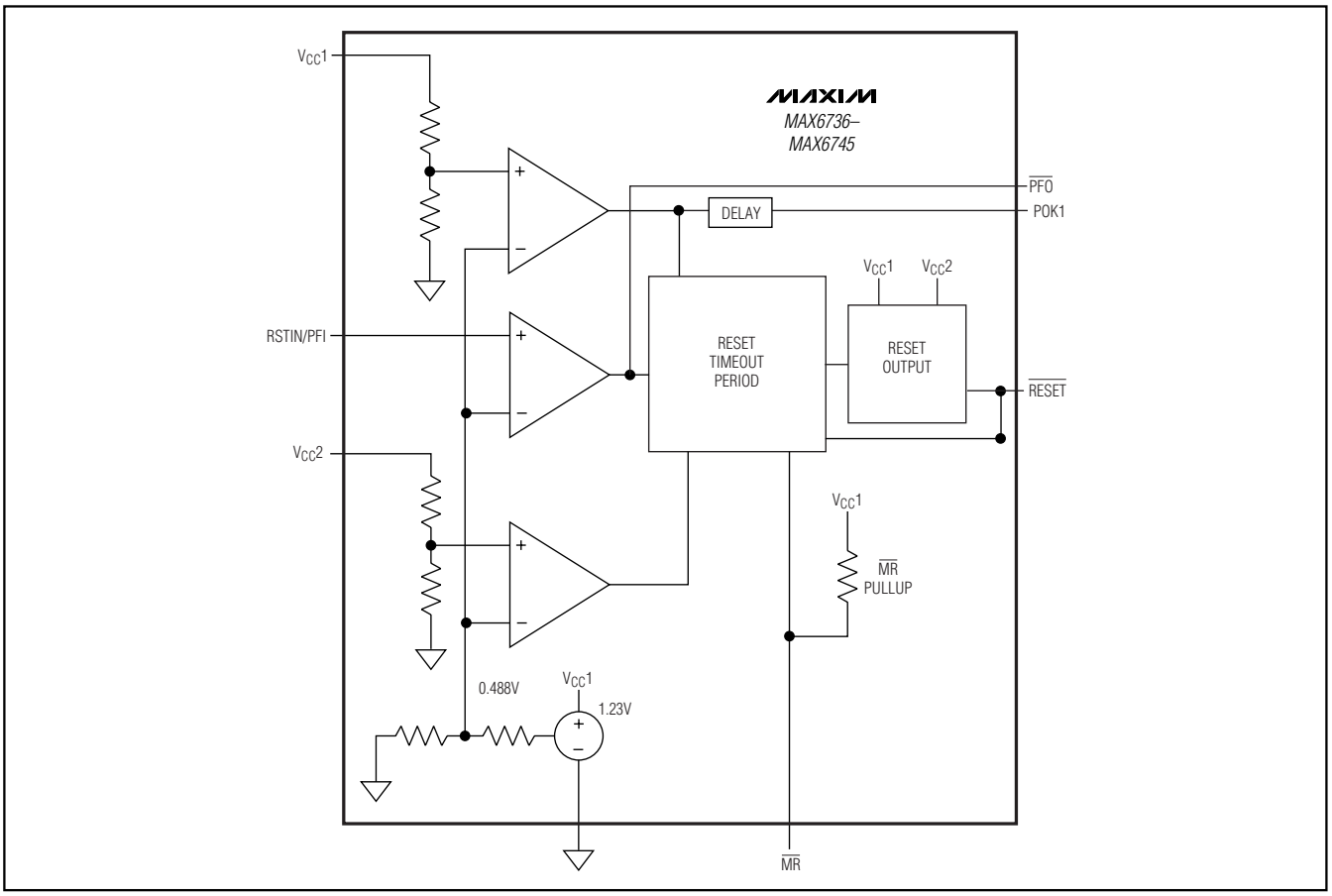
The MAX6736–MAX6745 supervisors are relatively immune to short-duration falling V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches. The *Typical Operating Characteristics* show Maximum $V_{CC}1$/$V_{CC}2$ Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph shows the maximum pulse width that a falling V_{CC} transient might typically have without causing a reset pulse to be issued. As the amplitude of the transient increases, the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Chip Information

TRANSISTOR COUNT: 249

PROCESS: BiCMOS

Functional Diagram



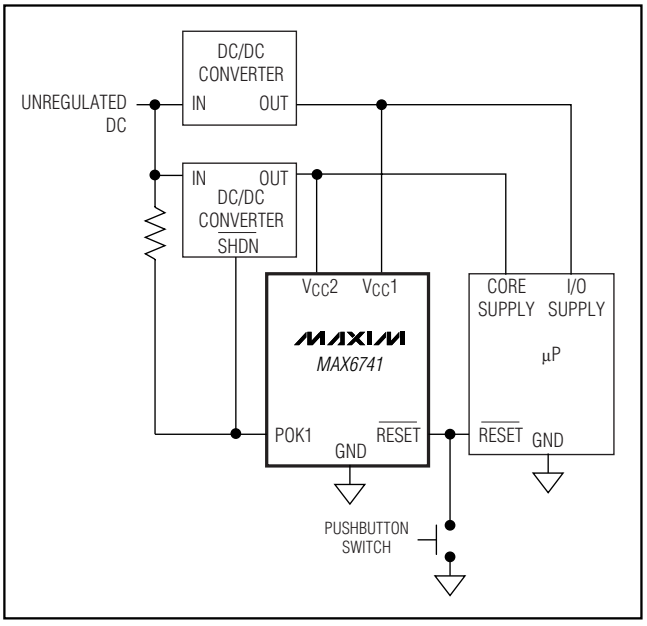
Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

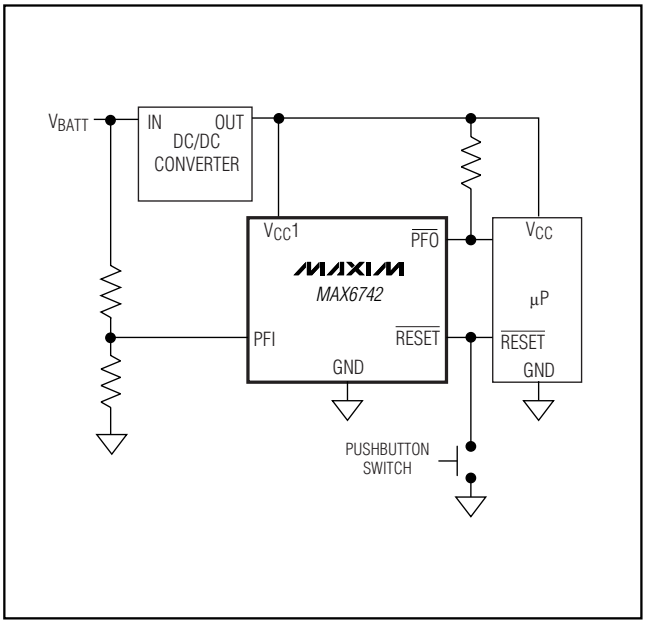
Selector Guide (continued)

PART	VOLTAGE MONITORS	OPEN-DRAIN $\overline{\text{RESET}}$	PUSH-PULL $\overline{\text{RESET}}$	MANUAL RESET	POWER-FAIL INPUT/ OUTPUT	POK OUTPUT	RSTIN INPUT
MAX6739	1 fixed, 1 adj	—	X	X	—	—	X
MAX6740	2 fixed, 1 adj	X*	—	X*	—	—	X
MAX6741	2 fixed	X*	—	X*	—	X	—
MAX6742	1 fixed	X*	—	X*	X	—	—
MAX6743	2 fixed, 1adj	—	X	—	—	—	X
MAX6744	2 fixed	—	X	—	—	X	—
MAX6745	1 fixed	—	X	—	X	—	—

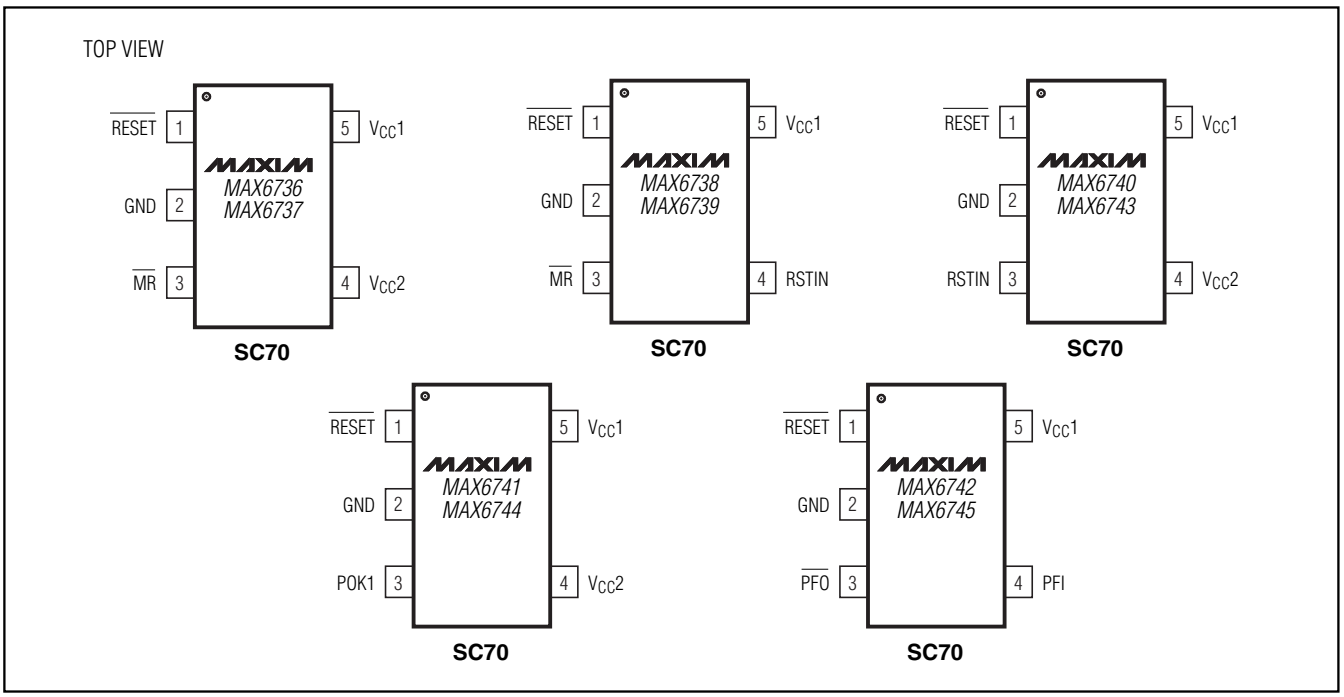
*Manual reset detect on $\overline{\text{RESET}}$ output.

Typical Application Circuits





Pin Configurations



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX6738XK_D_-T	-40°C to +85°C	5 SC70-5
MAX6739XK_D_-T	-40°C to +85°C	5 SC70-5
MAX6740XK_ _D_-T	-40°C to +85°C	5 SC70-5
MAX6741XK_ _D_-T	-40°C to +85°C	5 SC70-5
MAX6742XK_D_-T	-40°C to +85°C	5 SC70-5
MAX6743XK_ _D_-T	-40°C to +85°C	5 SC70-5
MAX6744XK_ _D_-T	-40°C to +85°C	5 SC70-5
MAX6745XK_D_-T	-40°C to +85°C	5 SC70-5

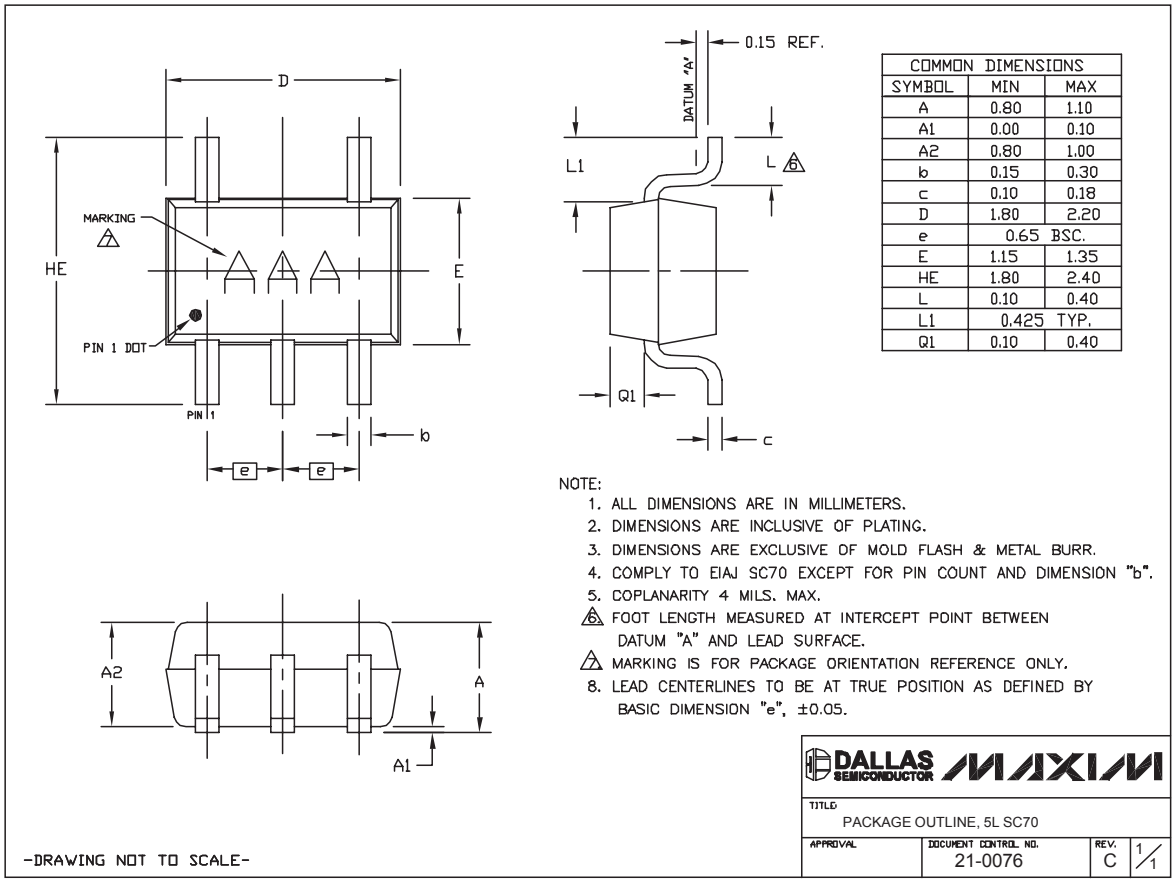
Note: *The first "_ _" or "_" are placeholders for the threshold voltage levels of the devices. Desired threshold levels are set by the part number suffix found in Tables 1 and 2. The "_" after the D is a placeholder for the reset timeout period suffix found in Table 3. For example, the MAX6736XKLTD3-T is a dual-voltage supervisor $V_{TH}1$ = 4.625V, $V_{TH}2$ = 3.075V, and a 150ms minimum reset timeout period. All devices are available in tape-and-reel only. There is a 2500-piece minimum order increment for standard versions (see Table 1). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.*

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Low-Power Dual-/Triple-Voltage SC70 µP Supervisory Circuits

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.15	0.30
c	0.10	0.18
D	1.80	2.20
e	0.65 BSC.	
E	1.15	1.35
HE	1.80	2.40
L	0.10	0.40
L1	0.425 TYP.	
Q1	0.10	0.40

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO EIAJ SC70 EXCEPT FOR PIN COUNT AND DIMENSION "b".
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

DALLAS SEMICONDUCTOR MAXIM

TITLE			
PACKAGE OUTLINE, 5L SC70			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0076	C	1/1

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