Absolute Maximum Ratings

V_{CC}, OUT, OUTA, OUTB, $\overline{CLEAR}$ to GND .....-0.3V to +30.0V
IN+, IN- to GND.....-0.3V to (V_{CC} + 0.3V)
REF to GND .....-0.3V to the lower of +6V and (V_{CC} + 0.3V)
Input Currents (V_{CC}, IN+, IN-) 20mA
Sink Current (OUT, OUTA, OUTB).....20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1 mW/°C above +70°C) 571mW
6-Pin SOT23 (derate 8.7 mW/°C above +70°C) 696mW
Junction Temperature.....+150°C
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-free.....+260°C
Containing lead (Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

5 SOT23

PACKAGE CODE	U5+1
Outline Number	21-0057
Land Pattern Number	90-0174
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	324.3°C/W
Junction to Case (θ_{JC})	82°C/W
Thermal Resistance, Multi-Layer Board:	
Junction to Ambient (θ_{JA})	255.9°C/W
Junction to Case (θ_{JC})	81°C/W

6 SOT23

PACKAGE CODE	U6+1/U6+1A
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Single-Layer Board:	
Junction to Case (θ_{JC})	80°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	115°C/W
Junction to Case (θ_{JC})	80°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 4V to 28V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	(Note 2)			4		28	V
Supply Current	I_{CC}	V_{CC} = 5V, no load				2	5	µA
		V_{CC} = 12V, no load				3.5	7.5	
		V_{CC} = 24V, no load				6.5	12.5	
Threshold Voltage	V_{TH+}	V_{IN} rising	T_A = -40°C to +85°C, V_{CC} ≥ 4V		1.195	1.228	1.255	V
			T_A = +85°C to +125°C, V_{CC} ≥ 4V		1.170		1.255	
	V_{TH-}	V_{IN} falling	MAX645_U_D_A	T_A = -40°C to +85°C	1.180		1.255	
				T_A = +85°C to +125°C	1.155		1.255	
			MAX645_U_D_B	T_A = -40°C to +85°C	1.133		1.194	
				T_A = +85°C to +125°C	1.111		1.194	
			MAX645_U_D_C	T_A = -40°C to +85°C	1.093		1.151	
				T_A = +85°C to +125°C	1.071		1.151	
Threshold Voltage Hysteresis		MAX64_ _U_D_A				0.5		%V_{TH+}
		MAX64_ _U_D_B				5		
		MAX64_ _U_D_C				8.3		
IN Operating Voltage Range	V_{IN}	(Note 2)			0		V_{CC}	V
IN Leakage Current	I_{IN}	V_{IN} = 1.25V, V_{CC} = +28V			-55		+55	nA
OUT Timeout Period	t_{TP}	MAX645_UKD0_ MAX6459UT_ MAX6460UT				50		µs
		MAX6457 and MAX6458 only, D3 option			90	150	210	ms
Startup Time		V_{CC} rising from GND to V_{CC} ≥ 4V in less than 1µs (Note 3)				2		ms
$\overline{CLEAR}$ Input Logic Voltage (MAX6457)	V_{IL}						0.4	V
	V_{IH}				2			

Electrical Characteristics (continued)

(V_{CC} = 4V to 28V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Low	V_{OL}	V_{CC} ≥ 1.5V, I_{SINK} = 250µA, OUT asserted, T_A = -40°C to +85°C			0.4	V
		V_{CC} ≥ 4.0V, I_{SINK} = 1mA, OUT asserted, T_A = -40°C to +125°C			0.4	
Output Leakage Current	I_{LKG}	V_{CC} = 5V, V_{OUT} = 28V (Note 4)			500	nA
Output Short-Circuit Sink	I_{SC}	OUT asserted, OUT = V_{CC}		10		mA
MAX6460						
Reference Short-Circuit Current		REF = GND		7		mA
Reference Output Voltage	V_{REF}	T_A = -40°C to +85°C	2.183	2.25	2.303	V
		T_A = +85°C to +125°C	2.171	2.25	2.303	
Load Regulation		Sourcing: 0 ≤ I_{REF} ≤ 100µA, sinking: 0 ≤ $\|I_{REF}\|$ ≤ 300nA		50		µV/µA
Input Offset Voltage	V_{OFFSET}		-4.5		+4.5	mV
Input Hysteresis				6		mV
Input Bias Current	I_{BIAS}	V_{IN}+ = 1.4V, V_{IN}- = 1V	-25		+25	nA
Input Offset Current	I_{OFFSET}			2		pA
Common-Mode Voltage Range	CMVR		0		1.4	V
Common-Mode Rejection Ratio	CMRR			80		dB
Comparator Power-Supply Rejection Ratio	PSRR	V_{IN}+ = V_{IN}- = 1.4V		80		dB

Note 1: Devices are production tested at T_A = +25°C. Overtemperature limits are guaranteed by design.

Note 2: IN voltage monitoring requires that V_{CC} ≥ 4V, but OUT remains asserted in the correct undervoltage lockout state for V_{CC} down to 1.5V.

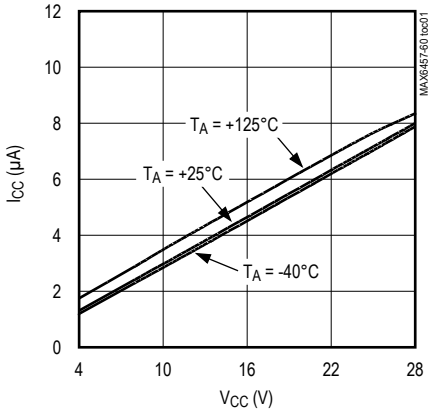
Note 3: Startup time is the time required for the internal regulator and reference to reach specified accuracy after the monitor is powered up from GND.

Note 4: The open-drain output can be pulled up to a voltage greater than V_{CC} but cannot exceed +28V.

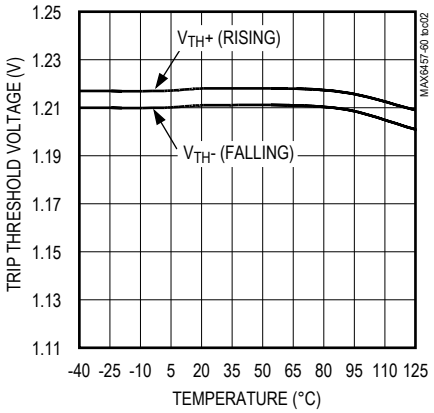
Typical Operating Characteristics

(GND = 0, R_{PULLUP} = 10kΩ, and T_A = +25°C, unless otherwise noted.)

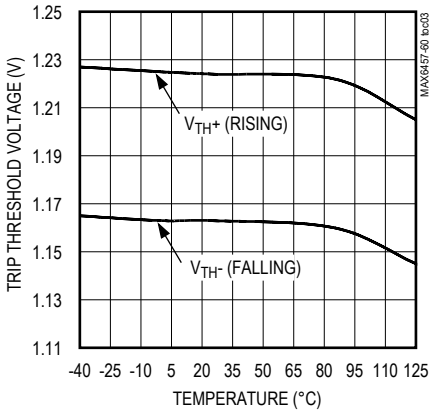
SUPPLY CURRENT vs. SUPPLY VOLTAGE



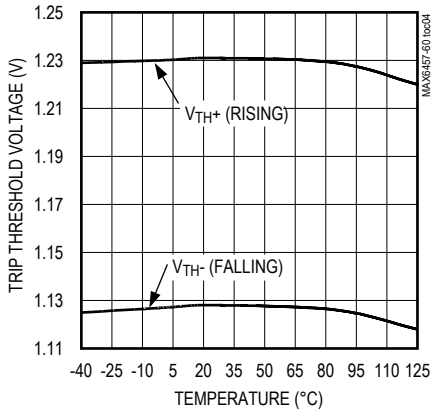
TRIP THRESHOLD VOLTAGE vs. TEMPERATURE (0.5% HYSTERESIS)



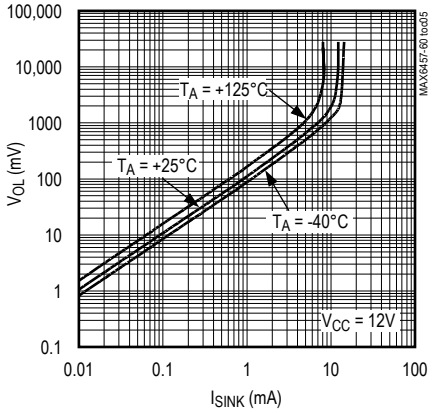
TRIP THRESHOLD VOLTAGE vs. TEMPERATURE (5% HYSTERESIS)



TRIP THRESHOLD VOLTAGE vs. TEMPERATURE (8.3% HYSTERESIS)



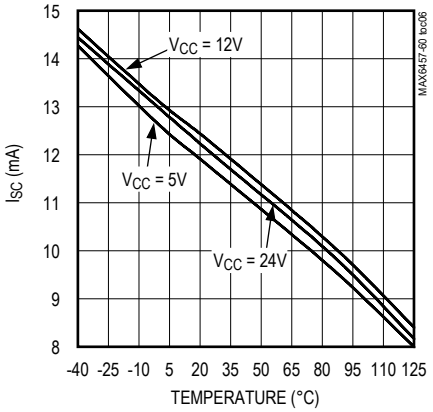
OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



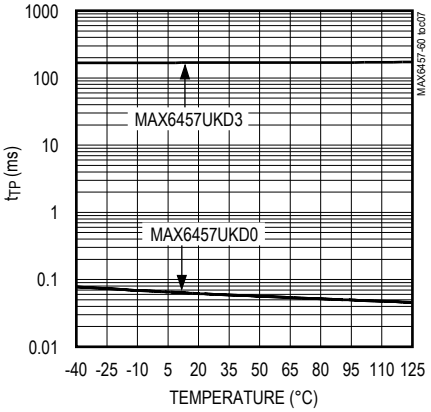
Typical Operating Characteristics (continued)

(GND = 0, R_{PULLUP} = 10kΩ, and T_A = +25°C, unless otherwise noted.)

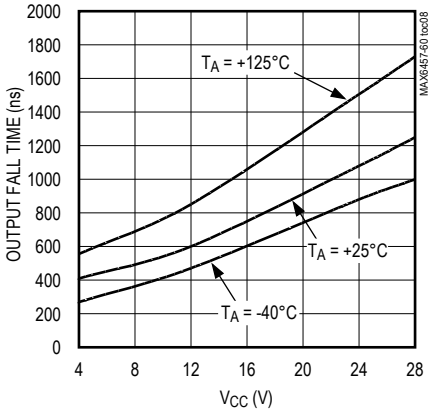
OUTPUT SHORT-CIRCUIT SINK CURRENT vs. TEMPERATURE



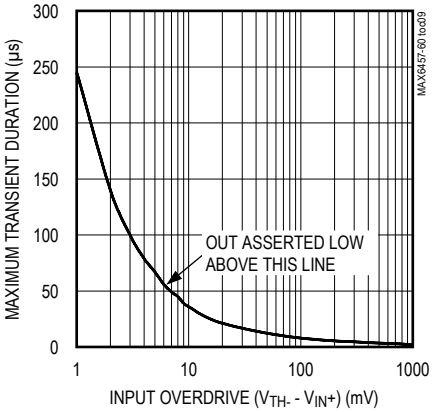
TIMEOUT PERIOD vs. TEMPERATURE



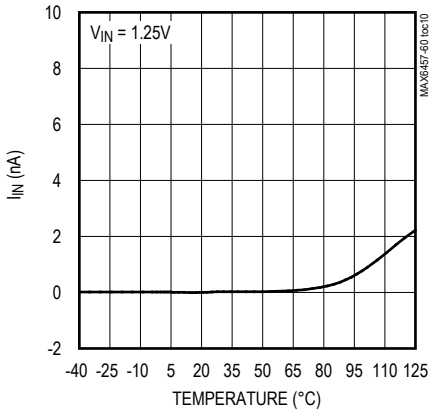
OUTPUT FALL TIME vs. SUPPLY VOLTAGE



MAXIMUM TRANSIENT DURATION vs. INPUT OVERDRIVE



INPUT LEAKAGE CURRENT vs. TEMPERATURE



Pin Description

PIN				NAME	FUNCTION
MAX6457	MAX6458	MAX6459	MAX6460		
1	1	—	1	OUT	**MAX6457:** Open-Drain Monitor Output. OUT requires an external pullup resistor. OUT asserts low for V_{CC} between 1.5V and 4V. OUT asserts low when V_{IN+} drops below V_{TH-} and goes high after the timeout period (t_{TP}) when V_{IN+} exceeds V_{TH+}.
					MAX6458: Open-Drain Monitor Output. OUT requires an external pullup resistor. OUT asserts low for V_{CC} between 1.5V and 4V. OUT asserts low when V_{IN+} drops below V_{TH-} or when V_{IN-} exceeds V_{TH+}. OUT goes high after the timeout period (t_{TP}) when V_{IN+} exceeds V_{TH+} and V_{IN-} drops below V_{TH-}.
					MAX6460: Open-Drain Monitor Output. OUT requires an external pullup resistor. OUT asserts low for V_{CC} between 1.5V and 4V. OUT asserts low when V_{IN+} drops below V_{IN-}. OUT goes high when V_{IN+} is above V_{IN-}.
—	—	1	—	OUTA	Open-Drain Monitor A Undervoltage Output. OUTA requires an external pullup resistor. OUTA goes low when V_{IN+} drops below V_{TH-} and goes high when V_{IN+} exceeds V_{TH+}. OUTA also goes low for V_{CC} between 1.5V and 4V.
—	—	5	—	OUTB	Open-Drain Monitor B Overvoltage Output. OUTB requires an external pullup resistor. OUTB goes low when V_{IN-} exceeds V_{TH+} and goes high when V_{IN-} drops below V_{TH-}. OUTB also goes low when V_{CC} drops below 4V.
2	2	2	2	GND	Ground
3	3	3	3	IN+	Adjustable Undervoltage Monitor Threshold Input. Noninverting input for MAX6460.
—	4	4	4	IN-	Adjustable Overvoltage Monitor Threshold Input. Inverting input for MAX6460.
4	—	—	—	$\overline{\text{CLEAR}}$	Clear Input. For $V_{IN+} > V_{TH+}$, drive $\overline{\text{CLEAR}}$ high to latch OUT high. Connect $\overline{\text{CLEAR}}$ to GND to make the latch transparent. $\overline{\text{CLEAR}}$ must be low when powering up the device. Connect $\overline{\text{CLEAR}}$ to GND when not used.
—	—	—	5	REF	Reference. Internal 2.25V reference output. Connect REF to IN+ through a voltage divider for active-low output. Connect REF to IN- through a voltage divider for active-high output. REF can source up to 100µA and sink up to 300nA. Leave REF floating when not used. REF output is stable with capacitive loads from 0 to 50pF or greater than 1µF.
5	5	6	6	V_{CC}	Supply Voltage

Functional Diagrams

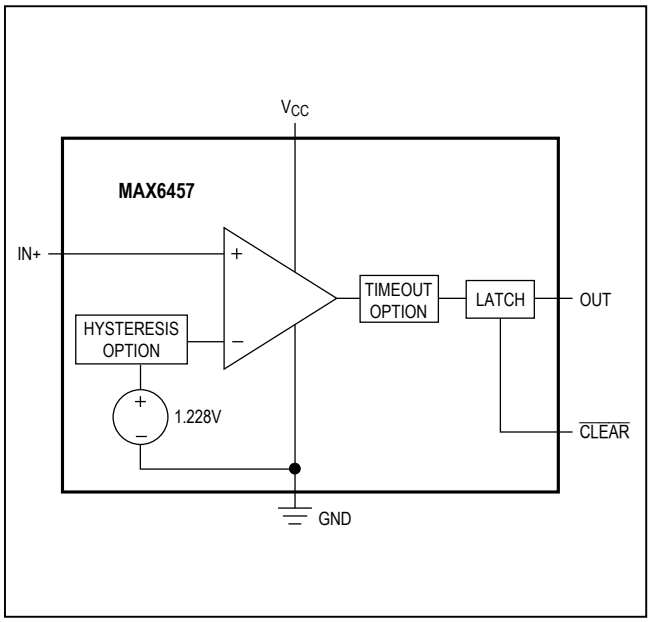


Figure 1. MAX6457 Functional Diagram

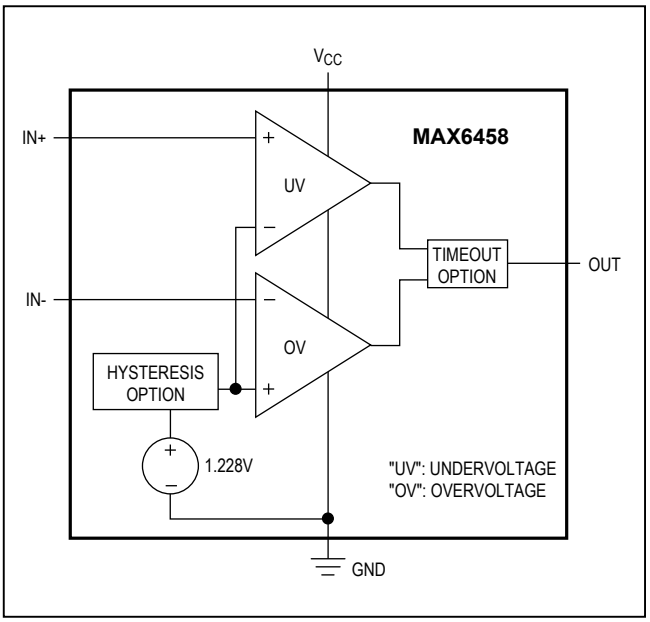


Figure 2. MAX6458 Functional Diagram

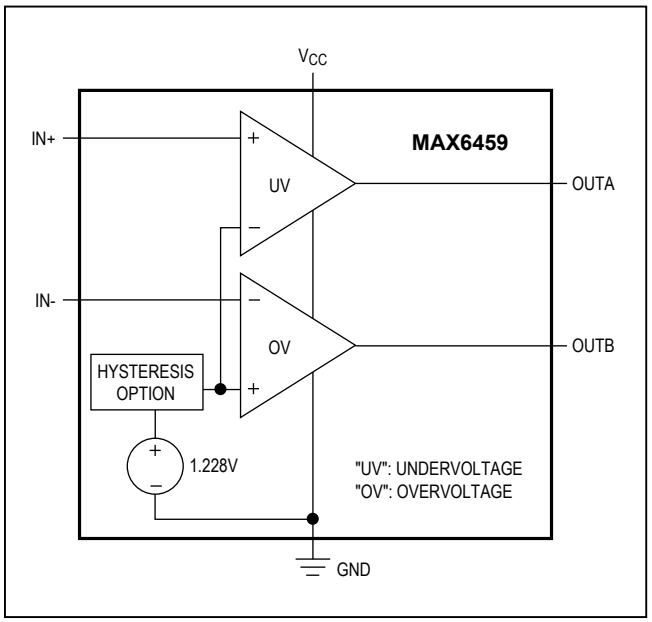


Figure 3. MAX6459 Functional Diagram

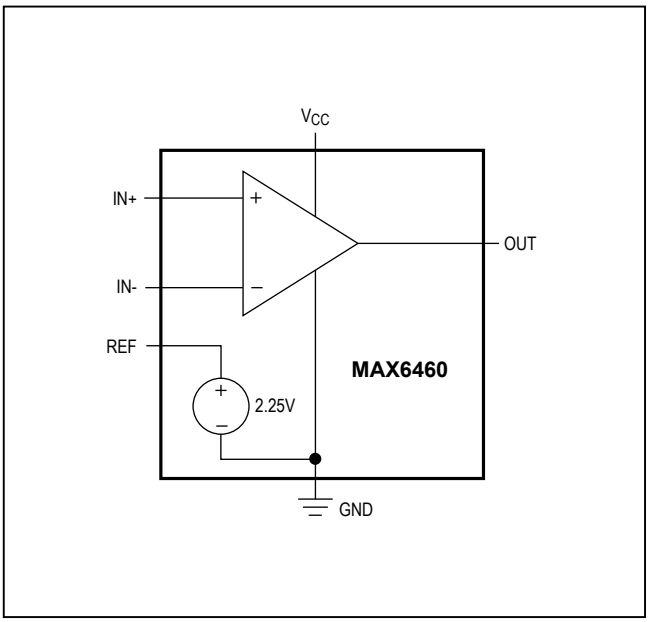


Figure 4. MAX6460 Functional Diagram

Detailed Description

Each of the MAX6457–MAX6460 high-voltage (4V to 28V), low-power voltage monitors include a precision bandgap reference, one or two low-offset-voltage comparators, internal threshold hysteresis, internal timeout period, and one or two high-voltage open-drain outputs.

Programming the Trip Voltage (V_{TRIP})

Two external resistors set the trip voltage, V_{TRIP} (Figure 5). V_{TRIP} is the point at which the applied voltage (typically V_{CC}) toggles OUT. The MAX6457/MAX6458/MAX6459/MAX6460's high input impedance allows large-value resistors without compromising trip-voltage accuracy. To minimize current consumption, select a value for R2 between 10kΩ and 1MΩ, then calculate R1 as follows:

$$R1 = R2\left(\frac{V_{TRIP}}{V_{TH}} - 1\right)$$

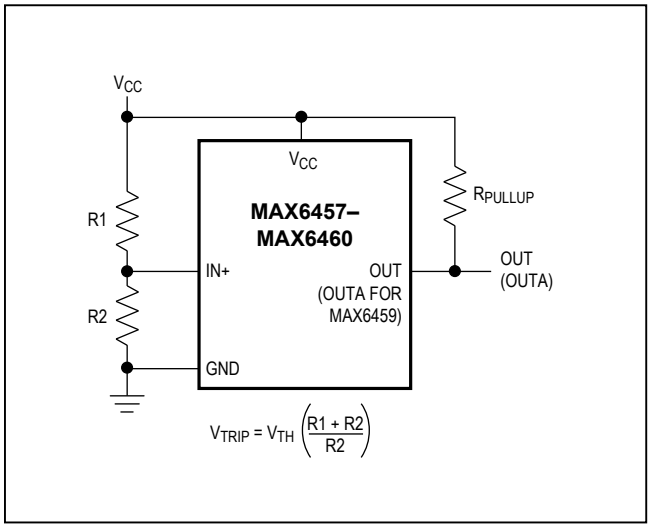


Figure 5a. Programming the Trip Voltage

where V_{TRIP} = desired trip voltage (in volts), V_{TH} = threshold trip voltage (V_{TH+} for overvoltage detection or V_{TH-} for undervoltage detection).

Use the MAX6460 voltage reference (REF) to set the trip threshold by connecting IN+ or IN- through a voltage divider (within the inputs common-mode voltage range) to REF. Do not connect REF directly to IN+ or IN- since this violates the input common-mode voltage range. Small leakage currents into the comparators inputs allows use of large value resistors to prevent loading the reference and affecting its accuracy. Figure 5b shows an active-high power-good output. Use the following equation to determine the resistor values when connecting REF to IN-:

$$V_{REFD} = V_{REF}\left(\frac{R4}{R3+R4}\right)$$

$$R1 = R2\left(\frac{V_{TRIP}}{V_{REFD}} - 1\right)$$

where V_{REF} = reference output voltage (2.25V, typ), V_{REFD} = divided reference, V_{TRIP} = desired trip threshold in (in volts).

For an active-low power-good output, connect the resistor divider R1 and R2 to the inverting input and the reference-divider network to the noninverting input. Alternatively, connect an external reference less than 1.4V to either input.

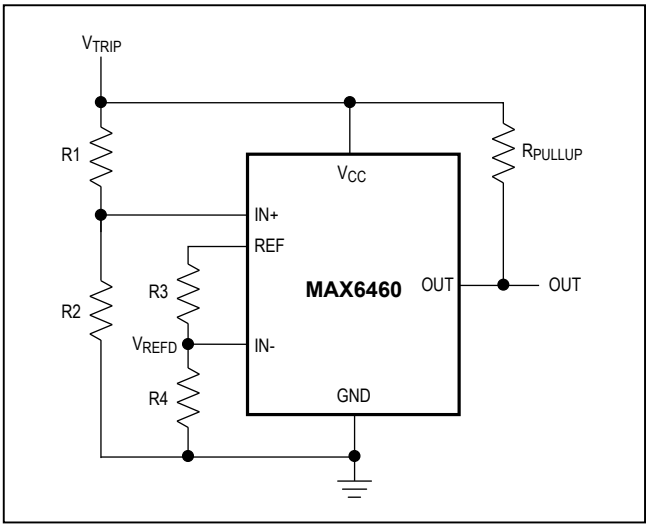


Figure 5b. Programming the MAX6460 Trip Voltage

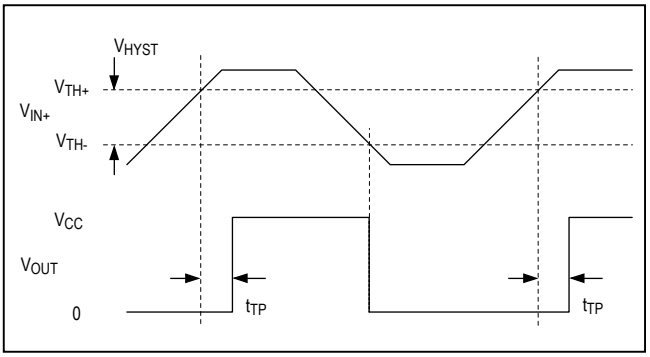


Figure 6. Input and Output Waveforms (Noninverting Input Varied)

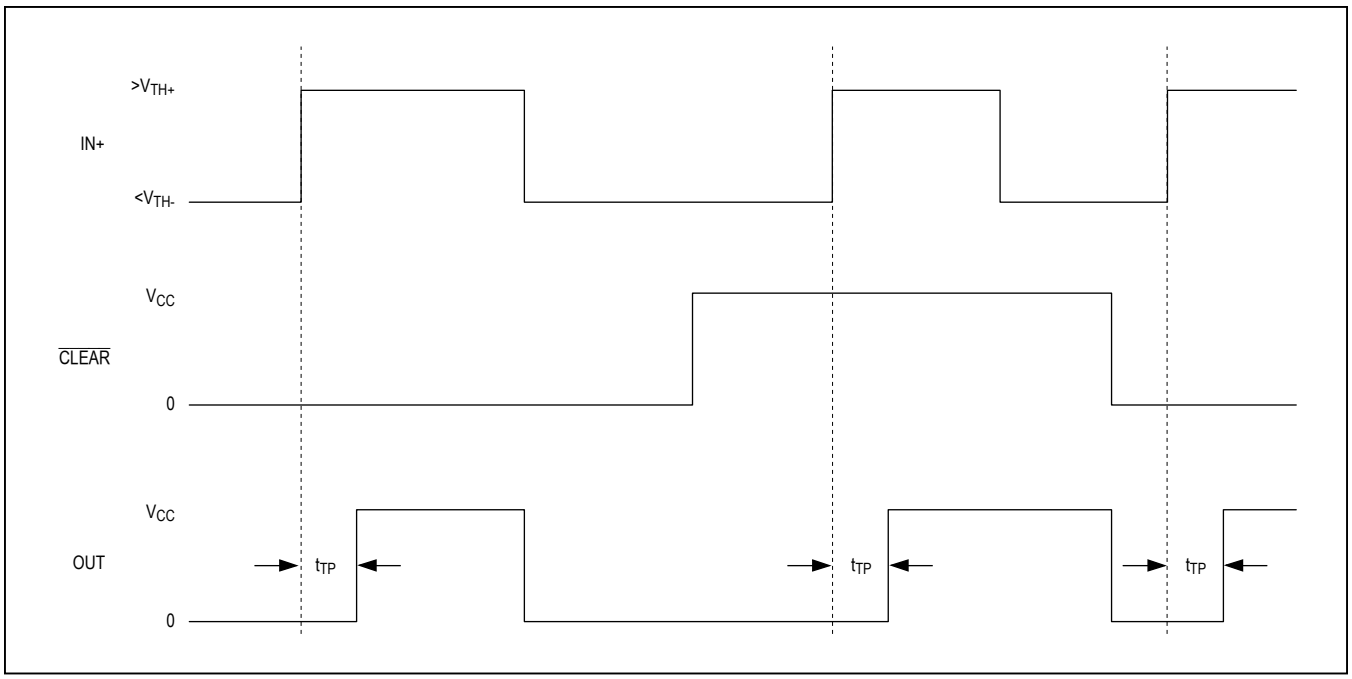


Figure 7. Timing Diagram (MAX6457)

Hysteresis

Hysteresis adds noise immunity to the voltage monitors and prevents oscillation due to repeated triggering when V_{IN} is near the threshold trip voltage. The hysteresis in a comparator creates two trip points: one for the rising input voltage (V_{TH+}) and one for the falling input voltage (V_{TH-}). These thresholds are shown in Figure 6.

The internal hysteresis options of the MAX6457/MAX6458/MAX6459 are designed to eliminate the need for adding an external hysteresis circuit.

Timeout Period

The timeout period (t_{TP}) for the MAX6457 is the time from when the input (IN+) crosses the rising input threshold (V_{TH+}) to when the output goes high (see Figures 6 and 7). For the MAX6458, the monitored voltage must be in the "window" before the timeout starts. The MAX6459 and MAX6460 do not offer the extended timeout option (150ms). The extended timeout period is suitable for overvoltage protection applications requiring transient immunity to avoid false output assertion due to noise spikes.

Latched-Output Operation

The MAX6457 features a digital latch input ($\overline{CLEAR}$) to latch any overvoltage event. If the voltage on IN+ (V_{IN+}) is below the internal threshold (V_{TH-}), or if V_{CC} is below

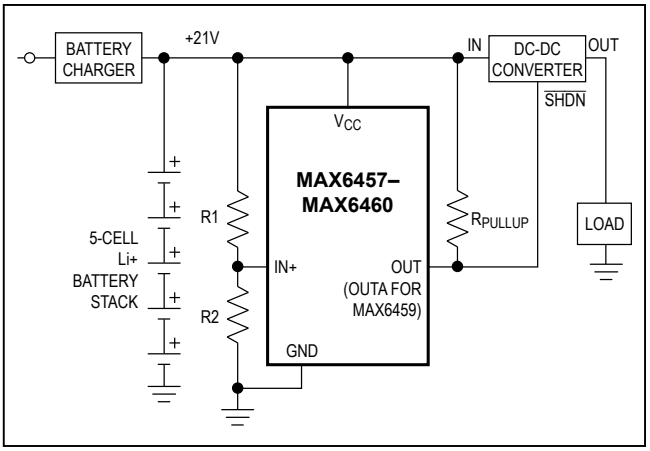


Figure 8. Undervoltage Lockout Typical Application Circuit

4V, OUT remains low regardless of the state of $\overline{CLEAR}$. Drive $\overline{CLEAR}$ high to latch OUT high when V_{IN+} exceeds V_{TH+}. When $\overline{CLEAR}$ is high, OUT does not deassert if V_{IN+} drops back below V_{IN-}. Toggle $\overline{CLEAR}$ to deassert OUT. Drive $\overline{CLEAR}$ low to make the latch transparent (Figure 7). $\overline{CLEAR}$ must be low when powering up the MAX6457. To initiate self-clear at power-up, add a 100kΩ pullup resistor from $\overline{CLEAR}$ to V_{CC} and a 1µF capacitor from $\overline{CLEAR}$ to GND to hold $\overline{CLEAR}$ low. Connect $\overline{CLEAR}$ to GND when not used. See Figure 9.

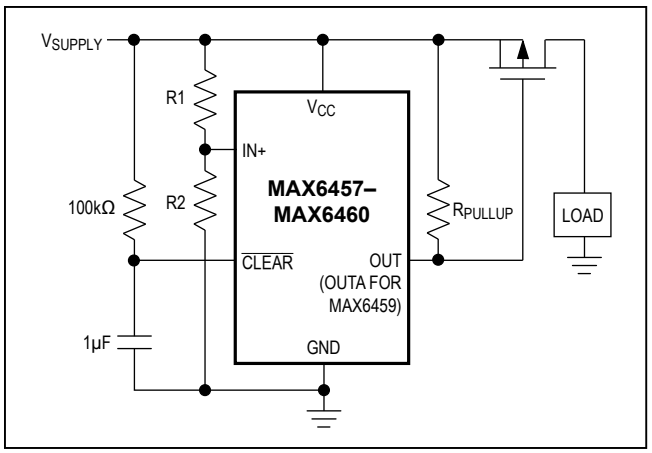


Figure 9. Overvoltage Shutdown Circuit (with External Pass MOSFET)

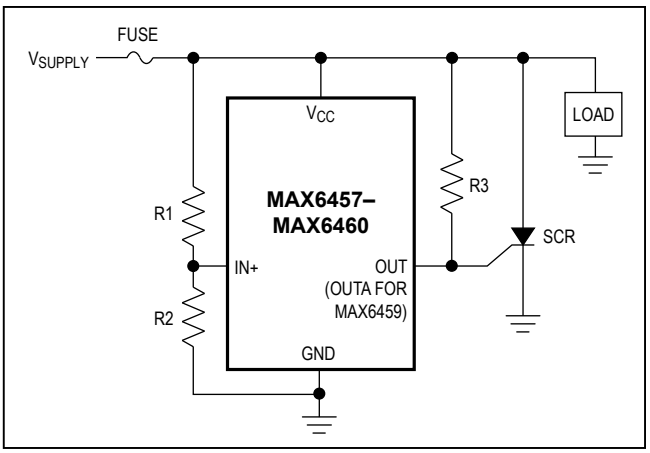


Figure 10. Overvoltage Shutdown Circuit (with SCR Fuse)

Applications Information

Undervoltage Lockout

Figure 8 shows the typical application circuit for detecting an undervoltage event of a 5-cell Li+ battery stack. Connect OUT of the MAX6457/MAX6458/MAX6460 (OUTA of the MAX6459) to the shutdown input of the DCDC converter to cut off power to the load in case of an undervoltage event. Select R1 and R2 to set the trip voltage (see the *Programming the Trip Voltage (V_{TRIP})* section). When the voltage of the battery stack decreases so that V_{IN+} drops below V_{TH-} of the MAX6457–MAX6460, then OUT (OUTA) goes low and disables the power supply to the load. When the battery charger restores the voltage of the 5-cell stack so that $V_{IN+} > V_{TH+}$, OUT (OUTA) goes high and the power supply resumes driving the load.

Overvoltage Shutdown

The MAX6457–MAX6460 are ideal for overvoltage shutdown applications. Figure 9 shows a typical circuit for this application using a pass P-channel MOSFET. The MAX6457–MAX6460 are powered directly from the system voltage supply. Select R1 and R2 to set the trip voltage (see the *Programming the Trip Voltage (V_{TRIP})* section). When the supply voltage remains below the selected threshold, a low logic level on OUT (OUTB for MAX6459) turns on the p-channel MOSFET. In the case of an overvoltage event, OUT (OUTB) asserts high, turns off the MOSFET, and shuts down the power to the load.

Figure 10 shows a similar application using a fuse and a silicon-controlled rectifier (SCR). An overvoltage event turns on the SCR and shorts the supply to ground. The surge of current through the short circuit blows the fuse and terminates the current to the load. Select R3 so that the gate of the SCR is properly biased when OUT (OUTB) goes high impedance.

Window Detection

The MAX6458/MAX6459 include undervoltage and overvoltage comparators for window detection (Figures 2 and 3). The circuit in Figure 11 shows the typical configuration for this application. For the MAX6458, OUT asserts high when V_{CC} is within the selected "window." When V_{CC} falls below the lower limit of the window ($V_{TRIPLOW}$) or exceeds the upper limit ($V_{TRIPHIGH}$), OUT asserts low.

The MAX6459 features two independent open-drain outputs: OUTA (for undervoltage events) and OUTB (for overvoltage events). When V_{CC} is within the selected window, OUTA and OUTB assert high. When V_{CC} falls below $V_{TRIPLOW}$, OUTA asserts low while OUTB remains

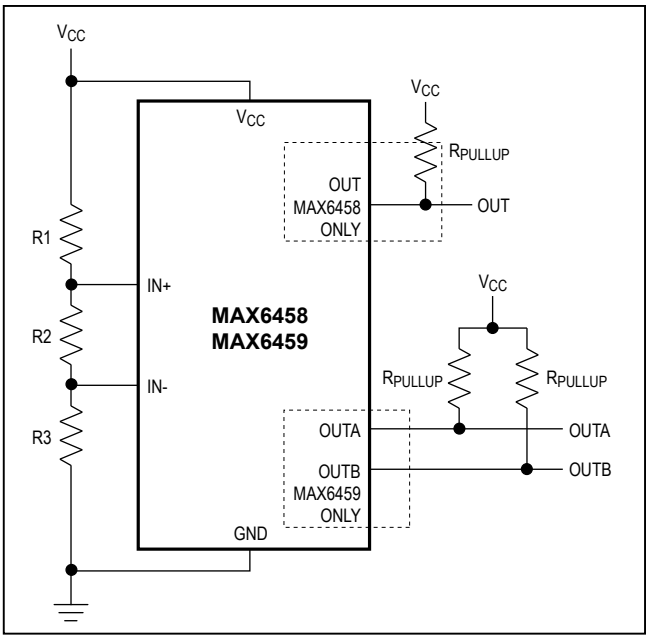


Figure 11. Window Detection

high. When V_{CC} exceeds $V_{TRIPHIGH}$, OUTB asserts low while OUTA remains high. $V_{TRIPLOW}$ and $V_{TRIPHIGH}$ are given by the following equations:

$$V_{TRIPLOW} = V_{TH-}\left(\frac{R_{TOTAL}}{R2 + R3}\right)$$

$$V_{TRIPHIGH} = V_{TH+}\left(\frac{R_{TOTAL}}{R3}\right)$$

where R_{TOTAL} = R1 + R2 + R3.

Use the following steps to determine the values for R1, R2, and R3.

1) Choose a value for R_{TOTAL}, the sum of R1, R2, and R3. Because the MAX6458/MAX6459 have very high input impedance, R_{TOTAL} can be up to 5MΩ.
2) Calculate R3 based on R_{TOTAL} and the desired upper trip point:

$$R3 = \frac{V_{TH+} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

3) Calculate R2 based on R_{TOTAL}, R3, and the desired lower trip point:

$$R2 = \frac{V_{TH-} \times R_{TOTAL}}{V_{TRIPLOW}} - R3$$

4) Calculate R1 based on R_{TOTAL}, R3, and R2:

$$R1 = R_{TOTAL} - R2 - R3$$

Example Calculations for Window Detection

The following is an example for calculating R1, R2, and R3 of Figure 11 for window detection. Select the upper and lower trip points ($V_{TRIPHIGH}$ and $V_{TRIPLOW}$).

V_{CC} = 21V

$V_{TRIPHIGH}$ = 23.1V

$V_{TRIPLOW}$ = 18.9V

For 5% hysteresis, V_{TH+} = 1.228 and V_{TH-} = 1.167.

1) Choose R_{TOTAL} = 4.2MΩ = R1 + R2 + R3
2) Calculate R3

$$R3 = \frac{V_{TH+} \times R_{TOTAL}}{V_{TRIPHIGH}} = \frac{(1.228V)(4.2M\Omega)}{23.1V}$$

$$= 223.273k\Omega$$

3) Calculate R2

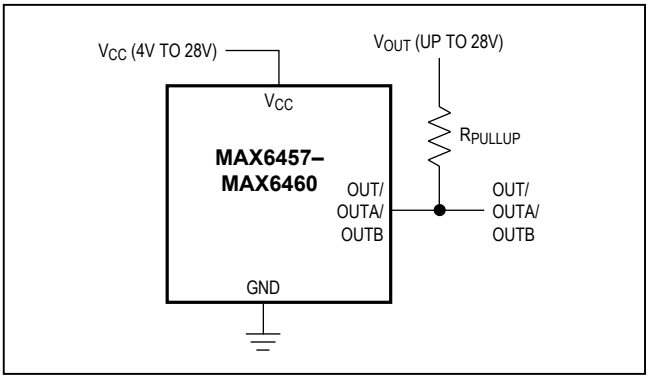


Figure 13. Interfacing to Voltages Other than V_{CC}

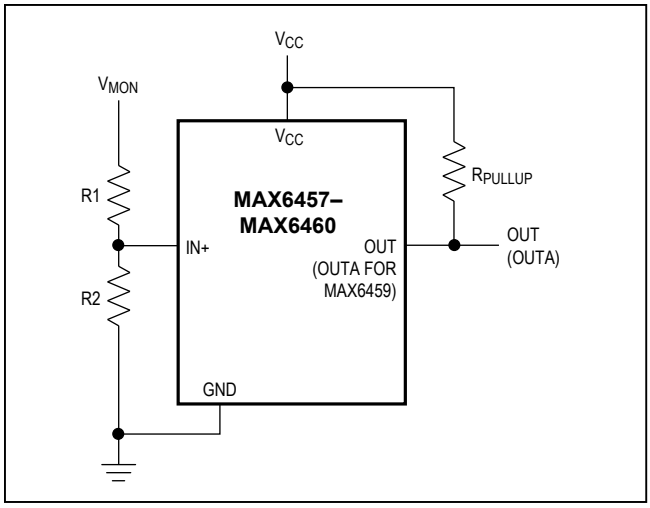


Figure 12. Monitoring Voltages Other than V_{CC}

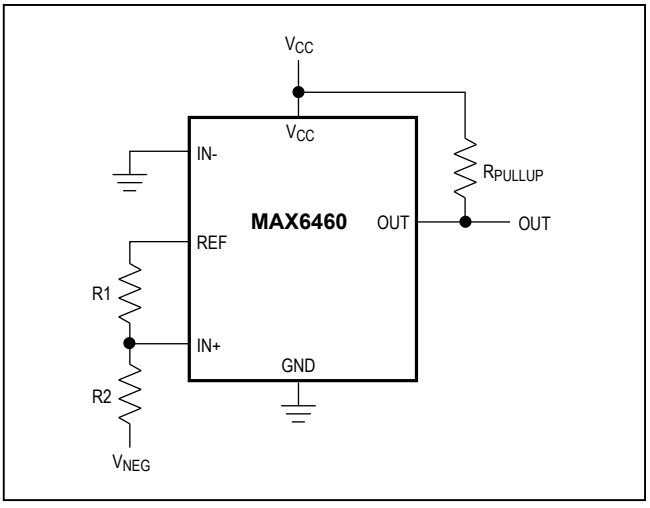


Figure 14. Monitoring Negative Voltages

Table 1. Factory-Trimmed Internal Hysteresis and Timeout Period Options

PART	SUFFIX	TIMEOUT OPTION	HYSTERESIS OPTION (%)
MAX6457UKD_ _ -T MAX6458UKD_ _ -T	0A	50µs	0.5
	0B	50µs	5
	0C	50µs	8.3
	3A	150ms	0.5
	3B	150ms	5
	3C	150ms	8.3
MAX6459UT_ -T	A	50µs	0.5
	B	50µs	5
	C	50µs	8.3
MAX6460UT-T	N/A	50µs	0.5

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PART	PIN COUNT	LATCHED OUTPUT	NUMBER OF OUTPUTS	HYSTERESIS ($\%V_{TH+}$)	TIMEOUT PERIOD	TOP MARK	COMPARATORS
MAX6457UKD0A-T	5	✓	1	0.5	50µs	AEAA	1
MAX6457UKD3A-T	5	✓	1	0.5	150ms	AANN	1
MAX6457UKD0B-T	5	✓	1	5	50µs	AANL	1
MAX6457UKD3B-T	5	✓	1	5	150ms	AANO	1
MAX6457UKD0C-T	5	✓	1	8.3	50µs	AANM	1
MAX6457UKD3C-T	5	✓	1	8.3	150ms	ADZZ	1
MAX6458UKD0A-T	5	—	1	0.5	50µs	AANP	2
MAX6458UKD3A-T	5	—	1	0.5	150ms	AANS	2
MAX6458UKD0B-T	5	—	1	5	50µs	AANQ	2
MAX6458UKD3B-T	5	—	1	5	150ms	AEAB	2
MAX6458UKD0C-T	5	—	1	8.3	50µs	AANR	2
MAX6458UKD3C-T	5	—	1	8.3	150ms	AANT	2
MAX6459UTA-T	6	—	2	0.5	50µs	ABML	2
MAX6459UTB-T	6	—	2	5	50µs	ABEJ	2
MAX6459UTC-T	6	—	2	8.3	50µs	ABMM	2
MAX6460UT-T	6	—	1	0.5	50µs	ABEG	1
MAX6459UTA/V-T	6	—	2	0.5	50µs	ACRY	2

$$R2 = \frac{V_{TH-} \times R_{TOTAL}}{V_{TRIPLOW}} - R3$$
$$= \frac{(1.167V)(4.2M\Omega)}{18.9V} - 223.273k\Omega$$
$$= 36.06k\Omega$$

4) Calculate R1

$$R1 = R_{TOTAL} - R2 - R3$$
$$= 4.2M\Omega - 223.273k\Omega - 36.06k\Omega$$
$$= 3.94067M\Omega$$

Monitoring Voltages Other than V_{CC}

The MAX6457–MAX6460 can monitor voltages other than V_{CC} (Figure 12). Calculate V_{TRIP} as shown in the *Programming the Trip Voltage (V_{TRIP})* section. The monitored voltage (V_{MON}) is independent of V_{CC}. V_{IN+} must be within the specified operating range: 0 to V_{CC}.

Interfacing to Voltages Other than V_{CC}

The open-drain outputs of the MAX6457–MAX6460 allow the output voltage to be selected independent of V_{CC}. For systems requiring an output voltage other than V_{CC}, connect the pullup resistor between OUT, OUTA, or OUTB and any desired voltage up to 28V (see Figure 13).

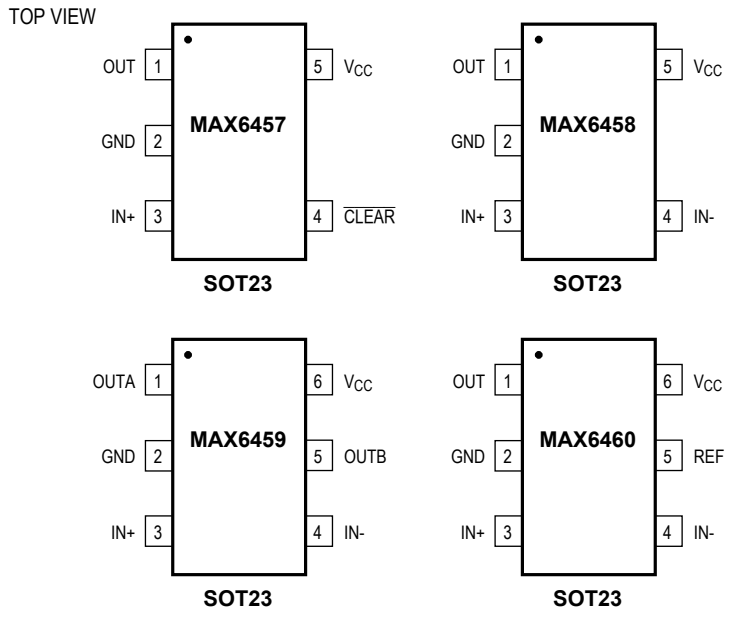
Monitoring Negative Voltages

Figure 14 shows the typical application circuit for monitoring negative voltages (V_{NEG}) using the MAX6460. Select a value for R1 between 25kΩ and 1MΩ. Use the following equation to select R2:

$$R2 = R1 \times \frac{-V_{NEG}}{V_{REF}}$$

where V_{REF} = 2.25V and V_{NEG} < 0. V_{IN+} must always be within the specified operating range: 0 to V_{CC}.

Pin Configurations



Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/02	Initial release	—
1	6/03	Updated the *Pin Description* and *Detailed Description* sections.	6, 8
2	12/05	Added lead-free notation to *Ordering Information*.	1
3	1/07	Updated the *Pin Description* and Figures 5a, 9, 12.	6, 8, 10, 11, 13-16
4	3/09	Updated the *Programming the Trip Voltage (V_{TRIP})* section.	8
5	7/12	Updated the *Package Information* table.	14
6	12/12	Added MAX6459UT_/V+ to *Ordering Information*	1
7	7/17	Added AEC-Q100 to Benefits and Features section and /V part to *Ordering Information* and *Selector Guide*	1, 12
8	1/19	Added *Package Information* section	2

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