Absolute Maximum Ratings

All Voltages Referenced to GND
V_{CC} ..... -0.3V to +6.0V
SRT, $\overline{MR}$, RESET IN ..... -0.3V to (V_{CC} + 0.3V)
RESET, $\overline{RESET}$ (Push-Pull) ..... -0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ (Open-Drain) ..... -0.3V to +6.0V
Input Current (All Pins) ..... ±20mA
Output Current ($\overline{RESET}$, RESET) ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
Lead(Pb)-free packages ..... +260°C
Packages containing lead (Pb) ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SOT23-5

PACKAGE CODE	U5+2/U5+2A
Outline Number	21-0057
Land Pattern Number	90-0174
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	324.3°C/W
Junction to Case (θ_{JC})	82°C/W
Thermal Resistance, Multi-Layer Board:	
Junction to Ambient (θ_{JA})	255.9°C/W
Junction to Case (θ_{JC})	81°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 1V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = 5V and T_A = +25°C.) (Note 1)

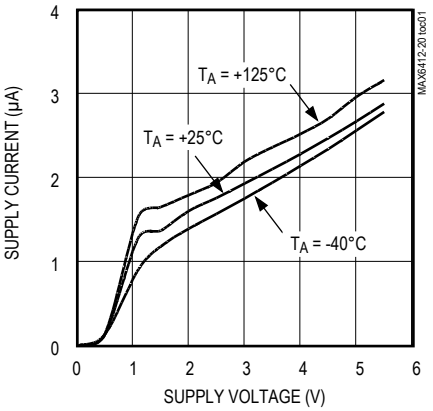
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		1.0		5.5	V
Supply Current	I_{CC}	V_{CC} ≤ 5.0V		2.6	4.5	µA
		V_{CC} ≤ 3.3V		2	3.5	
		V_{CC} ≤ 2.0V		1.7	2.5	
V_{CC} Reset Threshold Accuracy	V_{TH}	T_A = +25°C	V_{TH} - 1.25%		V_{TH} + 1.25%	V
		T_A = -40°C to +125°C	V_{TH} - 2.5%		V_{TH} + 2.5%	
Hysteresis	V_{HYST}			4 x V_{TH}		mV
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling at 1mV/µs		100		µs
Reset Timeout Period	t_{RP}	C_{SRT} = 1500pF	3.00	4.375	5.75	ms
		C_{SRT} = 0F		0.275		
V_{SRT} Ramp Current	I_{RAMP}	V_{SRT} = 0 to 0.65V; V_{CC} = 1.6V to 5V		240		nA
V_{SRT} Ramp Threshold	$V_{TH-RAMP}$	V_{CC} = 1.6V to 5V (V_{RAMP} rising)		0.65		V
RAMP Threshold Hysteresis		V_{RAMP} falling threshold		33		mV
$\overline{RESET}$ Output Voltage LOW	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50µA			0.3	V
		V_{CC} ≥ 2.7V, I_{SINK} = 1.2mA			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	
$\overline{RESET}$ Output Voltage HIGH, (Push-Pull)	V_{OH}	V_{CC} ≥ 1.8V, I_{SOURCE} = 200µA	0.8 x V_{CC}			V
		V_{CC} ≥ 2.25V, I_{SOURCE} = 500µA	0.8 x V_{CC}			
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{CC}			
$\overline{RESET}$ Output Leakage Current, (Open-Drain)	I_{LKG}	V_{CC} > V_{TH}, reset not asserted			1.0	µA
RESET Output Voltage HIGH	V_{OH}	V_{CC} ≥ 1.0V, I_{SOURCE} = 1µA	0.8 x V_{CC}			V
		V_{CC} ≥ 1.8V, I_{SOURCE} = 150µA	0.8 x V_{CC}			
		V_{CC} ≥ 2.7V, I_{SOURCE} = 500µA	0.8 x V_{CC}			
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{CC}			
RESET Output Voltage LOW	V_{OL}	V_{CC} ≥ 1.8V, I_{SINK} = 500µA			0.3	V
		V_{CC} ≥ 2.7V, I_{SINK} = 1.2mA			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	
RESET IN Leakage Current					10	nA
RESET IN Threshold	V_{RST}	V_{RST} falling, V_{CC} = 1.6V to 5.0V	1.205	1.255	1.305	V
$\overline{MR}$ Input	V_{IL}	V_{CC} > 4.0V			0.8	V
	V_{IH}		2.4			
	V_{IL}	V_{CC} < 4.0V			0.3 x V_{CC}	
	V_{IH}		0.7 x V_{CC}			
$\overline{MR}$ Minimum Pulse Width			1			µs
$\overline{MR}$ Glitch Rejection				75		ns
$\overline{MR}$ to RESET Delay				20		ns
$\overline{MR}$ Pullup Resistance		Pull up to V_{CC}	12	20	28	kΩ

Note 1: Devices production tested at T_A = +25°C. Over temperature limits are guaranteed by design.

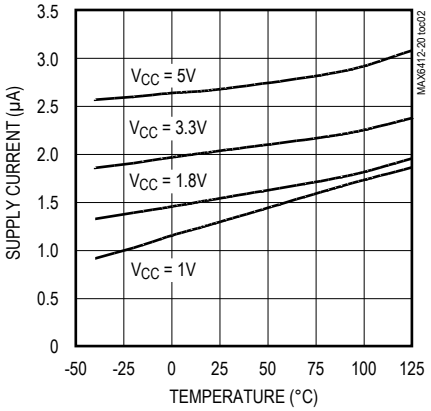
Typical Operating Characteristics

(V_{CC} = 5V, C_{SRT} = 1500pF, T_A = +25°C, unless otherwise noted.)

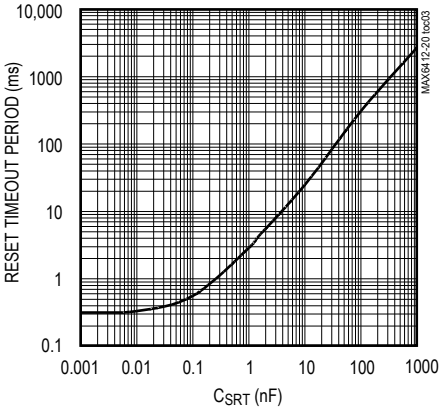
SUPPLY CURRENT vs. SUPPLY VOLTAGE



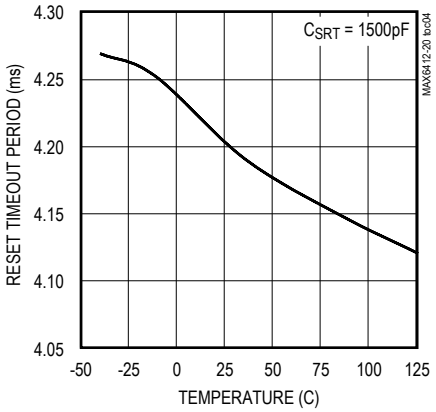
SUPPLY CURRENT vs. TEMPERATURE



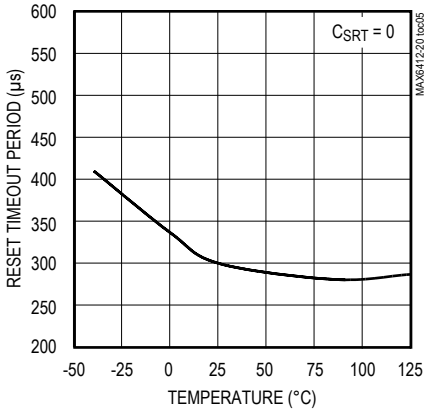
RESET TIMEOUT PERIOD vs. C_{SRT}



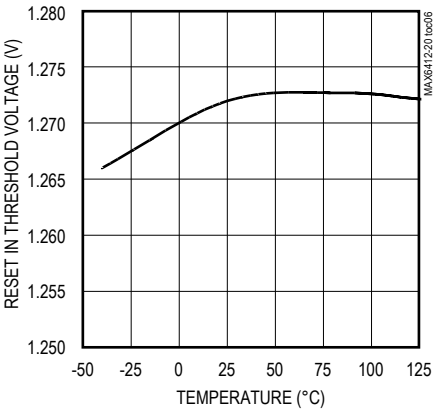
RESET TIMEOUT PERIOD vs. TEMPERATURE



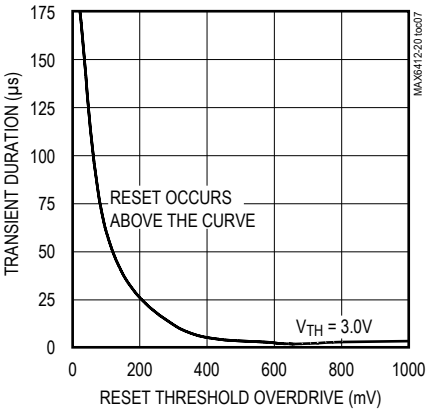
RESET TIMEOUT PERIOD vs. TEMPERATURE



RESET IN THRESHOLD VOLTAGE vs. TEMPERATURE



MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



Pin Description

PIN			NAME	FUNCTION
MAX6412/ MAX6413/ MAX6414	MAX6415/ MAX6416/ MAX6417	MAX6418/ MAX6419/ MAX6420		
1	1	1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ changes from high to low whenever V_{CC} or RESET IN drops below the selected reset threshold voltage (V_{TH} or $V_{RESET\ IN}$, respectively) or manual reset is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after all reset conditions are deasserted and then goes high.
			RESET	RESET changes from low to high whenever the V_{CC} or RESET IN drops below the selected reset threshold voltage (V_{TH} or $V_{RESET\ IN}$) or manual reset is pulled low. RESET remains high for the reset timeout period after all reset conditions are deasserted and then goes low.
2	2	2	GND	Ground
—	3	3	RESET IN	Reset Input. High-impedance input to the adjustable reset comparator. Connect RESET IN to the center point of an external resistor-divider network to set the threshold of the externally monitored voltage. See *Reset Threshold* section.
3	—	—	$\overline{\text{MR}}$	Manual Reset Input. Pull this pin low to manually reset the device. Reset remains asserted for the reset timeout period after $\overline{\text{MR}}$ is released.
4	4	4	SRT	Set Reset Timeout Input. Connect a capacitor between SRT and ground to set the timeout period. Determine the period as follows: $t_{RP} = (2.71 \times 10^6) \times C_{SRT} + 275\mu s$ with t_{RP} in seconds and C_{SRT} in Farads.
5	5	5	V_{CC}	Supply Voltage and Input for Fixed-Threshold V_{CC} Monitor

Detailed Description

The MAX6412–MAX6420 low-power microprocessor (µP) supervisory circuits provide maximum adjustability for supply-voltage monitoring and reset functionality. In addition, the MAX6412–MAX6420 reset timeout period is adjustable using an external capacitor.

The MAX6412/MAX6413/MAX6414 have factory-trimmed reset threshold voltages in approximately 100mV increments from 1.575V to 5.0V with a manual reset input. The MAX6415/MAX6416/MAX6417 contain a reset threshold that can be adjusted to any voltage above 1.26V using external resistors. The MAX6418/MAX6419/MAX6420 offer both a factory-trimmed reset threshold and an adjustable reset threshold input for dual-voltage monitoring.

A reset signal is asserted when V_{CC} and/or RESET IN falls below the preset values or when $\overline{\text{MR}}$ is asserted. The reset remains asserted for an externally programmed interval after V_{CC} and/or RESET IN has risen above the reset threshold or $\overline{\text{MR}}$ is deasserted.

Reset Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. The MAX6412–MAX6420 µP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see *Typical Operating Circuit*).

For the MAX6413, MAX6416, and MAX6419, RESET changes from low to high whenever V_{CC} or RESET IN drops below the reset threshold voltages. Once RESET IN and V_{CC} exceed their respective reset threshold voltage(s), RESET remains high for the reset timeout period, then goes low.

On power-up, once V_{CC} reaches 1V, RESET is guaranteed to be a logic high. For applications requiring valid reset logic when V_{CC} is less than 1V, see the section *Ensuring a Valid RESET/$\overline{\text{RESET}}$ Output Down to V_{CC} = 0V*.

The active-low $\overline{\text{RESET}}$ output of the remaining supervisors is the inverse of the MAX6413, MAX6416, and MAX6419 active-high RESET output and is guaranteed valid for $V_{CC} \geq 1V$.

Reset Threshold

The MAX6415–MAX6420 monitor the voltage on RESET IN with an external resistor voltage-divider (Figure 1).

Use the following formula to calculate the externally monitored voltage (V_{MON_TH}):

$$V_{MON\_TH} = V_{RST} \times (R1 + R2)/R2$$

where V_{MON_TH} is the desired reset threshold voltage and V_{RST} is the reset input threshold (1.26V). Resistors R1 and R2 can have very high values to minimize current consumption due to low leakage currents. Set R2 to some conveniently high value (1MΩ, for example) and calculate R1 based on the desired monitored voltage, using the following formula:

$$R1 = R2 \times (V_{MON\_TH}/V_{RST} - 1)\ (\Omega)$$

Manual Reset Input (MAX6412/MAX6413/MAX6414)

Many µP-based products require manual reset capability, allowing the operator, a technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low and for the reset timeout period after $\overline{MR}$ returns high.

The $\overline{MR}$ has an internal 20kΩ pullup resistor so it can be left open if not used. Connect a normally open momentary switch from $\overline{MR}$ to ground to create a manual reset function (external debounce circuitry is not required for long reset timeout periods).

A manual reset option can easily be implemented with the MAX6415–MAX6420 by connecting a normally open momentary switch in parallel with R2 (Figure 2). When the switch is closed, the voltage on RESET IN goes to zero, initiating a reset. Similar to the MAX6412/MAX6413/MAX6414 manual reset, reset remains asserted while the switch is closed and for the reset timeout period after the switch is opened.

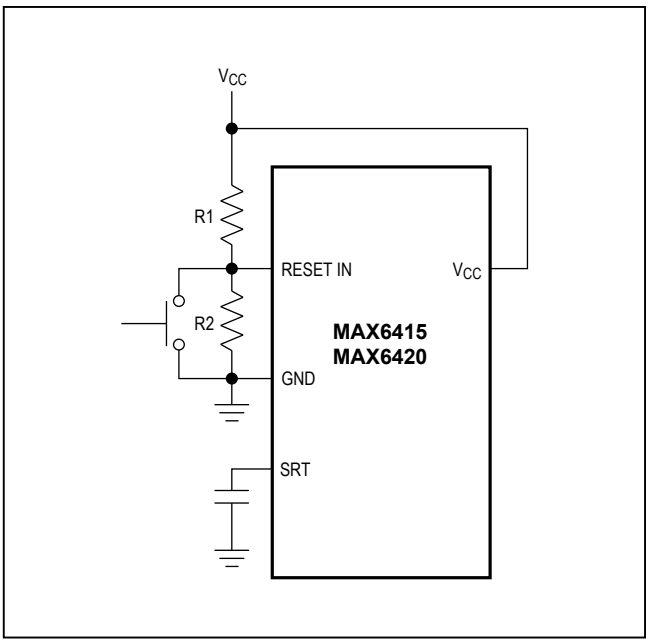


Figure 2. Adding an External Manual Reset Function to the MAX6415–MAX6420

Monitoring Voltages Other than V_{CC} (MAX6415/MAX6416/MAX6417)

The MAX6415/MAX6416/MAX6417 contain an adjustable reset threshold input. These devices can be used to monitor voltages other than V_{CC}. Calculate V_{MON_TH} as shown in the *Reset Threshold* section. (See Figure 3.)

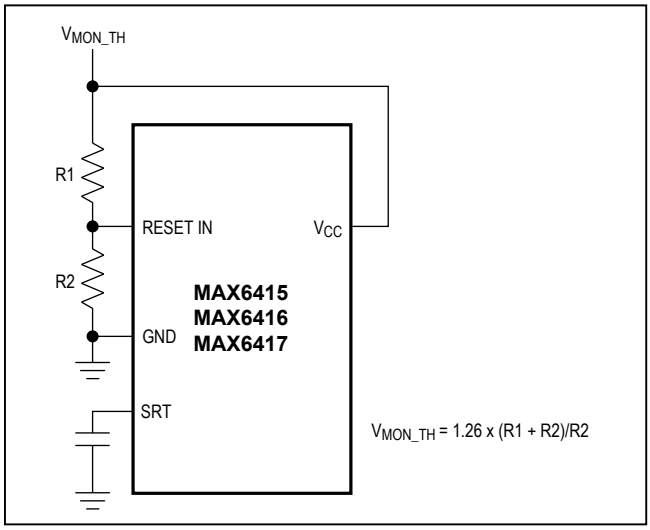


Figure 1. Calculating the Monitored Threshold Voltage (V_{MON_TH})

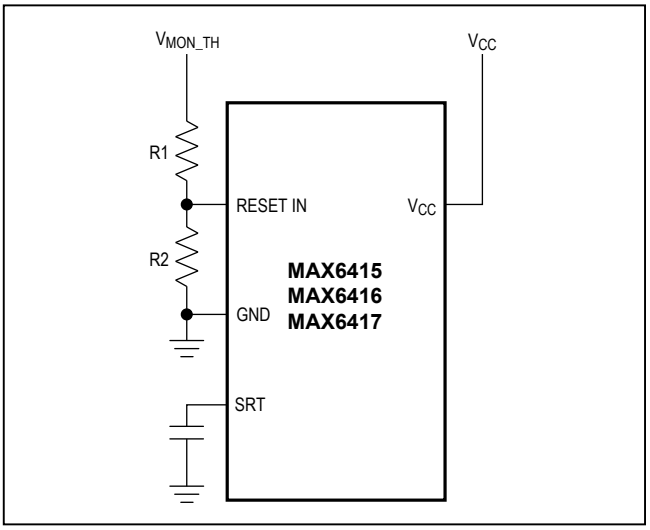


Figure 3. Monitoring External Voltages

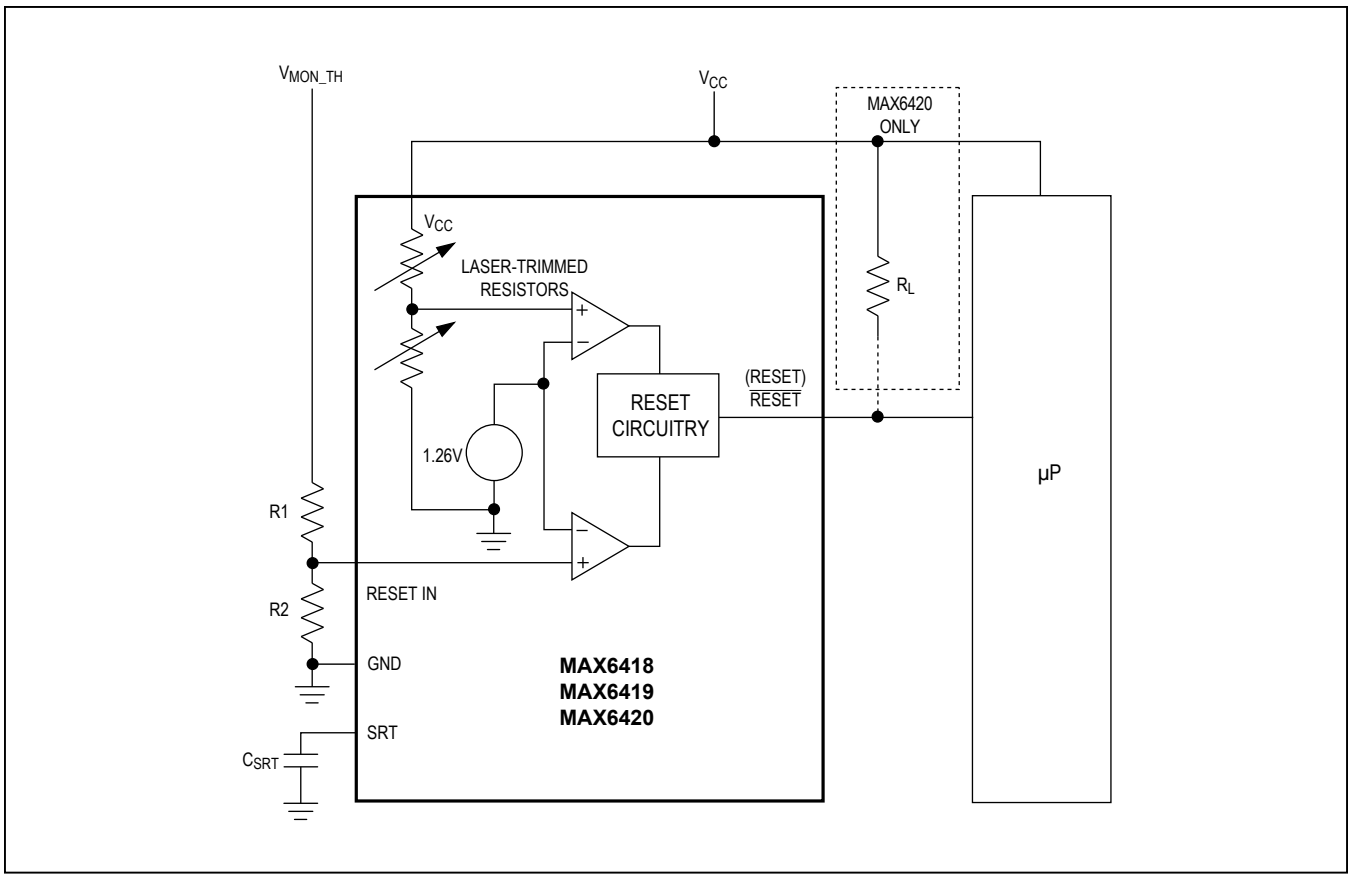


Figure 4. MAX6418/MAX6419/MAX6420 Monitoring Two Voltages

Dual-Voltage Monitoring (MAX6418/MAX6419/MAX6420)

The MAX6418/MAX6419/MAX6420 contain both factory-trimmed threshold voltages and an adjustable reset threshold input, allowing the monitoring of two voltages, V_{CC} and V_{MON_TH} (see Figure 4). Reset is asserted when either of the voltages falls below its respective threshold voltage.

Application Information

Selecting a Reset Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and ground. Calculate the reset timeout capacitor as follows:

$$C_{SRT} = (t_{RP} - 275\mu s) / (2.71 \times 10^6)$$

where t_{RP} is in seconds and C_{SRT} is in Farads

The reset delay time is set by a current/capacitor-controlled ramp compared to an internal 0.65V reference. An internal 240nA ramp current source charges the external capacitor. The charge to the capacitor is cleared when a reset condition is detected. Once the reset condition is removed, the voltage on the capacitor ramps according to the formula: dV/dt = I/C. The C_{SRT} capacitor must ramp to 0.65V to deassert the reset. C_{SRT} must be a low-leakage (<10nA) type capacitor, ceramic is recommended.

Operating as a Voltage Detector

The MAX6412–MAX6420 can be operated in a voltage detector mode by leaving SRT unconnected. The reset delay times for V_{CC} rising above or falling below the threshold are not significantly different. The reset output is deasserted smoothly without false pulses.

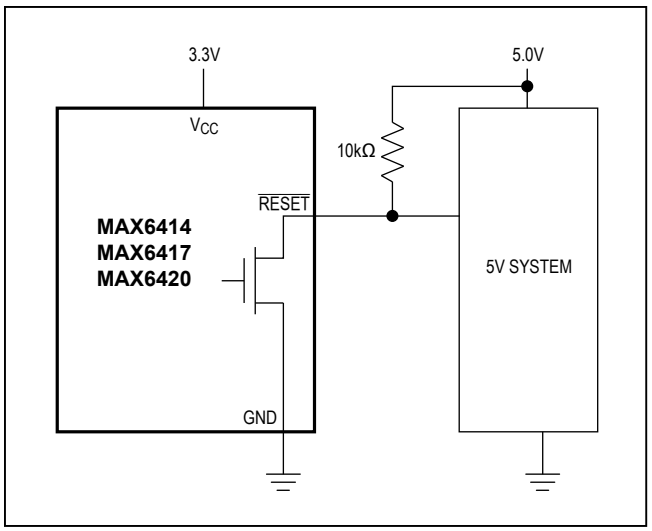


Figure 5. MAX6414/MAX6417/MAX6420 Open-Drain $\overline{RESET}$ Output Allows use with Multiple Supplies

Interfacing to Other Voltages for Logic Compatibility

The open-drain outputs of the MAX6414/MAX6417/MAX6420 can be used to interface to µPs with other logic levels. As shown in Figure 5, the open-drain output can be connected to voltages from 0 to 5.5V. This allows for easy logic compatibility to various microprocessors.

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going transients (glitches). The Maximum Transient Duration vs. Reset Threshold Overdrive graph in the *Typical Operating Characteristics* shows this relationship.

The area below the curve of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{CC}, starting above the actual reset threshold (V_{TH}) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient decreases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50µs or less will not cause a reset pulse to be issued.

Ensuring a Valid $\overline{RESET}$ or RESET Down to V_{CC} = 0V

When V_{CC} falls below 1V, $\overline{RESET}$/RESET current sinking (sourcing) capabilities decline drastically. In the case of the MAX6412, MAX6415, and MAX6418, high-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problems in most applications, since most µPs and other circuitry do not operate with V_{CC} below 1V.

In those applications where $\overline{RESET}$ must be valid down to 0, adding a pulldown resistor between $\overline{RESET}$ and ground sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 6). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. For applications using the MAX6413, MAX6416, and MAX6419, a 100kΩ pullup resistor between RESET and V_{CC} will hold RESET high when V_{CC} falls below 1V (Figure 7). Open-drain $\overline{RESET}$ versions are not recommended for applications requiring valid logic for V_{CC} down to 0V.

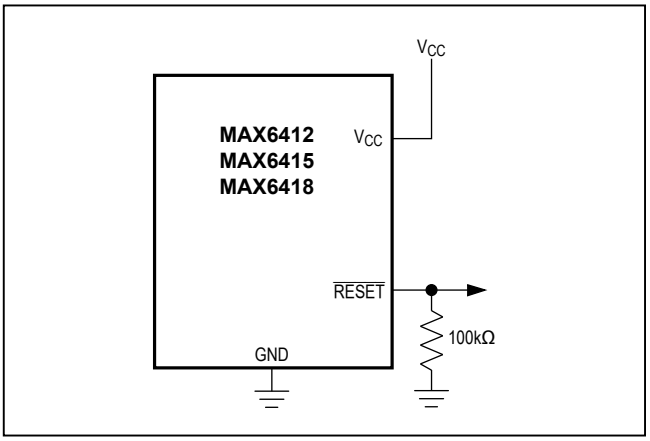


Figure 6. Ensuring $\overline{RESET}$ Valid to V_{CC} = 0V

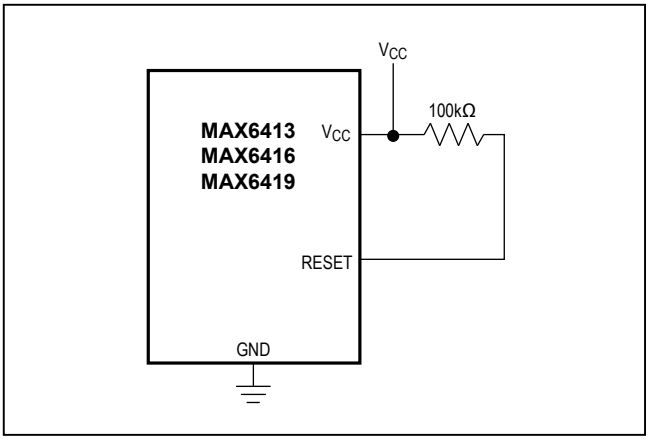


Figure 7. Ensuring RESET Valid to V_{CC} = 0V

Layout Consideration

SRT is a precise current source. When developing the layout for the application, be careful to minimize board capacitance and leakage currents around this pin. Traces connected to SRT should be kept as short as possible. Traces carrying high-speed digital signals and traces with large voltage potentials should be routed as far from SRT as possible. Leakage current and stray capacitance (e.g., a scope probe) at this pin could cause errors in the reset timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset periods.

RESET IN is a high-impedance input, which is typically driven by a high-impedance resistor-divider network (e.g., 1MΩ to 10MΩ). Minimize coupling to transient signals by keeping the connections to this input short. Any DC leakage current at RESET IN (e.g., a scope probe) causes errors in the programmed reset threshold.

Chip Information

TRANSISTOR COUNT: 329

PROCESS: BiCMOS

Table 1. Reset Voltages Suffix Table

SUFFIX	MIN	TYP	MAX
16	1.536	1.575	1.614
17	1.623	1.665	1.707
18	1.755	1.800	1.845
19	1.853	1.900	1.948
20	1.950	2.000	2.050
21	2.048	2.100	2.153
22	2.133	2.188	2.243
23	2.313	2.313	2.371
24	2.340	2.400	2.460
25	2.438	2.500	2.563
26	2.559	2.625	2.691
27	2.633	2.700	2.768
28	2.730	2.800	2.870
29	2.852	2.925	2.998
30	2.925	3.000	3.075
31	2.998	3.075	3.152
32	3.120	3.200	3.280
33	3.218	3.300	3.383
34	3.315	3.400	3.485
35	3.413	3.500	3.558
36	3.510	3.600	3.690
37	3.608	3.700	3.793
38	3.705	3.800	3.895
39	3.803	3.900	3.998
40	3.900	4.000	4.100
41	3.998	4.100	4.203
42	4.095	4.200	4.305
43	4.193	4.300	4.408
44	4.266	4.375	4.484
45	4.388	4.500	4.613
46	4.509	4.625	4.741
47	4.583	4.700	4.818
48	4.680	4.800	4.920
49	4.778	4.900	5.023
50	4.875	5.000	5.125

Standard Versions Table

PART*
MAX6412UK16-T
MAX6412UK22-T
MAX6412UK26-T
MAX6412UK29-T
MAX6412UK46-T
MAX6413UK16-T
MAX6413UK22-T
MAX6413UK26-T
MAX6413UK29-T
MAX6413UK46-T
MAX6414UK16-T
MAX6414UK22-T
MAX6414UK26-T
MAX6414UK29-T
MAX6414UK46-T
MAX6415UK-T
MAX6416UK-T
MAX6417UK-T
MAX6418UK16-T
MAX6418UK22-T
MAX6418UK26-T
MAX6418UK29-T
MAX6418UK46-T
MAX6419UK16-T
MAX6419UK22-T
MAX6419UK26-T
MAX6419UK29-T
MAX6419UK46-T
MAX6420UK16-T
MAX6420UK22-T
MAX6420UK26-T
MAX6420UK29-T
MAX6420UK46-T

**Sample Stock is generally held on all standard versions. Contact factory for availability of nonstandard versions.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6412UK_ _-T	-40°C to +125°C	5 SOT23
MAX6412UK_ _+T	-40°C to +125°C	5 SOT23
MAX6413UK_ _-T	-40°C to +125°C	5 SOT23
MAX6413UK_ _+T	-40°C to +125°C	5 SOT23
MAX6414UK_ _-T	-40°C to +125°C	5 SOT23
MAX6414UK_ _+T	-40°C to +125°C	5 SOT23
MAX6414UK_ _/V+T*	-40°C to +125°C	5 SOT23
MAX6414UK29/V+T	-40°C to +125°C	5 SOT23
MAX6414UK31/V+T	-40°C to +125°C	5 SOT23
MAX6414UK175/V+T	-40°C to +125°C	5 SOT23
MAX6415UK+T	-40°C to +125°C	5 SOT23
MAX6416UK+T	-40°C to +125°C	5 SOT23
MAX6417UK+T	-40°C to +125°C	5 SOT23
MAX6418UK_ _-T	-40°C to +125°C	5 SOT23
MAX6418UK_ _+T	-40°C to +125°C	5 SOT23
MAX6419UK_ _-T	-40°C to +125°C	5 SOT23
MAX6419UK_ _+T	-40°C to +125°C	5 SOT23
MAX6420UK_ _-T	-40°C to +125°C	5 SOT23
MAX6420UK_ _+T	-40°C to +125°C	5 SOT23
MAX6420UK_ _/V-T*	-40°C to +125°C	5 SOT23

Note: *The MAX6412/MAX6413/MAX6414 and MAX6418/MAX6419/MAX6420 are available with factory-set V_{CC} reset thresholds from 1.575V to 5.0V in approximately 0.1V increments. Insert the desired nominal reset threshold suffix (from Table 1) into the blanks following the letters UK. There are 33 standard versions with a required order increment of 2500 pieces. Sample stock is generally held on standard versions only (see Standard Versions Table). Required order increment is 10,000 pieces for nonstandard versions. Contact factory for availability. All devices are available in tape-and-reel only.*

Devices are available in both leaded (-) and lead-free (+) packaging. /V denotes an automotive qualified part.

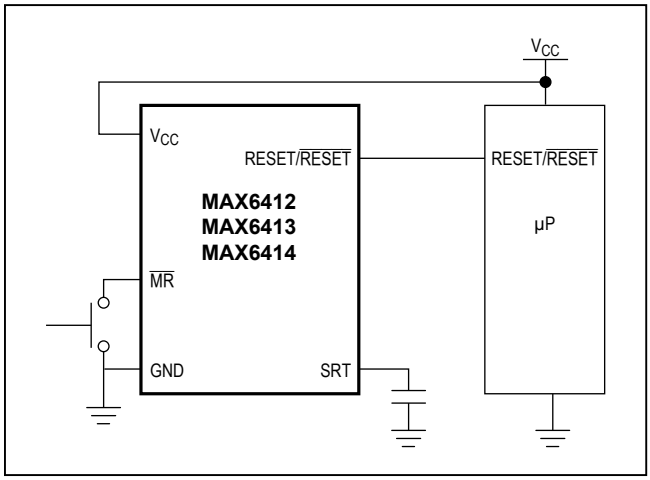
For top mark information, please visit Maxim's website at **www.maximintegrated.com**.

**Future product—contact factory for availability.*

Selector Guide

PART	FIXED V_{TH}	MANUAL RESET	RESET IN	PUSH-PULL $\overline{\text{RESET}}$	PUSH-PULL RESET	OPEN-DRAIN $\overline{\text{RESET}}$
MAX6412	✓	✓	—	✓	—	—
MAX6413	✓	✓	—	—	✓	—
MAX6414	✓	✓	—	—	—	✓
MAX6415	—	—	✓	✓	—	—
MAX6416	—	—	✓	—	✓	—
MAX6417	—	—	✓	—	—	✓
MAX6418	✓	—	✓	✓	—	—
MAX6419	✓	—	✓	—	✓	—
MAX6420	✓	—	✓	—	—	✓

Typical Operating Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	01/02	Initial release	—
1	8/03	Corrected top marks	10
2	12/05	Added lead-free information in *Ordering Information*	1
3	3/10	Deleted RESET in Hysteresis parameter in the *Electrical Characteristics* table	3
4	2/11	Corrected formula for SRT	5, 7
5	8/12	Added automotive qualified part to *Ordering Information*	1
6	3/14	Added MAX6414UK_ _/V+T to *Ordering Information*	1
7	12/15	Added lead-free part numbers to Ordering Information table, updated package code and removed top mark information from page 10.	1, 10
8	3/18	Updated *Benefits and Features* and *Ordering Information* tables	1, 10
9	12/18	Added *Package Information*	2
10	2/19	Updated Transistor Count	9
11	7/19	Updated *Electrical Characteristics*	3

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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