ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
All other pins to GND (Note 1).....-0.3V to V_{CC} + 0.3V
Continuous Current
NO_, NC_, COM_ .....±100mA
Peak Current NO_, NC_, COM_
(pulsed at 1ms, 50% Duty Cycle).....±200mA
(pulsed at 1ms, 10% Duty Cycle).....±300mA
Continuous Power Dissipation (T_A = +70°C)
25-Bump UCSP (derate 12.2mW/°C above +70°C) 976mW
24-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C
Lead Temperature (soldering).....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Signals on CB_, NO_, NC_, COM_, $\overline{EN}$ exceeding V_{CC} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V_{CC}		T_{MIN} to T_{MAX}	1.8		5.5	V
Power-Supply Current	I_{CC}	V_{CC} = 5.5V, $V_{CB\_}$ = 0V or V_{CC}	T_{MIN} to T_{MAX}			1.0	µA
		V_{CC} = 2.7V, $V_{CB\_}$ = 1.6V or 0.5V				5	
		V_{CC} = 5.5V, $V_{CB\_}$ = 1.6V or 0.5V				10	
ANALOG SWITCH							
Analog Signal Range	$V_{NO\_}$, $V_{NC\_}$, $V_{COM\_}$,		T_{MIN} to T_{MAX}	0		V_{CC}	V
On-Resistance (Note 4)	R_{ON}	V_{CC} = 2.7V, $I_{COM\_}$ = 10mA; $V_{NC\_}$ or $V_{NO\_}$ = 0 or V_{CC}	+25°C		4.0	5.5	Ω
			T_{MIN} to T_{MAX}			6.5	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V_{CC} = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 0 or V_{CC}	+25°C		0.3	0.5	Ω
			T_{MIN} to T_{MAX}			0.6	
On-Resistance Flatness (Notes 4, 6)	R_{FLAT}	V_{CC} = 2.7V, $I_{COM\_}$ = 10mA; $V_{NC\_}$ or $V_{NO\_}$ = 0 or V_{CC}	+25°C		0.5	1	Ω
			T_{MIN} to T_{MAX}			1.2	
NO_ or NC_ Off-Leakage Current	$I_{NO\_(OFF)}$ or $I_{NC\_(OFF)}$	V_{CC} = 3.6V; $V_{COM\_}$ = 3.6V, 0; $V_{NO\_}$ or $V_{NC\_}$ = 0, 3.6V	+25°C	-3		+3	nA
			T_{MIN} to T_{MAX}	-10		+10	
COM_ On-Leakage Current	$I_{NO\_(ON)}$	V_{CC} = 3.6V; $V_{COM\_}$ = 3.6V, 0; $V_{NO\_}$ or $V_{NC\_}$ = 3.6V, 0 or unconnected	+25°C	-6		+6	nA
			T_{MIN} to T_{MAX}	-10		+10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V_{CC} = 3.6V (MAX4948); $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0, 3V, 3.3V	+25°C	-6		+6	nA
			T_{MIN} to T_{MAX}	-10		+10	
DYNAMIC							
Turn-On Time	t_{ON}	V_{CC} = 2.7V; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 1	+25°C		400	800	ns
			T_{MIN} to T_{MAX}			800	
Turn-Off Time	t_{OFF}	V_{CC} = 2.7V; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 1	+25°C		300	800	ns
			T_{MIN} to T_{MAX}			800	
Break-Before-Make	t_{BBM}	V_{CC} = 2.7V; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 2 (Note 7)	+25°C		100		ns
			T_{MIN} to T_{MAX}	2			
HIGH-SPEED TIMING CHARACTERISTICS (rising time = 20ns)							
Skew	t_{SKEW}	V_{CC} = 2.7V; R_S = 39Ω; C_L = 50pF, Figure 3	T_{MIN} to T_{MAX}		0.2		ns
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1nF , Figure 4	+25°C		10		pC
-3dB Bandwidth	BW	Signal = 0dBm, C_L = 5pF, R_L = 50Ω, Figure 5	+25°C		300		MHz
Off-Isolation	V_{ISO}	C_L = 5pF; R_L = 50Ω; $V_{COM\_}$ = $1V_{P-P}$, f = 1MHz, Figure 5 (Note 8)	+25°C		-70		dB
Crosstalk	V_{CT}	C_L = 5pF; R_L = 50Ω; f = 1MHz, $V_{COM\_}$ = $1V_{P-P}$, Figure 5 (Note 9)	+25°C		-90		dB
NC_ or NO_ Off-Capacitance	$C_{NC\_(OFF)}$ $C_{NO\_(OFF)}$	NC_ = NO_ = 0V, f = 1MHz Figure 6	+25°C		15		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	V_{COM} = GND, f = 1MHz (MAX4948), Figure 6	+25°C		25		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	COM_ = 0V, f = 1MHz, Figure 6	+25°C		30		pF
DIGITAL I/O ($\overline{EN}$, CB_)							
Input-Logic High	V_{IH}		T_{MIN} to T_{MAX}	1.6			V
Input-Logic Low	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	I_{CB}	$V_{CB\_}$ = 0 or V_{CC}	T_{MIN} to T_{MAX}			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, T_A = +25°C.) (Notes 2, 3)

Note 2: The algebraic convention is used. The most negative value is shown in the minimum column.

Note 3: UCSP parts are 100% tested at T_A = +25°C. Limits across the full temperature range are guaranteed by correlation and design. TQFN parts are guaranteed by correlation and design at T_A = --40°C.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design, not production tested.

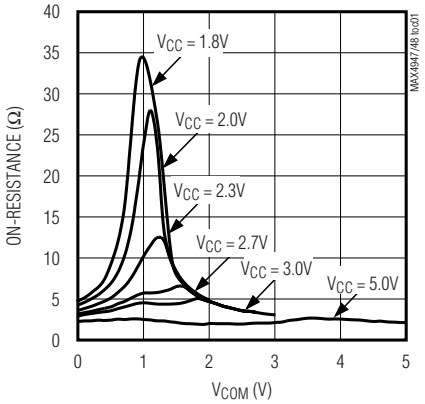
Note 8: Off-Isolation = $20\log_{10}$ [$V_{COM\_}$ / ($V_{NO\_}$ or $V_{NC\_}$)], $V_{COM\_}$ = output, $V_{NO\_}$ or $V_{NC\_}$ = input to off switch.

Note 9: Between any two switches.

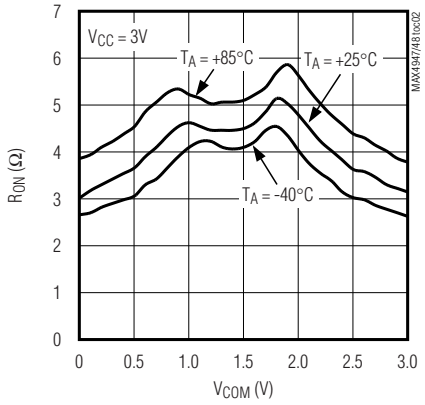
Typical Operating Characteristics

(V_{CC} = 3V, T_A = +25°C, unless otherwise noted.)

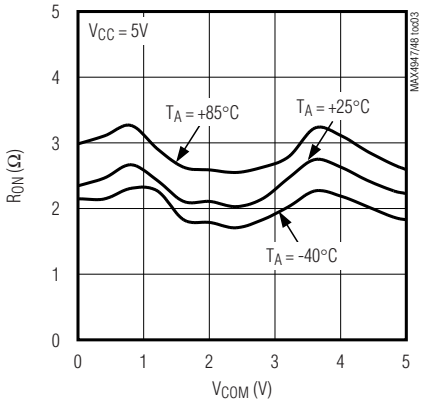
ON-RESISTANCE vs. V_{COM}



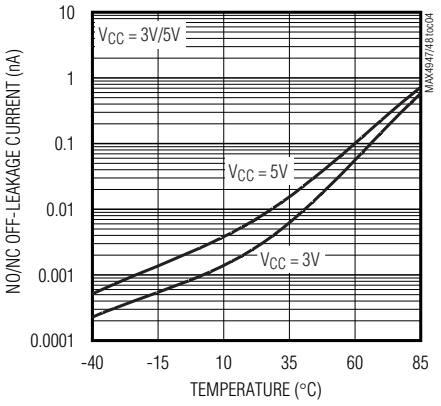
ON-RESISTANCE vs. V_{COM} TEMPERATURE



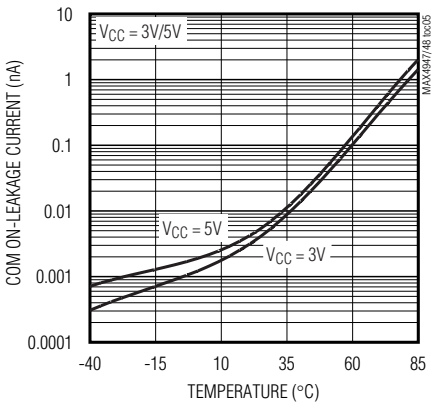
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



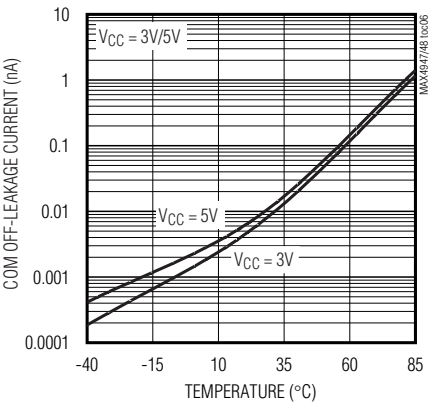
NO/NC OFF-LEAKAGE CURRENT vs. TEMPERATURE



COM ON-LEAKAGE CURRENT vs. TEMPERATURE



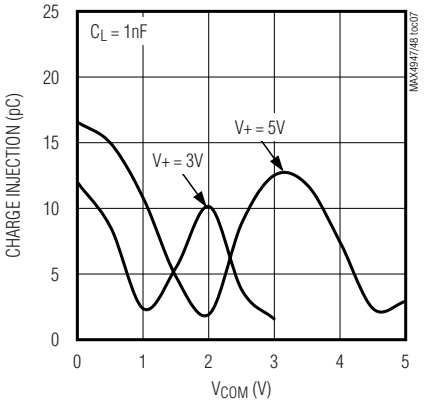
COM OFF-LEAKAGE CURRENT vs. TEMPERATURE (MAX4748)



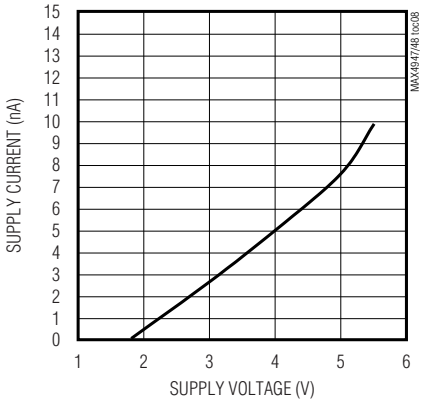
Operating Characteristics (continued)

(V_{CC} = +3V, T_A = +25°C, unless otherwise noted.)

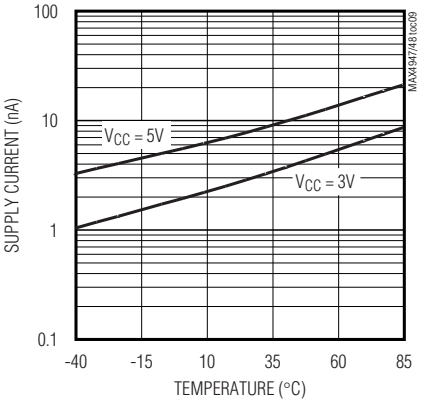
CHARGE INJECTION vs. V_{COM}



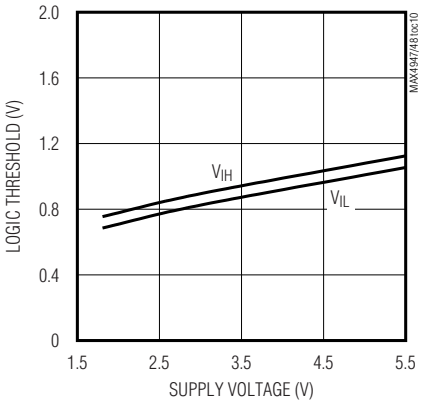
SUPPLY CURRENT vs. SUPPLY VOLTAGE



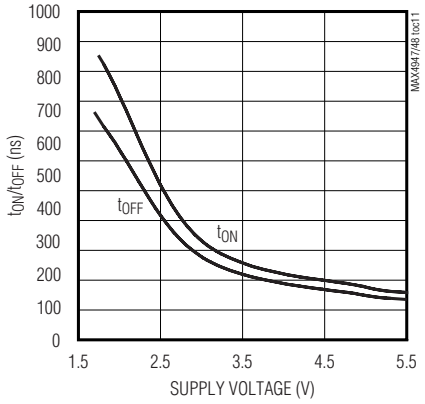
SUPPLY CURRENT vs. TEMPERATURE



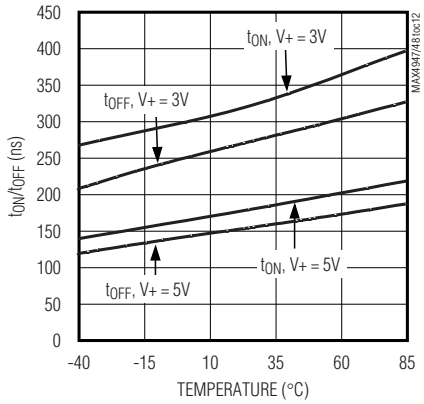
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



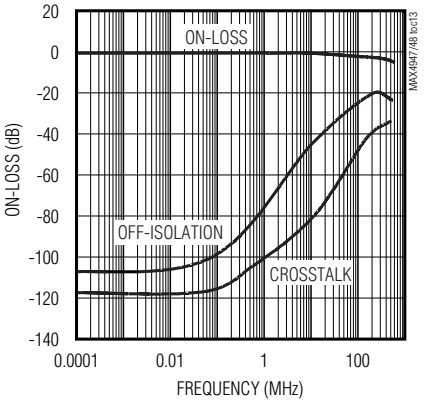
TURN-ON/-OFF TIME vs. SUPPLY VOLTAGE



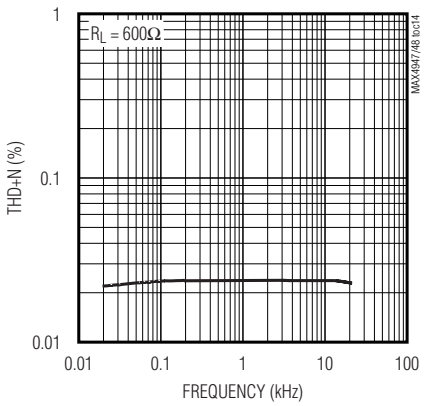
TURN-ON/-OFF TIMES vs. TEMPERATURE



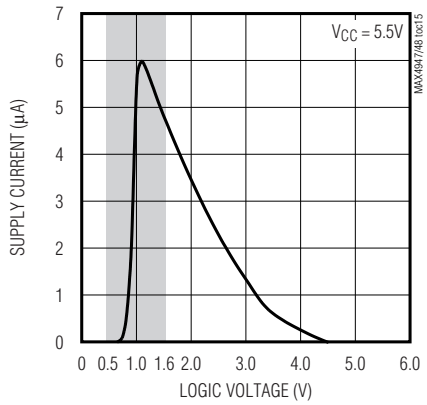
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



SUPPLY CURRENT vs. LOGIC VOLTAGE

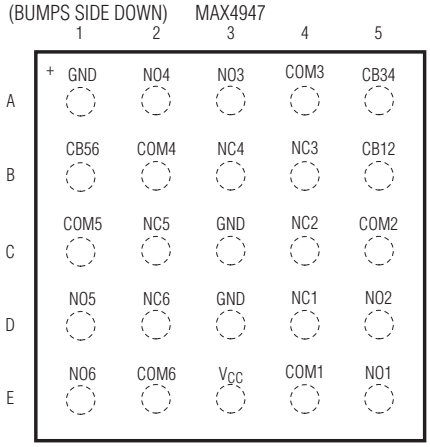


Pin Description

PIN				NAME	FUNCTION
MAX4947		MAX4948			
TQFN	UCSP	TQFN	UCSP		
1	D2	1	D2	NC6	Analog Switch 6. Normally Closed Terminal 6.
2	D1	2	D1	NO5	Analog Switch 5. Normally Open Terminal 5.
3	C1	3	C1	COM5	Analog Switch 5. Common Terminal 5.
4	C2	4	C2	NC5	Analog Switch 5. Normally Closed Terminal 5.
5	B1	—	—	CB56	Digital Control Input for Analog Switches 5 and 6
6, 21	A1, C3, D3	6, 21	A1, C3, D3	GND	Ground
7	B2	7	B2	COM4	Analog Switch 4. Common Terminal 4.
8	A2	8	A2	NO4	Analog Switch 4. Normally Open Terminal 4.
9	B3	9	B3	NC4	Analog Switch 4. Normally Closed Terminal 4.
10	A3	10	A3	NO3	Analog Switch 3. Normally Open Terminal 3.
11	A4	11	A4	COM3	Analog Switch 3. Common Terminal 3.
12	B4	12	B4	NC3	Analog Switch 3. Normally Closed Terminal 3.
13	A5	—	—	CB34	Digital Control Input for Analog Switches 3 and 4
14	B5	—	—	CB12	Digital Control Input for Analog Switches 1 and 2
15	C4	15	C4	NC2	Analog Switch 2. Normally Closed Terminal 2.
16	C5	16	C5	COM2	Analog Switch 2. Common Terminal 2.
17	D5	17	D5	NO2	Analog Switch 2. Normally Open Terminal 2.
18	D4	18	D4	NC1	Analog Switch 1. Normally Closed Terminal 1.
19	E5	19	E5	NO1	Analog Switch 1. Normally Open Terminal 1.
20	E4	20	E4	COM1	Analog Switch 1. Common Terminal 2.
22	E3	22	E3	V_{CC}	Positive Supply Voltage
23	E2	23	E2	COM6	Analog Switch 6. Common Terminal 6.
24	E1	24	E1	NO6	Analog Switch 6. Normally Open Terminal 6.
—	—	5	B1	$\overline{EN}$	Enable-Logic In. Drive $\overline{EN}$ high to set all switches into high-impedance mode.
—	—	13	A5	N.C.	No Connection. Leave N.C. unconnected.
—	—	14	B5	CB	Digital Control Input for Analog Switches 1–6. Drive CB low to connect COM_ to NC_ for all six switches. Drive CB high to connect COM_ to NO_ for all six switches. CB is valid only when $\overline{EN}$ is driven low. If $\overline{EN}$ is driven high then all switches are high impedance.
EP	—	EP	—	EP	Exposed Pad. Connect exposed pad to ground.

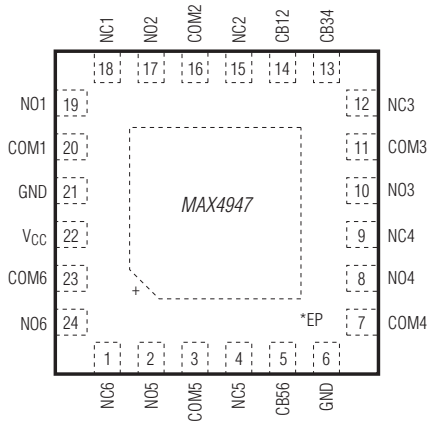
Pin Configurations/Truth Tables

(BUMPS SIDE DOWN) MAX4947



UCSP 2.5mm x 2.5mm

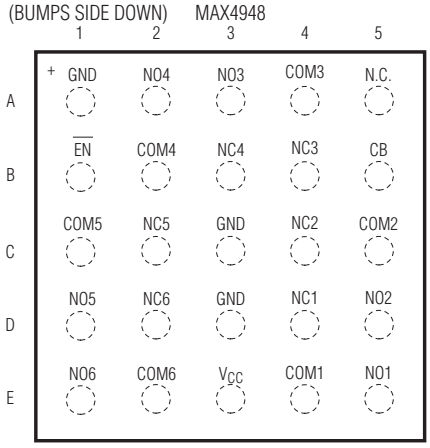
TOP VIEW



TQFN 4mm x 4mm

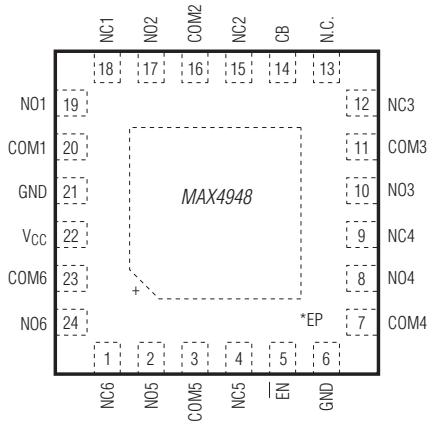
*EXPOSED PADDLE CONNECT TO GROUND

(BUMPS SIDE DOWN) MAX4948



UCSP 2.5mm x 2.5mm

TOP VIEW



TQFN 4mm x 4mm

*EXPOSED PADDLE-CONNECT TO GROUND

MAX4947		
CB12	**NO1/NO2**	**NC1/INC2**
0	OFF	ON
1	ON	OFF
CB34	**NO3/NO4**	**NC3/NC4**
0	OFF	ON
1	ON	OFF
CB56	**NO5/NO6**	**NC5/NC6**
0	OFF	ON
1	ON	OFF

MAX4948			
$\overline{EN}$	**CB**	**NO_**	**NC_**
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF

Detailed Description

The MAX4947 triple DPDT and the MAX4948 hex SPDT analog switches operate from a single +1.8V to +5.5V supply. These devices are fully specified for +3V applications.

The MAX4947/MAX4948 have a guaranteed 4Ω (typ) on-resistance and a low 30pF (typ) capacitance that makes the switch ideal for data switching applications. The MAX4947 has three logic inputs to control two switches in pairs and the MAX4948 has one logic control input and an enable input ($\overline{EN}$) to disable the switches.

Applications Information

Digital Control Inputs

The MAX4947/MAX4948 provide a digital control logic input, CB_. CB_ controls the position of the switches as shown in the *Pin Configurations/Truth Tables*. Driving CB_ rail-to-rail minimizes power consumption.

The MAX4948 features an $\overline{EN}$ input to turn all switches on or off. When $\overline{EN}$ is driven high, CB is disabled, and the analog inputs enter a high-impedance state. Drive $\overline{EN}$ low to turn the switches on and enable CB.

Analog Signal Levels

The on-resistance of the MAX4947/MAX4948 is very low and stable as the analog input signals are swept from ground to V_{CC} (see the *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs.

Power-Supply Biasing

Power-supply bypassing improves noise margin and prevents switching noise to propagate from V_{CC} supply to other components. A 0.1µF capacitor connected from V+ to GND is adequate for most applications.

Power-Supply Sequencing

CMOS devices require proper power-supply sequencing. Always apply V_{CC} before the analog signals, especially if the input signal is not current limited.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to the Maxim website at www.maxim-ic.com/ucsp for the Application Note: *UCSP-A Wafer-Level Chip-Scale Package.*

Timing Circuits/Timing Diagrams

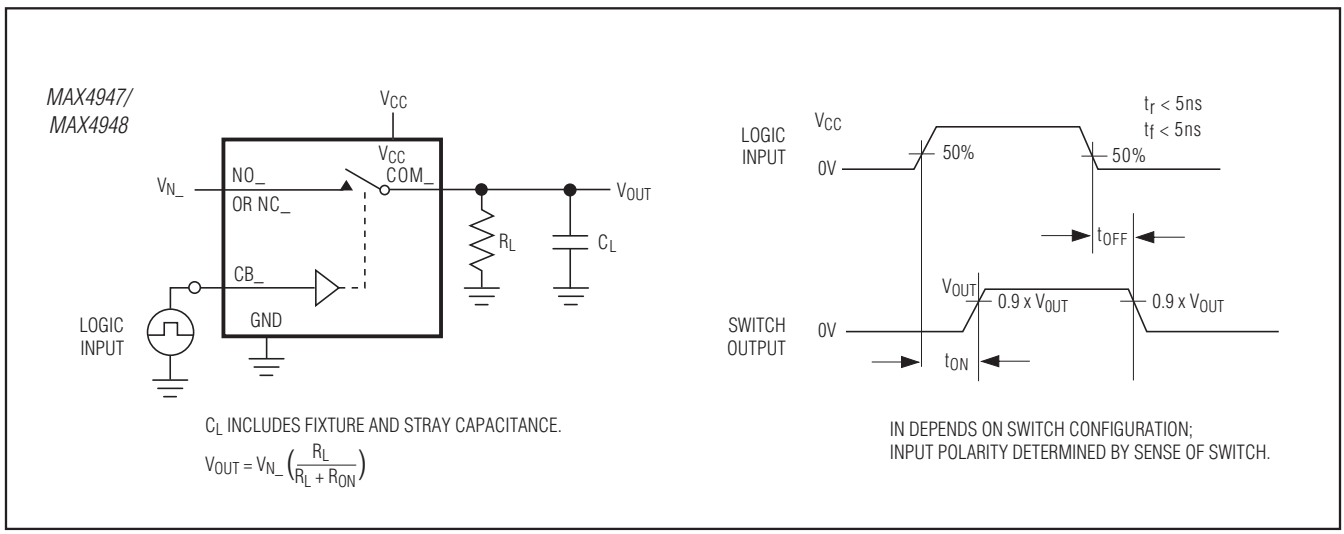


Figure 1. Switching Time

Timing Circuits/Timing Diagrams (continued)

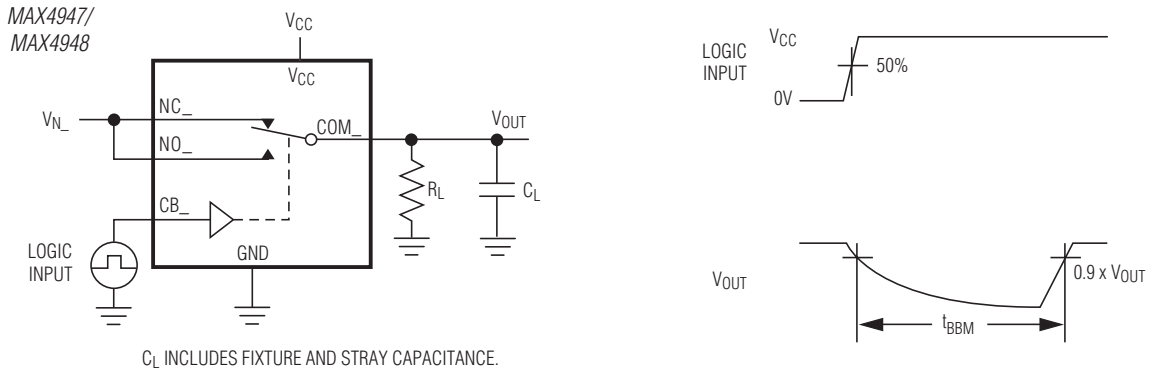
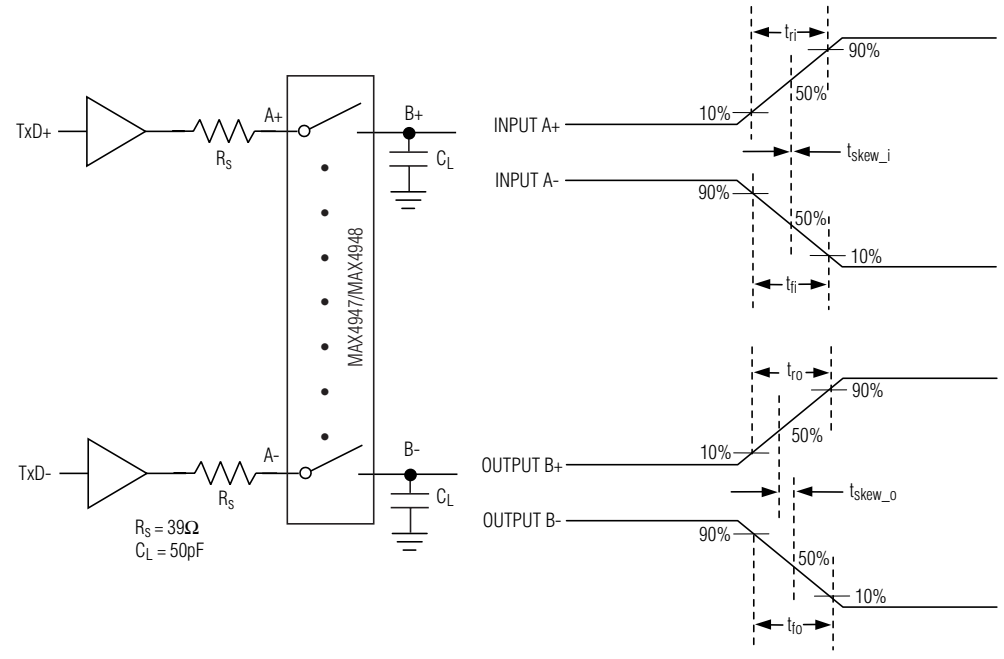


Figure 2. Break-Before-Make-Interval



|tro - tri| DELAY DUE TO SWITCH FOR RISING INPUT AND RISING OUTPUT SIGNALS.

|tfo - tfi| DELAY DUE TO SWITCH FOR FALLING INPUT AND FALLING OUTPUT SIGNALS.

|tskew_o| CHANGE IN SKEW THROUGH THE SWITCH FOR OUTPUT SIGNALS.

|tskew_i| CHANGE IN SKEW THROUGH THE SWITCH FOR INPUT SIGNALS.

Figure 3. Input/Output Skew Timing Diagram

Timing Circuits/Timing Diagrams (continued)

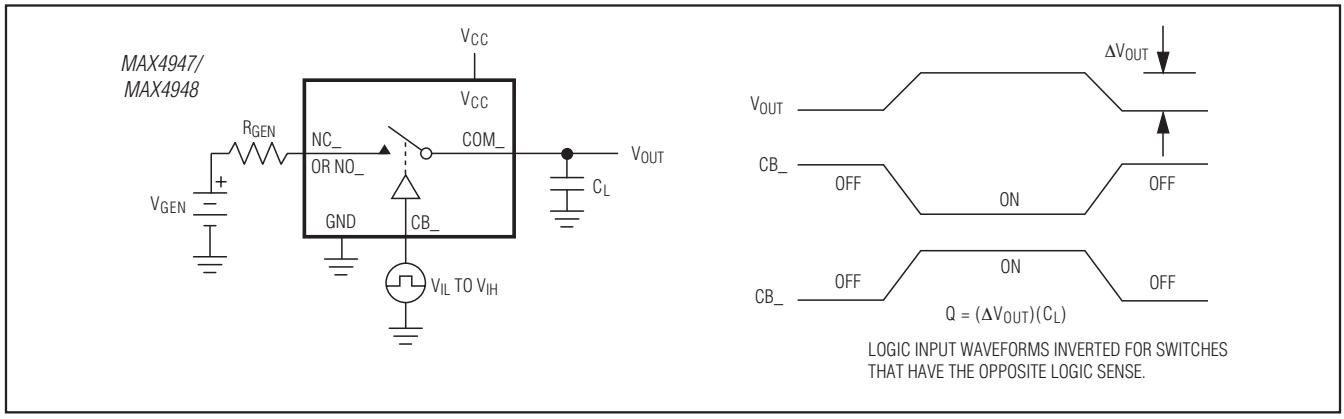


Figure 4. Charge Injection

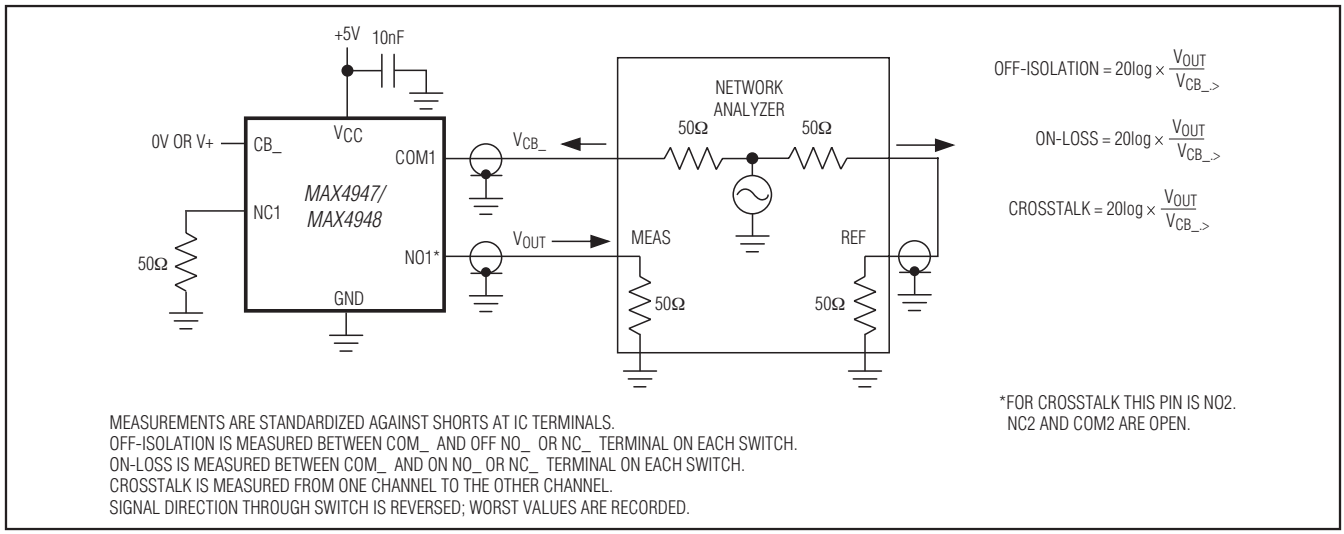


Figure 5. On-Loss, Off-Isolation, and Crosstalk

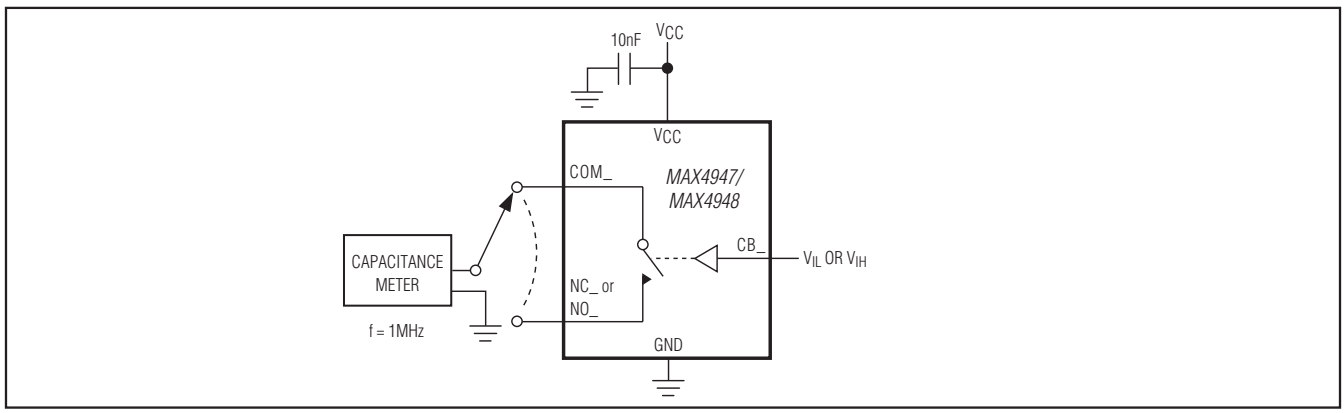
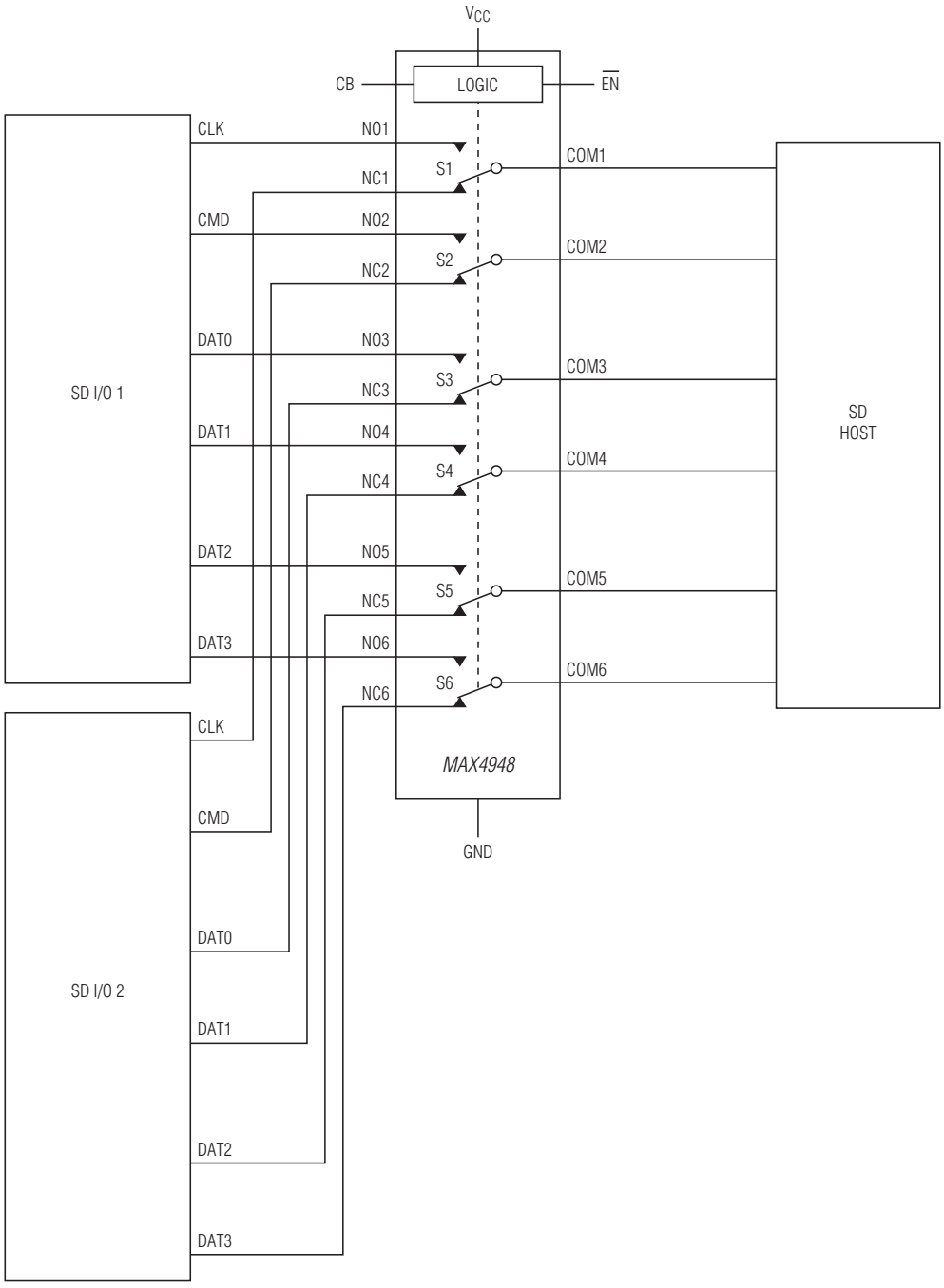


Figure 6. On-Loss, Off-Isolation, and Crosstalk

Typical Operating Circuit



Chip Information

PROCESS: CMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4947ERA+*	-40°C to +85°C	25 UCSP-25
MAX4947ETG+	-40°C to +85°C	24 TQFN-EP
MAX4948ERA+	-40°C to +85°C	25 UCSP-25
MAX4948ETG+	-40°C to +85°C	24 TQFN-EP

** Future product—contact factory for availability.*
+ Denotes lead-free package.
EP = Exposed paddle.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25 UCSP	R252A2+1	21-0466	Refer to Application Note 1891
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/06	Initial release	—
1	1/07	Updated *Ordering Information* table	1
2	12/14	Future product asterisk removed, product name updated to MAX4948ERA+	1, 2, 4, 12