

MAX4475–MAX4478/  
MAX4488/MAX4489

SOT23, Low-Noise, Low-Distortion,  
Wide-Band, Rail-to-Rail Op Amps

**Absolute Maximum Ratings**

Power-Supply Voltage (V <sub>DD</sub> to V <sub>SS</sub> ).....	-0.3V to +6.0V	8-Pin SO (derate 5.88mW/°C above +70°C).....	471mW
Analog Input Voltage (IN <sub>+</sub> , IN <sub>-</sub> ). (V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)		14-Pin SO (derate 8.33mW/°C above +70°C).....	667mW
SHDN Input Voltage .....(V <sub>SS</sub> - 0.3V) to +6.0V		14-Pin TSSOP (derate 9.1mW/°C above +70°C).....	727mW
Output Short-Circuit Duration to Either Supply .....	Continuous	Operating Temperature Range.....	-40°C to +125°C
Continuous Input Current (IN <sub>+</sub> , IN <sub>-</sub> ).....	±10mA	Junction Temperature.....	+150°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Storage Temperature Range.....	-65°C to +150°C
6-Pin SOT23 (derate 5.4mW/°C above +70°C) .....	431.3mW	Lead Temperature (soldering, 10s) .....	+300°C
6-Pin TDFN (derate 18.2mW/°C above 70°C) .....	1454mW	Soldering Temperature (reflow).....	+260°C
8-Pin μMAX (derate 4.5mW/°C above +70°C).....	362mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Information**

**SOT23-6**

PACKAGE CODE	U6F+6
Outline Number	<a href="#">21-0058</a>
Land Pattern Number	<a href="#">90-0175</a>
<b>Thermal Resistance, Single-Layer Board</b>	
Junction to Ambient (θ <sub>JA</sub> )	185.5°C/W
Junction to Case (θ <sub>JC</sub> )	75°C/W
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient (θ <sub>JA</sub> )	134.4°C/W
Junction to Case (θ <sub>JC</sub> )	39°C/W

**μMAX-8**

PACKAGE CODE	U8+4
Outline Number	<a href="#">21-0036</a>
Land Pattern Number	<a href="#">90-0092</a>
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient (θ <sub>JA</sub> )	206°C/W
Junction to Case (θ <sub>JC</sub> )	42

**μMAX-8**

PACKAGE CODE	U8+1
Outline Number	<a href="#">21-0036</a>
Land Pattern Number	<a href="#">90-0092</a>
<b>Thermal Resistance, Single-Layer Board</b>	
Junction to Ambient (θ <sub>JA</sub> )	221°C/W
Junction to Case (θ <sub>JC</sub> )	42°C/W
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient (θ <sub>JA</sub> )	206°C/W
Junction to Case (θ <sub>JC</sub> )	42°C/W

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## Package Information (continued)

### TSSOP-14

PACKAGE CODE	U14+2
Outline Number	<a href="#">21-0066</a>
Land Pattern Number	<a href="#">90-0113</a>
<b>Thermal Resistance, Single-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	110°C/W
Junction to Case ( $\theta_{JC}$ )	30°C/W
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	100.4°C/W
Junction to Case ( $\theta_{JC}$ )	30°C/W

### SO-8

PACKAGE CODE	S8+4
Outline Number	<a href="#">21-0041</a>
Land Pattern Number	<a href="#">90-0096</a>
<b>Thermal Resistance, Single-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	170°C/W
Junction to Case ( $\theta_{JC}$ )	40
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	132°C/W
Junction to Case ( $\theta_{JC}$ )	38

### SO-14

PACKAGE CODE	S14+4
Outline Number	<a href="#">21-0041</a>
Land Pattern Number	<a href="#">90-0112</a>
<b>Thermal Resistance, Single-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	120°C/W
Junction to Case ( $\theta_{JC}$ )	37°C/W
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	84°C/W
Junction to Case ( $\theta_{JC}$ )	34°C/W

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## Package Information (continued)

### TDFN-6

PACKAGE CODE	T633+2
Outline Number	<a href="#">21-0137</a>
Land Pattern Number	<a href="#">90-0058</a>
<b>Thermal Resistance, Single-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	55°C/W
Junction to Case ( $\theta_{JC}$ )	9°C/W
<b>Thermal Resistance, Multi-Layer Board</b>	
Junction to Ambient ( $\theta_{JA}$ )	42°C/W
Junction to Case ( $\theta_{JC}$ )	9°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### DC Electrical Characteristics

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ ,  $\overline{SHDN} = V_{DD}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	(Note 3)		2.7		5.5	V
Quiescent Supply Current Per Amplifier	$I_D$	Normal mode	$V_{DD} = 3V$		2.2		mA
			$V_{DD} = 5V$		2.5	4.4	
		Shutdown mode ( $\overline{SHDN} = V_{SS}$ ) (Note 2)			0.01	1.0	$\mu\text{A}$
Input Offset Voltage	$V_{OS}$	$T_A = +25^\circ\text{C}$			$\pm 70$	$\pm 350$	$\mu\text{V}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				$\pm 750$	
Input Offset Voltage Tempco	$TC_{V_{OS}}$				$\pm 0.3$	$\pm 6$	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	(Note 4)			$\pm 1$	$\pm 150$	pA
Input Offset Current	$I_{OS}$	(Note 4)			$\pm 1$	$\pm 150$	pA
Differential Input Resistance	$R_{IN}$				1000		G $\Omega$
Input Common-Mode Voltage Range	$V_{CM}$	Guaranteed by CMRR Test	$T_A = +25^\circ\text{C}$	-0.2		$V_{DD} - 1.6$	V
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-0.1		$V_{DD} - 1.7$	
Common-Mode Rejection Ratio	CMRR	$(V_{SS} - 0.2V) \leq V_{CM} \leq (V_{DD} - 1.6V)$	$T_A = +25^\circ\text{C}$	90	115		dB
		$(V_{SS} - 0.1V) \leq V_{CM} \leq (V_{DD} - 1.7V)$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	90			
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.7$ to $5.5V$		90	120		dB
Large-Signal Voltage Gain	$A_{VOL}$	$R_L = 10k\Omega$ to $V_{DD}/2$ ; $V_{OUT} = 100mV$ to $(V_{DD} - 125mV)$		90	120		dB
		$R_L = 1k\Omega$ to $V_{DD}/2$ ; $V_{OUT} = 200mV$ to $(V_{DD} - 250mV)$		85	110		
		$R_L = 500\Omega$ to $V_{DD}/2$ ; $V_{OUT} = 350mV$ to $(V_{DD} - 500mV)$		85	110		
Output Voltage Swing	$V_{OUT}$	$ V_{IN+} - V_{IN-}  \geq 10mV$ , $R_L = 10k\Omega$ to $V_{DD}/2$	$V_{DD} - V_{OH}$		10	45	mV
			$V_{OL} - V_{SS}$		10	40	
		$ V_{IN+} - V_{IN-}  \geq 10mV$ , $R_L = 1k\Omega$ to $V_{DD}/2$	$V_{DD} - V_{OH}$		80	200	
			$V_{OL} - V_{SS}$		50	150	
		$ V_{IN+} - V_{IN-}  \geq 10mV$ , $R_L = 500\Omega$ to $V_{DD}/2$	$V_{DD} - V_{OH}$		100	300	
			$V_{OL} - V_{SS}$		80	250	
Output Short-Circuit Current	$I_{SC}$				48		mA
Output Leakage Current	$I_{LEAK}$	Shutdown mode ( $\overline{SHDN} = V_{SS}$ ), $V_{OUT} = V_{SS}$ to $V_{DD}$			$\pm 0.001$	$\pm 1.0$	$\mu\text{A}$
$\overline{SHDN}$ Logic-Low	$V_{IL}$					$0.3 \times V_{DD}$	V
$\overline{SHDN}$ Logic-High	$V_{IH}$			$0.7 \times V_{DD}$			V
$\overline{SHDN}$ Input Current		$\overline{SHDN} = V_{SS}$ to $V_{DD}$			0.01	1	$\mu\text{A}$
Input Capacitance	$C_{IN}$				10		pF

## AC Electrical Characteristics

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ ,  $\overline{SHDN} = V_{DD}$ ,  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP	MAX4475–MAX4478	$A_V = +1V/V$		10		MHz
		MAX4488/MAX4489	$A_V = +5V/V$		42		
Slew Rate	SR	MAX4475–MAX4478	$A_V = +1V/V$		3		V/ $\mu s$
		MAX4488/MAX4489	$A_V = +5V/V$		10		
Full-Power Bandwidth (Note 5)		MAX4475–MAX4478	$A_V = +1V/V$		0.4		MHz
		MAX4488/MAX4489	$A_V = +5V/V$		1.25		
Peak-to-Peak Input Noise Voltage	$e_{n(P-P)}$	f = 0.1Hz to 10Hz			260		nV <sub>P-P</sub>
Input Voltage-Noise Density	$e_n$	f = 10Hz			21		nV/ $\sqrt{Hz}$
		f = 1kHz			4.5		
		f = 30kHz			3.5		
Input Current-Noise Density	$i_n$	f = 1kHz			0.5		fA/ $\sqrt{Hz}$
Total Harmonic Distortion Plus Noise (Note 6)	THD + N	$V_{OUT} = 2V_{P-P}$ , $A_V = +1V/V$ (MAX4475–MAX4478), $R_L = 10k\Omega$ to GND	f = 1kHz		0.0002		%
			f = 20kHz		0.0007		
		$V_{OUT} = 2V_{P-P}$ , $A_V = +1V/V$ (MAX4475–MAX4478), $R_L = 1k\Omega$ to GND	f = 1kHz		0.0002		
			f = 20kHz		0.001		
		$V_{OUT} = 2V_{P-P}$ , $A_V = +5V/V$ (MAX4488/ MAX4489), $R_L = 10k\Omega$ to GND	f = 1kHz		0.0004		
			f = 20kHz		0.0006		
Total Harmonic Distortion Plus Noise (Note 6)	THD + N	$V_{OUT} = 2V_{P-P}$ , $A_V = +5V/V$ (MAX4488/MAX4489), $R_L = 1k\Omega$ to GND	f = 1kHz		0.0005		%
			f = 20kHz		0.008		
Capacitive-Load Stability		No sustained oscillations			200		pF
Gain Margin	GM				12		dB
Phase Margin	$\phi_M$	MAX4475–MAX4478, $A_V = +1V/V$			70		degrees
		MAX4488/MAX4489, $A_V = +5V/V$			80		
Settling Time		To 0.01%, $V_{OUT} = 2V$ step			2		$\mu s$
Delay Time to Shutdown	$t_{SH}$				1.5		$\mu s$
Enable Delay Time from Shutdown	$t_{EN}$	$V_{OUT} = 2.5V$ , $V_{OUT}$ settles to 0.1%			10		$\mu s$
Power-Up Delay Time		$V_{DD} = 0$ to 5V step, $V_{OUT}$ stable to 0.1%			13		$\mu s$

**Note 1:** All devices are 100% tested at  $T_A = +25^\circ C$ . Limits over temperature are guaranteed by design.

**Note 2:**  $\overline{SHDN}$  is available on the MAX4475/MAX4488 only.

**Note 3:** Guaranteed by the PSRR test.

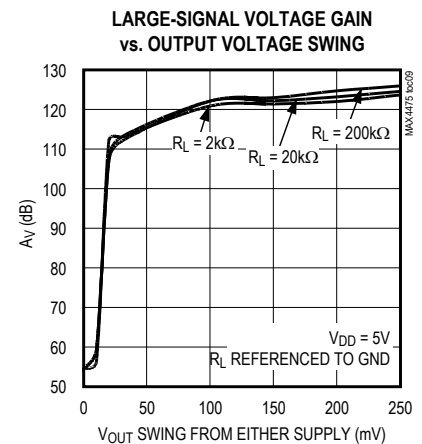
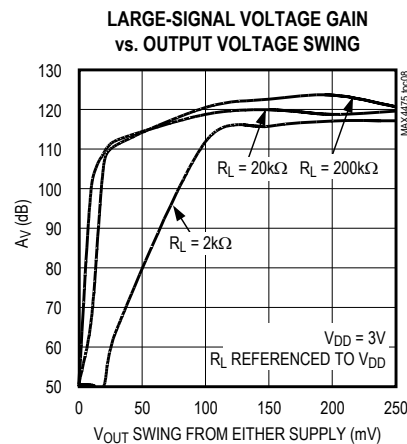
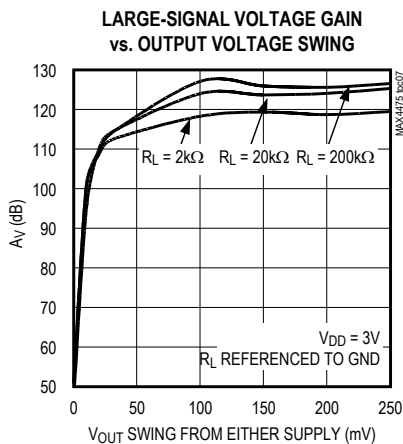
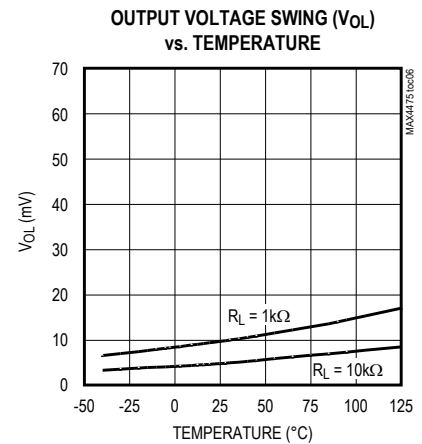
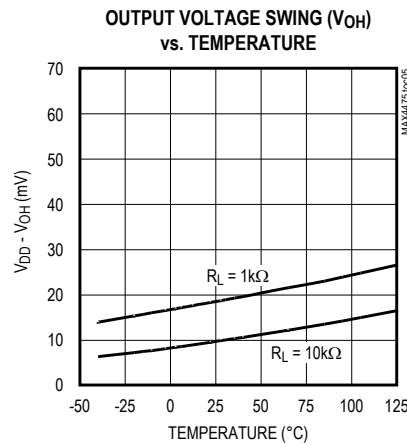
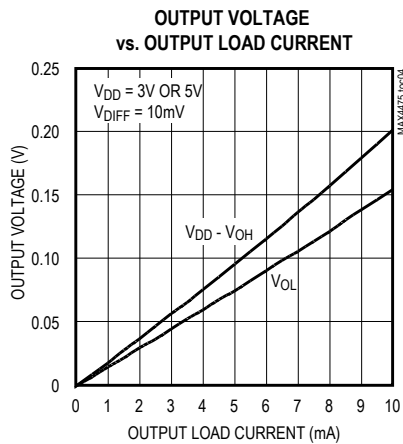
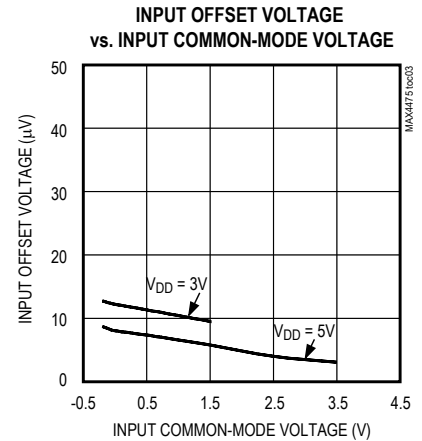
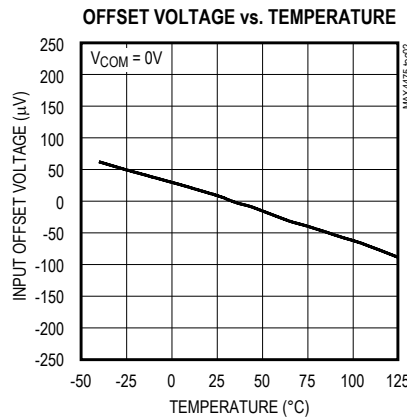
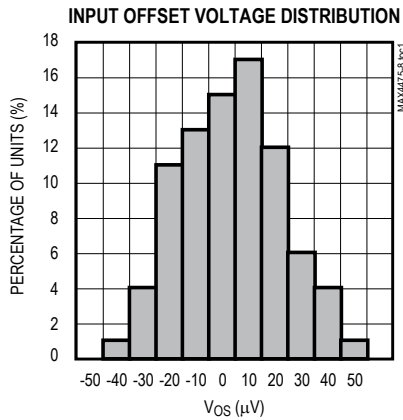
**Note 4:** Guaranteed by design.

**Note 5:** Full-power bandwidth for unity-gain stable devices (MAX4475–MAX4478) is measured in a closed-loop gain of +2V/V to accommodate the input voltage range,  $V_{OUT} = 4V_{P-P}$ .

**Note 6:** Lowpass-filter bandwidth is 22kHz for f = 1kHz and 80kHz for f = 20kHz. Noise floor of test equipment =  $10nV/\sqrt{Hz}$ .

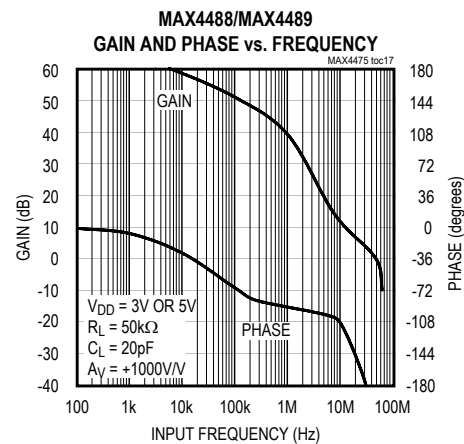
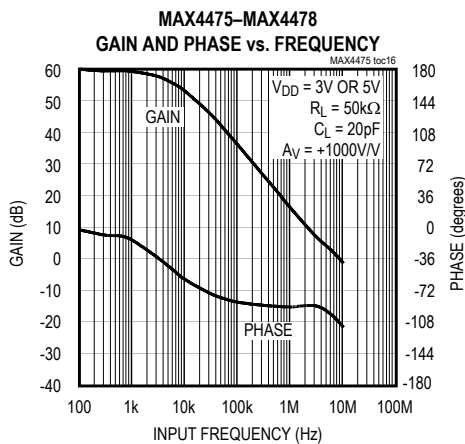
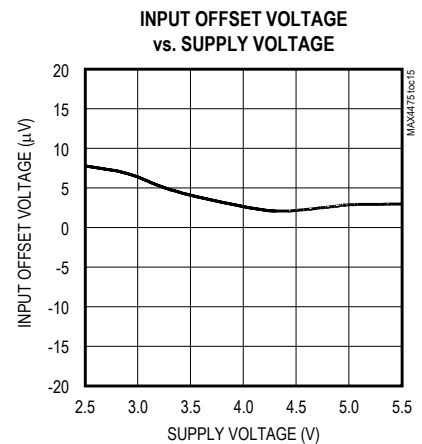
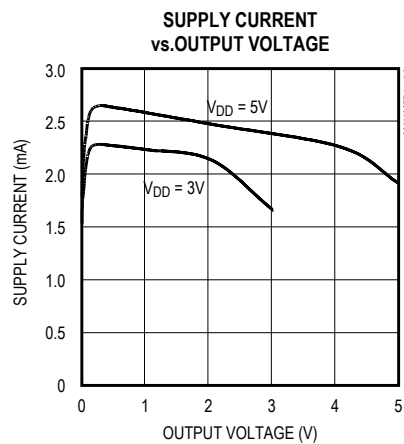
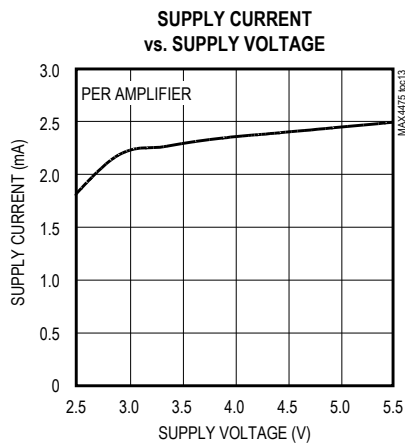
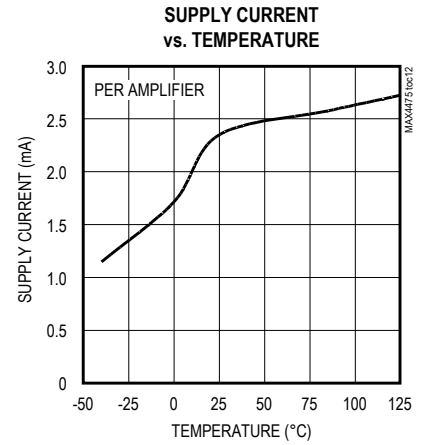
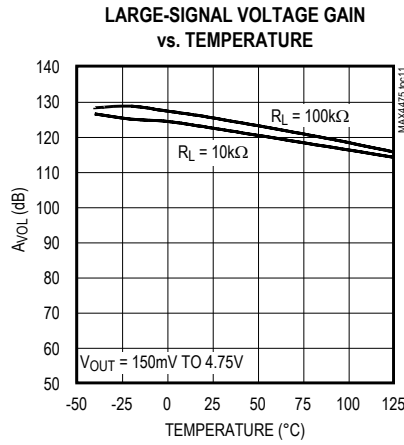
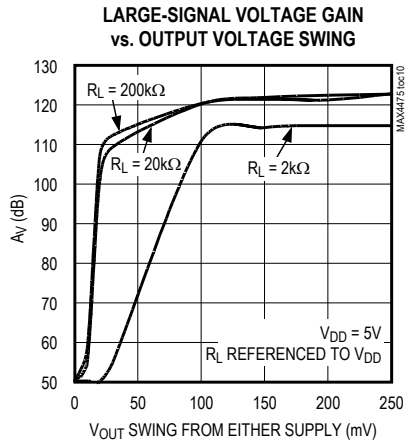
### Typical Operating Characteristics

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ , input noise floor of test equipment =  $10nV/\sqrt{Hz}$  for all distortion measurements,  $T_A = +25^\circ C$ , unless otherwise noted.)



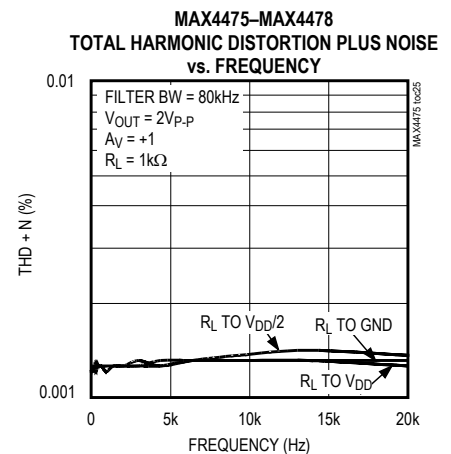
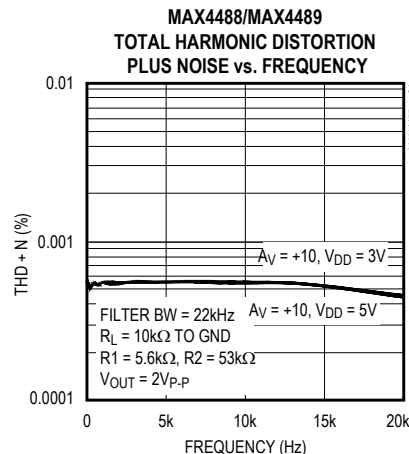
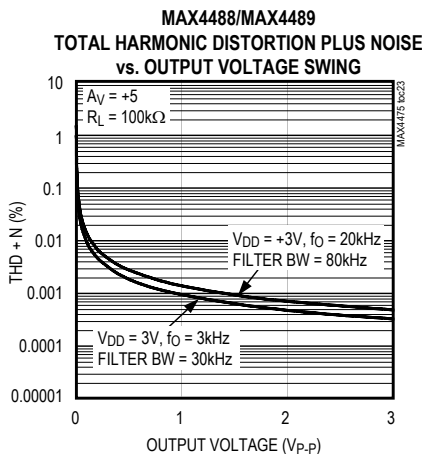
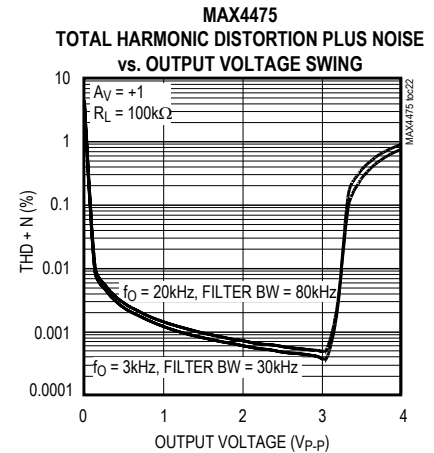
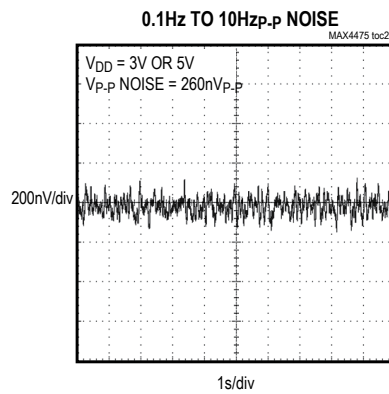
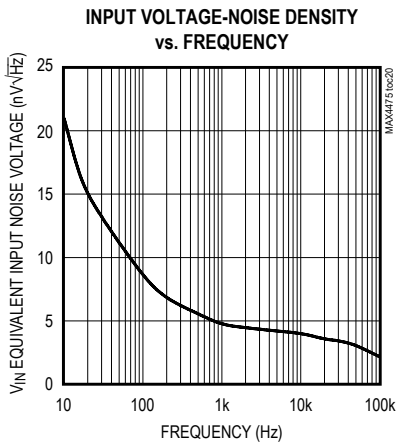
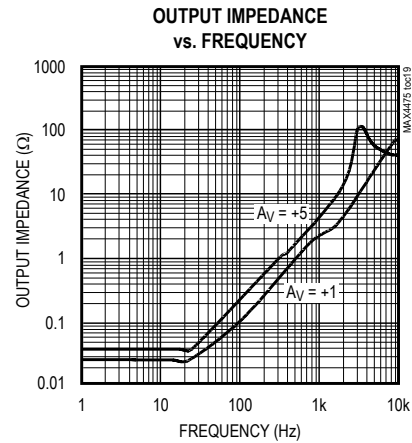
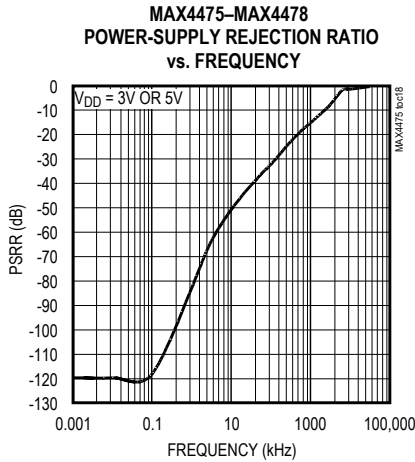
Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ , input noise floor of test equipment =  $10nV/\sqrt{Hz}$  for all distortion measurements,  $T_A = +25^\circ C$ , unless otherwise noted.)



Typical Operating Characteristics (continued)

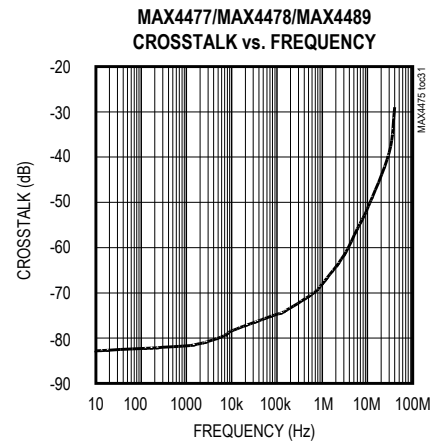
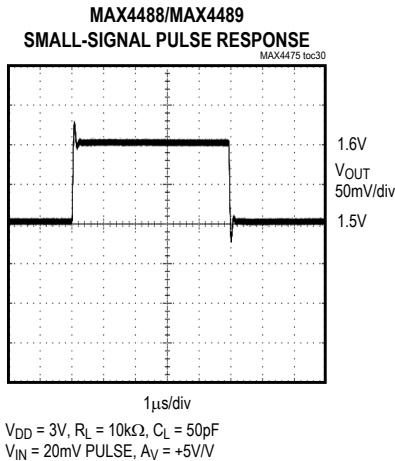
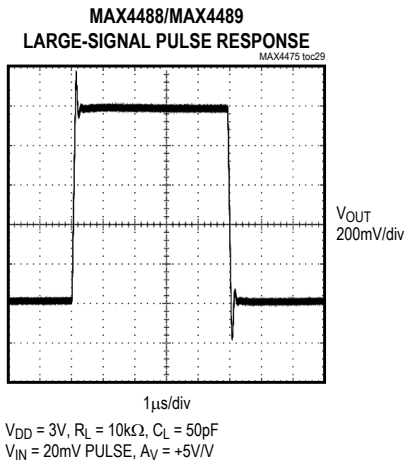
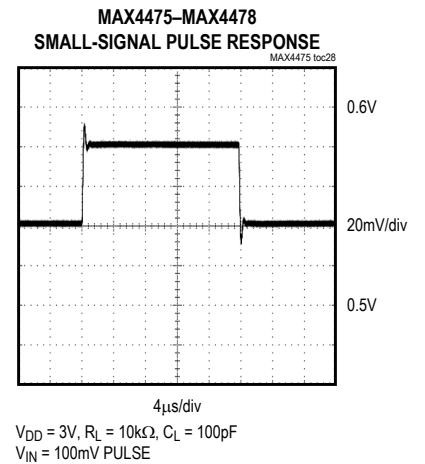
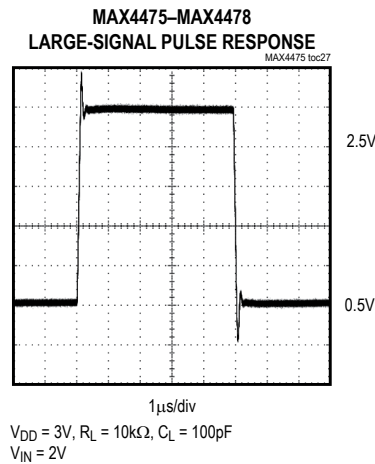
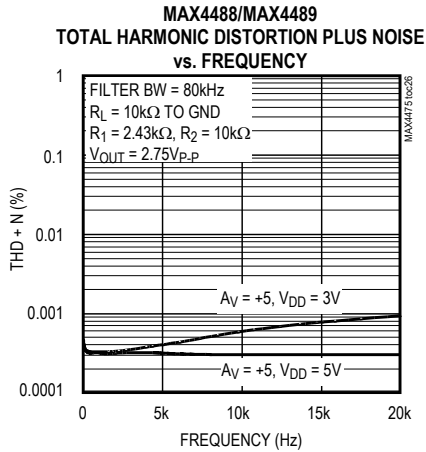
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Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L$  tied to  $V_{DD}/2$ , input noise floor of test equipment =  $10nV/\sqrt{Hz}$  for all distortion measurements,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

PIN					NAME	FUNCTION
MAX4475/ MAX4488	MAX4475/ MAX4488	MAX4476	MAX4477/ MAX4489	MAX4478		
SOT23/TDFN	SO/ $\mu$ MAX	SOT23/TDFN	SO/ $\mu$ MAX	SO/TSSOP		
1	6	1	1, 7	1, 7, 8, 14	OUT, OUTA, OUTB, OUTC, OUTD	Amplifier Output
2	4	2	4	11	V <sub>SS</sub>	Negative Supply. Connect to ground for single-supply operation
3	3	3	3, 5	3, 5, 10, 12	IN+, INA+, INB+, INC+, IND+	Noninverting Amplifier Input
4	2	4	2, 6	2, 6, 9, 13	IN-, INA-, INB-, INC-, IND-	Inverting Amplifier Input
6	7	6	8	4	V <sub>DD</sub>	Positive Supply
5	8	—	—	—	$\overline{\text{SHDN}}$	Shutdown Input. Connect to V <sub>DD</sub> for normal operation (amplifier(s) enabled).
—	1, 5	5	—	—	N.C.	No Connection. Not internally connected.
EP	—	EP	—	—	EP	Exposed Paddle (TDFN Only). Connect to V <sub>SS</sub> .

# MAX4475–MAX4478/ MAX4488/MAX4489

# SOT23, Low-Noise, Low-Distortion, Wide-Band, Rail-to-Rail Op Amps

## Detailed Description

The MAX4475–MAX4478/MAX4488/MAX4489 single-supply operational amplifiers feature ultra-low noise and distortion. Their low distortion and low noise make them ideal for use as preamplifiers in wide dynamic-range applications, such as 16-bit analog-to-digital converters (see *Typical Operating Circuit*). Their high-input impedance and low noise are also useful for signal conditioning of high-impedance sources, such as piezoelectric transducers.

These devices have true rail-to-rail output operation, drive loads as low as  $1\text{k}\Omega$  while maintaining DC accuracy, and can drive capacitive loads up to  $200\text{pF}$  without oscillation. The input common-mode voltage range extends from  $(V_{DD} - 1.6\text{V})$  to  $200\text{mV}$  below the negative rail. The push-pull output stage maintains excellent DC characteristics, while delivering up to  $\pm 5\text{mA}$  of current.

The MAX4475–MAX4478 are unity-gain stable, while the MAX4488/MAX4489 have a higher slew rate and are stable for gains  $\geq 5\text{V/V}$ . The MAX4475/MAX4488 feature a low-power shutdown mode, which reduces the supply current to  $0.01\mu\text{A}$  and disables the outputs.

## Low Distortion

Many factors can affect the noise and distortion that the device contributes to the input signal. The following guidelines offer valuable information on the impact of design choices on Total Harmonic Distortion (THD).

Choosing proper feedback and gain resistor values for a particular application can be a very important factor in reducing THD. In general, the smaller the closed-loop gain, the smaller the THD generated, especially when driving heavy resistive loads. The THD of the part normally increases at approximately  $20\text{dB}$  per decade, as a function of frequency. Operating the device near or above the full-power bandwidth significantly degrades distortion.

Referencing the load to either supply also improves the part's distortion performance, because only one of the MOSFETs of the push-pull output stage drives the output. Referencing the load to midsupply increases the part's distortion for a given load and feedback setting. (See the Total Harmonic Distortion vs. Frequency graph in the *Typical Operating Characteristics*.)

For gains  $\geq 5\text{V/V}$ , the decompensated devices MAX4488/MAX4489 deliver the best distortion performance, since they have a higher slew rate and provide a higher amount of loop gain for a given closed-loop gain setting. Capacitive loads below  $100\text{pF}$  do not significantly affect distortion results. Distortion performance is relatively constant over supply voltages.

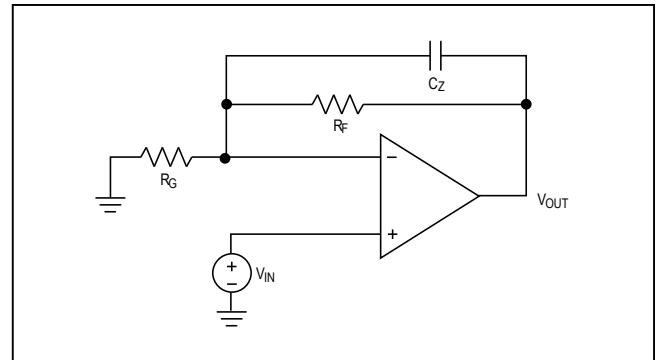


Figure 1. Adding Feed-Forward Compensation

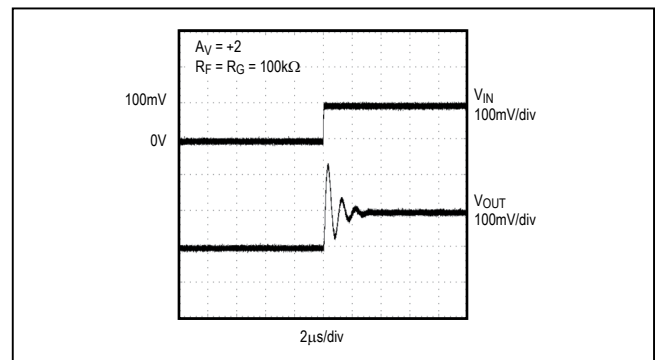


Figure 2a. Pulse Response with No Feed-Forward Compensation

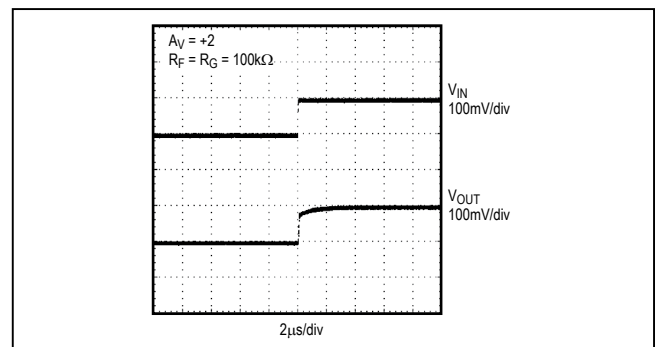


Figure 2b. Pulse Response with  $10\text{pF}$  Feed-Forward Compensation

### Low Noise

The amplifier's input-referred noise-voltage density is dominated by flicker noise at lower frequencies, and by thermal noise at higher frequencies. Because the thermal noise contribution is affected by the parallel combination of the feedback resistive network ( $R_F \parallel R_G$ , Figure 1), these resistors should be reduced in cases where the system bandwidth is large and thermal noise is dominant. This noise contribution factor decreases, however, with increasing gain settings.

For example, the input noise-voltage density of the circuit with  $R_F = 100\text{k}\Omega$ ,  $R_G = 11\text{k}\Omega$  ( $A_V = +5\text{V/V}$ ) is  $e_n = 14\text{nV}/\sqrt{\text{Hz}}$ ,  $e_n$  can be reduced to  $6\text{nV}/\sqrt{\text{Hz}}$  by choosing  $R_F = 10\text{k}\Omega$ ,  $R_G = 1.1\text{k}\Omega$  ( $A_V = +5\text{V/V}$ ), at the expense of greater current consumption and potentially higher distortion. For a gain of  $100\text{V/V}$  with  $R_F = 100\text{k}\Omega$ ,  $R_G = 1.1\text{k}\Omega$ , the  $e_n$  is still a low  $6\text{nV}/\sqrt{\text{Hz}}$ .

### Using a Feed-Forward Compensation Capacitor, $C_Z$

The amplifier's input capacitance is  $10\text{pF}$ . If the resistance seen by the inverting input is large (feedback network), this can introduce a pole within the amplifier's bandwidth resulting in reduced phase margin. Compensate the reduced phase margin by introducing a feed-forward capacitor ( $C_Z$ ) between the inverting input and the output (Figure 1). This effectively cancels the pole from the inverting input of the amplifier. Choose the value of  $C_Z$  as follows:

$$C_Z = 10 \times (R_F / R_G) \text{ [pF]}$$

In the unity-gain stable MAX4475–MAX4478, the use of a proper  $C_Z$  is most important for  $A_V = +2\text{V/V}$ , and  $A_V = -1\text{V/V}$ . In the decompensated MAX4488/MAX4489,  $C_Z$  is most important for  $A_V = +10\text{V/V}$ . Figures 2a and 2b show transient response both with and without  $C_Z$ .

Using a slightly smaller  $C_Z$  than suggested by the formula above achieves a higher bandwidth at the expense of reduced phase and gain margin. As a general guideline, consider using  $C_Z$  for cases where  $R_G \parallel R_F$  is greater than  $20\text{k}\Omega$  (MAX4475–MAX4478) or greater than  $5\text{k}\Omega$  (MAX4488/MAX4489).

### Applications Information

The MAX4475–MAX4478/MAX4488/MAX4489 combine good driving capability with ground-sensing input and rail-to-rail output operation. With their low distortion and low noise, they are ideal for use in ADC buffers, medical instrumentation systems and other noise-sensitive applications.

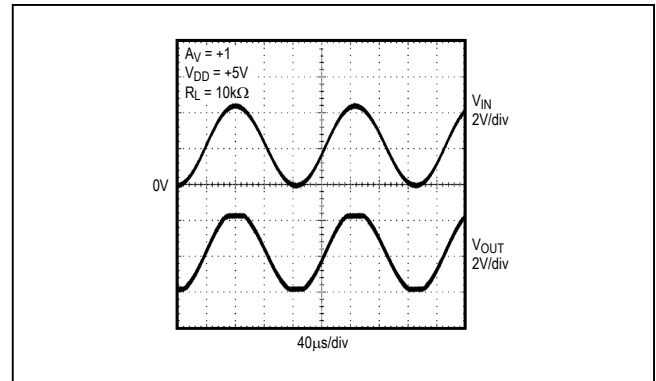


Figure 3. Overdriven Input Showing No Phase Reversal

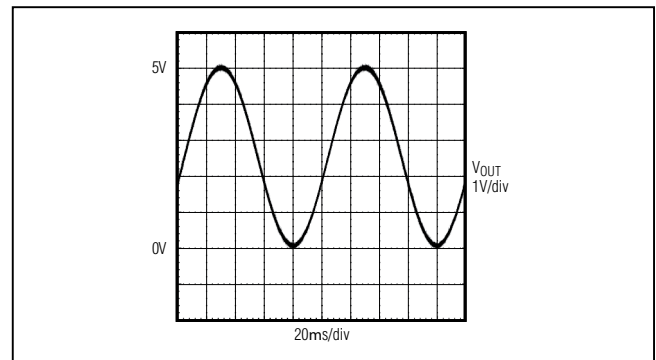


Figure 4. Rail-to-Rail Output Operation

### Ground-Sensing and Rail-to-Rail Outputs

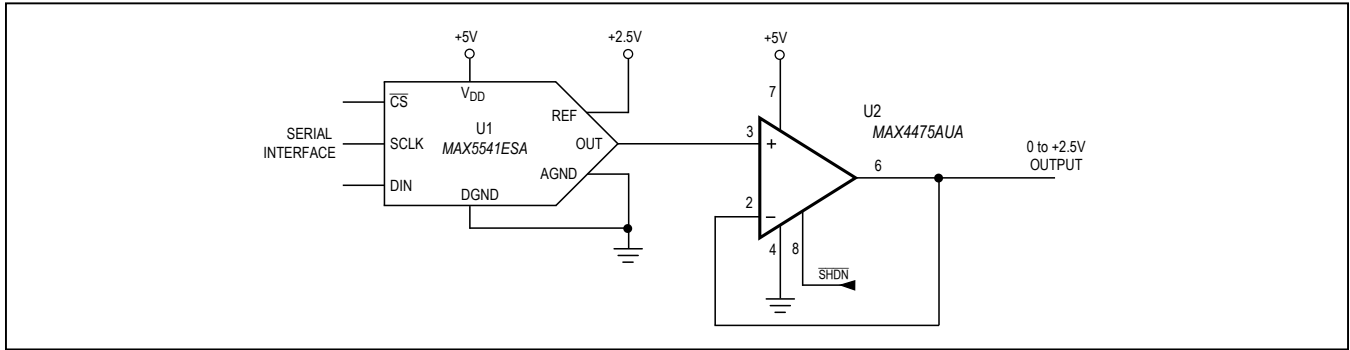
The common-mode input range of these devices extends below ground, and offers excellent common-mode rejection. These devices are guaranteed not to undergo phase reversal when the input is overdriven (Figure 3).

Figure 4 showcases the true rail-to-rail output operation of the amplifier, configured with  $A_V = 5\text{V/V}$ . The output swings to within  $8\text{mV}$  of the supplies with a  $10\text{k}\Omega$  load, making the devices ideal in low-supply voltage applications.

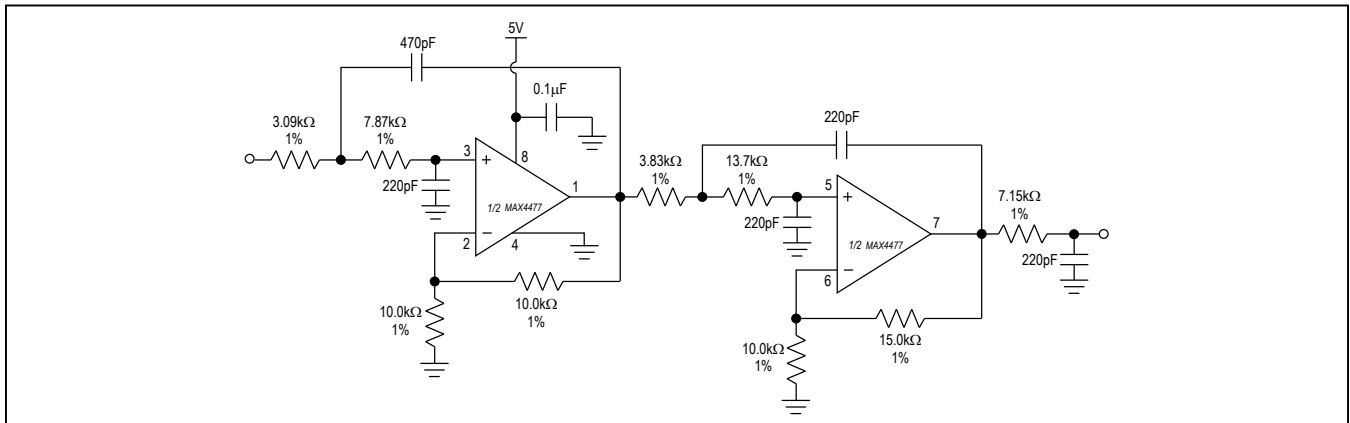
### Power Supplies and Layout

The MAX4475–MAX4478/MAX4488/MAX4489 operate from a single  $+2.7\text{V}$  to  $+5.5\text{V}$  power supply or from dual supplies of  $\pm 1.35\text{V}$  to  $\pm 2.75\text{V}$ . For single-supply operation, bypass the power supply with a  $0.1\mu\text{F}$  ceramic

### Typical Application Circuit



### Typical Operating Circuit



capacitor placed close to the  $V_{DD}$  pin. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and output. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amp's pins.

### Typical Application Circuit

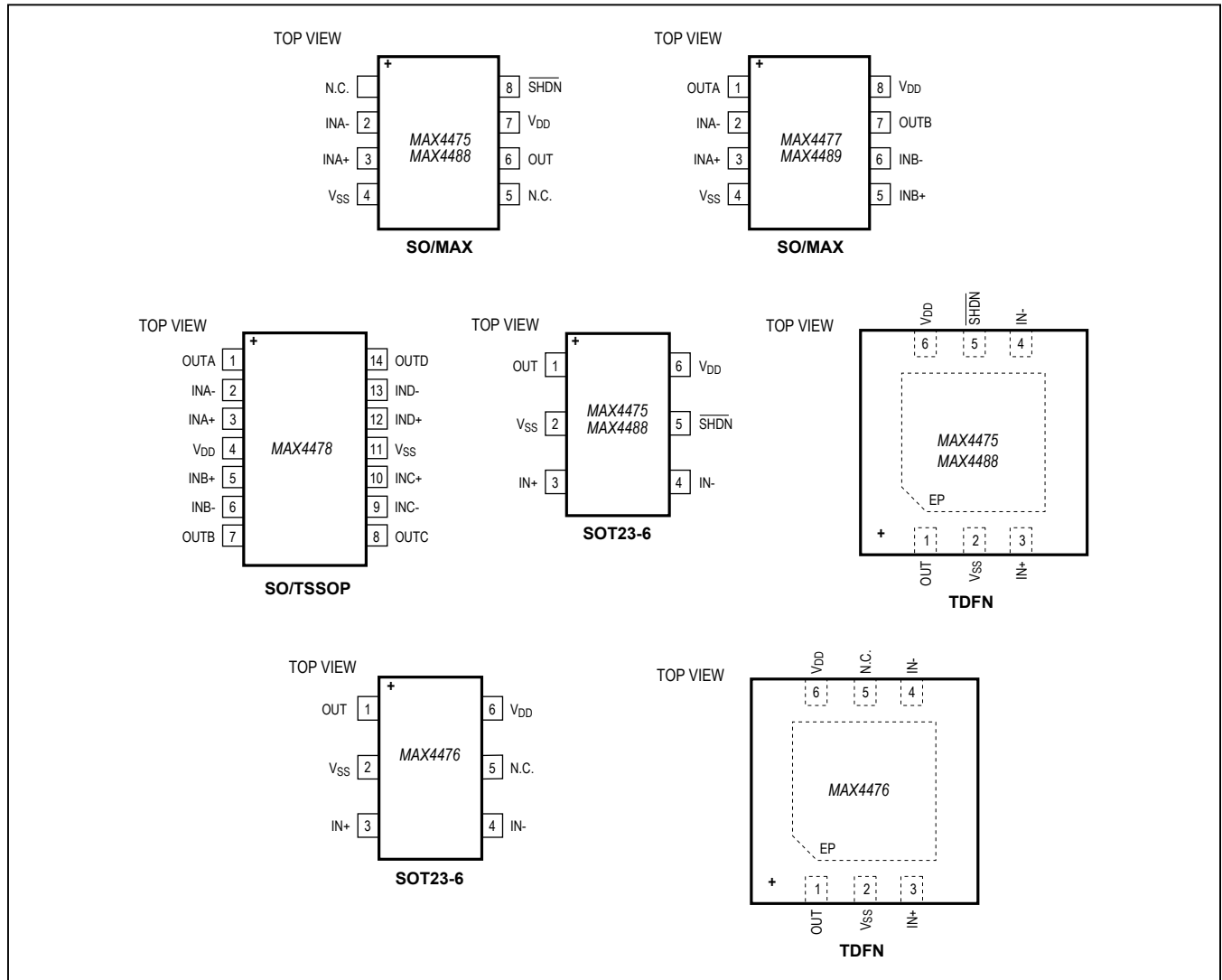
The *Typical Application Circuit* shows the single MAX4475 configured as an output buffer for the MAX5541 16-bit DAC. Because the MAX5541 has an unbuffered voltage output, the input bias current of the op amp used must be less than 6nA to maintain 16-bit accuracy. The MAX4475 has an input bias current of only 150pA (max), virtually eliminating this as a source

of error. In addition, the MAX4475 has excellent open-loop gain and common-mode rejection, making this an excellent output buffer amplifier.

### DC-Accurate Lowpass Filter

The MAX4475–MAX4478/MAX4488/MAX4489 offer a unique combination of low noise, wide bandwidth, and high gain, making them an excellent choice for active filters up to 1MHz. The *Typical Operating Circuit* shows the dual MAX4477 configured as a 5th order Chebyshev filter with a cutoff frequency of 100kHz. The circuit is implemented in the Sallen-Key topology, making this a DC-accurate filter.

Pin Configurations



MAX4475–MAX4478/  
MAX4488/MAX4489

SOT23, Low-Noise, Low-Distortion,  
Wide-Band, Rail-to-Rail Op Amps

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
<b>MAX4475</b> AUT+T	-40°C to +125°C	6 SOT23	AAZV
MAX4475AUA+	-40°C to +125°C	8 $\mu$ MAX	—
MAX4475ASA+	-40°C to +125°C	8 SO	—
MAX4475ATT+T	-40°C to +125°C	6 TDFN-EP*	+ADD
MAX4475AUT/V+T	-40°C to +125°C	6 SOT23	+ACQQ
<b>MAX4476</b> AUT+T	-40°C to +125°C	6 SOT23	AAZX
MAX4476ATT+T	-40°C to +125°C	6 TDFN-EP*	+ADF
<b>MAX4477</b> AUA+	-40°C to +125°C	8 $\mu$ MAX	—
MAX4477AUA+	-40°C to +125°C	8 $\mu$ MAX	—
MAX4477AUA/V+T	-40°C to +125°C	8 $\mu$ MAX	+AA/V
MAX4477ASA+	-40°C to +125°C	8 SO	—
<b>MAX4478</b> AUD+	-40°C to +125°C	14 TSSOP	—
MAX4478AUD/V+	-40°C to +125°C	14 TSSOP	—
MAX4478ASD+	-40°C to +125°C	14 SO	—
<b>MAX4488</b> AUT+T	-40°C to +125°C	6 SOT23	AAZW
MAX4488AUA+	-40°C to +125°C	8 $\mu$ MAX	—
MAX4488ASA+	-40°C to +125°C	8 SO	—
MAX4488ATT+T	-40°C to +125°C	6 TDFN-EP*	+ADE
<b>MAX4489</b> AUA+	-40°C to +125°C	8 $\mu$ MAX	—
MAX4489AUA/V+T	-40°C to +125°C	8 $\mu$ MAX	—
MAX4489ASA+	-40°C to +125°C	8 SO	—

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad (connect to  $V_{SS}$ ).

/V denotes an automotive qualified part.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Selector Guide

PART	GAIN BW (MHz)	STABLE GAIN (V/V)	NO. OF AMPS	$\overline{\text{SHDN}}$
MAX4475	10	1	1	Yes
MAX4476	10	1	1	—
MAX4477	10	1	2	—
MAX4478	10	1	4	—
MAX4488	42	5	1	Yes
MAX4489	42	5	2	—

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	12/09	Added lead-free designations and an automotive part to the Ordering Information and added input current spec in Absolute Maximum Ratings section	1, 2, 13
5	7/10	Added <i>IV</i> designation to the MAX4475 product and soldering temperature	1, 2
6	6/12	Added <i>IV</i> designation for MAX4489.	13
7	1/18	Added AEC statement to <i>Features</i> section	1
8	7/18	Updated <i>Ordering Information</i> table	14
9	7/18	Updated <i>Absolute Maximum Rating</i> and <i>Package Information</i>	2, 14
10	8/18	Updated <i>Package Information</i> section	2–4
11	4/19	Updated <i>General Description</i> and <i>Ordering Information</i> section	1, 16

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