Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +5.5V
IN+, IN- .....-0.3V to (V_{CC} + 0.3V)
OUT+, OUT- .....-0.3V to (V_{CC} + 3.6V)
TXEN, SDA, SCLK, $\overline{CS}$ ..... -0.3V to +4.2V
RF Input Power ..... +10dBm
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 29mW/°C above T_A = +70°C)..... 2000mW

Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(*Typical Application Circuit* as shown, V_{CC} = 4.75V to 5.25V, V_{GND} = 0V, TXEN = high, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75		5.25	V
Supply Current Transmit Mode	I_{CC}	Gain code = 63, power code = 3 (33dB gain typ)		360	385	mA
		Gain code = 59, power code = 1 (29dB gain typ)		190		
Supply Current Transmit Disable Mode	I_{CC}	TXEN = low		5	6.5	mA
Input High Voltage	V_{INH}		2.0		3.6	V
Input Low Voltage	V_{INL}				0.7	V
Input High Current	I_{BIASH}				10	µA
Input Low Current	I_{BIASL}		-10			µA

AC Electrical Characteristics

(*Typical Application Circuit* as shown, V_{CC} = 4.75V to 5.25V, V_{GND} = 0V, TXEN = high, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_{IN}	(Note 3)	5		85	MHz
Voltage Gain, Z_{IN} = 200Ω, Z_{OUT} = 75Ω, Power Code = 3 (Note 4)	A_V	Gain code = 63	32	33	34	dB
		Gain code = 53	22	23	24	
		Gain code = 43	12	13	14	
		Gain code = 33	2	3	4	
		Gain code = 23	-8	-7	-6	
		Gain code = 13	-18	-17	-16	
		Gain code = 03	-28	-27	-26	
Voltage Gain Variation with Power Code, Any Gain Code				±0.1		dB
Gain Rolloff		Voltage gain = -28dB to +33dB, f_{IN} = 5MHz to 85MHz		-0.3		dB
Gain Step Size		Voltage gain = -28dB to +33dB, fIN = 5MHz to 85MHz	0.7	1.0	1.3	dB
Transmit-Disable Mode Noise		Any BW = 160kHz from 5MHz to 85MHz, TXEN = low, voltage gain = -27dB to +33dB (Note 5)		-66		dBmV
Isolation in Transmit-Disable Mode		TXEN = low		80		dB
Noise Figure	NF	Transmit mode, voltage gain = +13dB to +33dB (Note 5)			11	dB
Noise Figure Slope		Transmit mode, voltage gain = -27dB to +33dB		-1.0		dB/dB
Transmit-Disable/Transmit-Enable Transient Duration		TXEN input rise/fall time < 0.1µs		2		µs
Transmit-Disable/Transmit-Enable Transient Step Size		Gain = 33dB		25	85	mV_{P-P}
		Gain = 4dB		1		
Input Impedance	Z_{IN}	Balanced		200		Ω
Input Return Loss		200Ω system		15		dB
Output Return Loss		75Ω system (Note 5)	11	15		dB
Output Return Loss in Transmit-Disable Mode		75Ω system, TXEN = low (Note 5)	11	15		dB
2nd Harmonic Distortion	HD2	Input tone at 33dBmV, V_{OUT} = +64dBmV, power code = 3 (Note 5)		-68	-57	dBc
3rd Harmonic Distortion	HD3	Input tone at 33dBmV, V_{OUT} = +64dBmV, power code = 3 (Note 5)		-65	-59	dBc
Two-Tone 2nd-Order Distortion	IM2	Input tones at 30dBmV, V_{OUT} = +61dBmV/tone, power code = 3 (Note 5)		-65	-57	dBc
Two-Tone 3rd-Order Distortion	IM3	Input tones at 30dBmV, V_{OUT} = +61dBmV/tone, power code = 3 (Note 5)		-65	-57	dBc
Four Tone Spurs		Four input tones at 27dBmV, V_{OUT} = +58dBmV/tone, power code = 3		-58		dBc
Output 1dB Compression Point	P1dB	Gain = 32dB		74		dBmV

Timing Characteristics

(*Typical Application Circuit* as shown, V_{CC} = 4.75V to 5.25V, V_{GND} = 0V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C.) (Note 2)

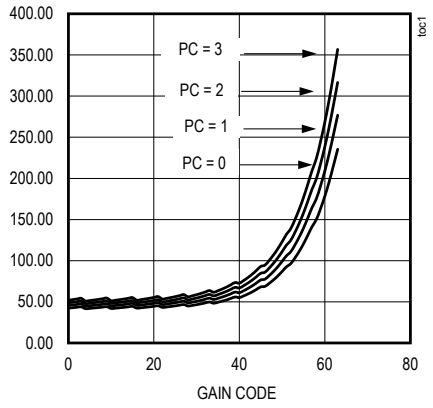
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to SCLK Rise Setup Time	t_{SENS}			20		ns
$\overline{CS}$ to SCLK Rise Hold Time	t_{SENH}			10		ns
SDA to SCLK Setup Time	t_{SDAS}			20		ns
SDA to SCLK Hold Time	t_{SDAH}			10		ns
SCLK Pulse-Width High	t_{SCLKH}			50		ns
SCLK Pulse-Width Low	t_{SCLKL}			50		ns
Maximum SCLK Frequency			10			MHz

Note 2: Min/max values are production tested at T_A = +85°C. Min/max limits at T_A = -40°C and T_A = +25°C are guaranteed by design and characterization.
Note 3: Production tested at 10MHz and 85MHz.
Note 4: Voltage gain does not include loss due to input and output transformers.
Note 5: Guaranteed by design and characterization.

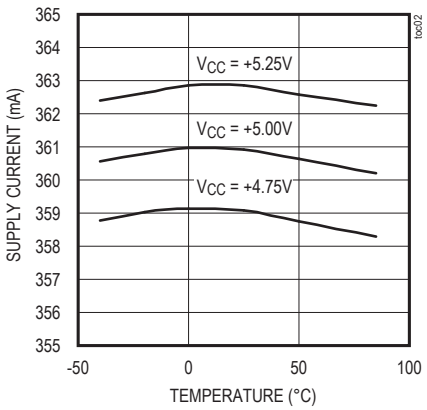
Typical Operating Characteristics

(MAX3519 EV kit, V_{CC} = +5V, V_{IN} = 33dBmV, f_{IN} = 42MHz, Z_{LOAD} = 75Ω, T_A = +25°C, power code = 3, unless otherwise noted.)

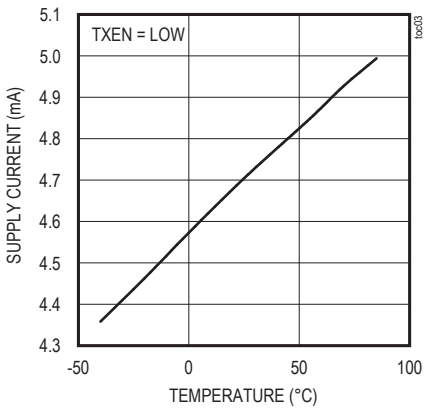
SUPPLY CURRENT vs. GAIN CODE



SUPPLY CURRENT vs. TEMPERATURE



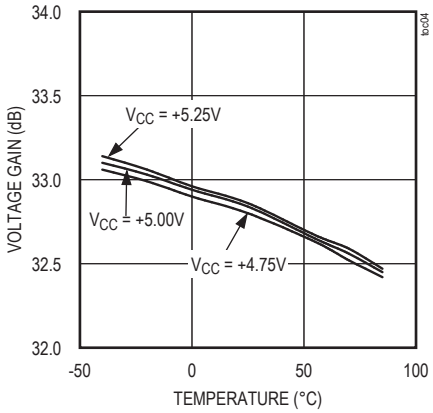
TRANSMIT DISABLE CURRENT vs. TEMPERATURE



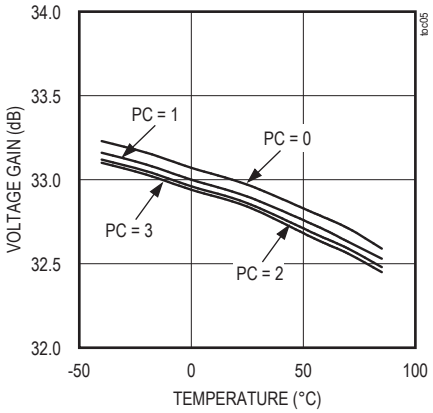
Typical Operating Characteristics (continued)

(MAX3519 EV kit, V_{CC} = +5V, V_{IN} = 33dBmV, f_{IN} = 42MHz, Z_{LOAD} = 75Ω, T_A = +25°C, power code = 3, unless otherwise noted.)

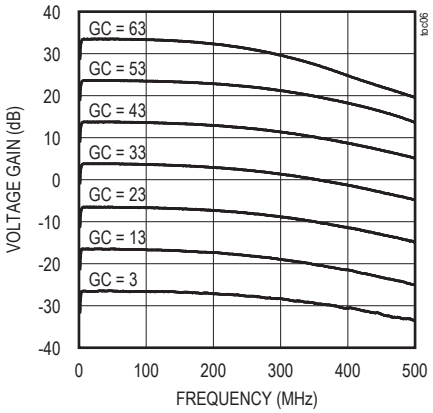
VOLTAGE GAIN vs. TEMPERATURE



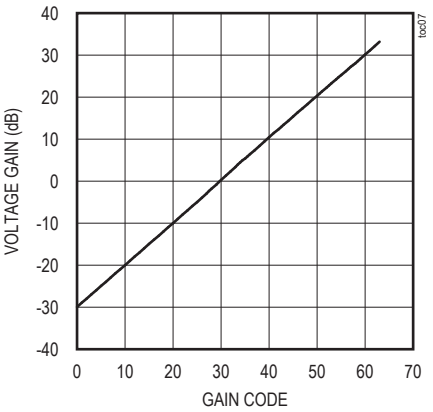
VOLTAGE GAIN vs. TEMPERATURE



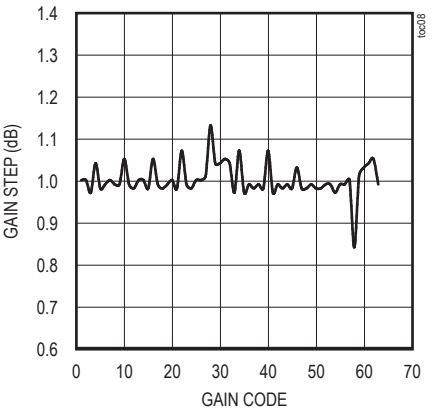
VOLTAGE GAIN vs. FREQUENCY



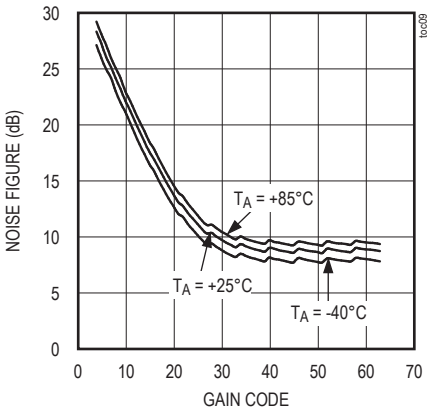
VOLTAGE GAIN vs. GAIN CODE



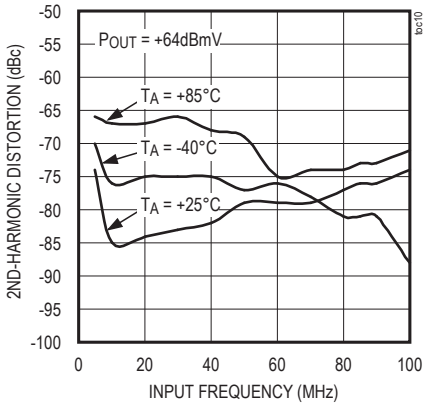
GAIN STEP SIZE vs. GAIN CODE



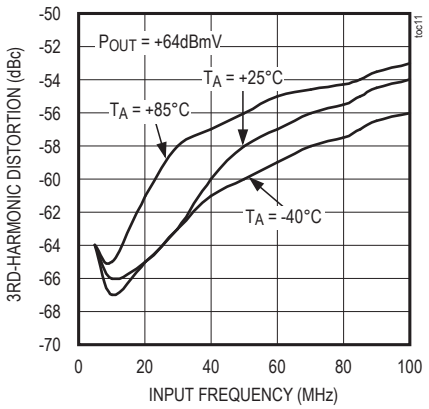
NOISE FIGURE vs. GAIN CODE



2ND-HARMONIC DISTORTION vs. INPUT FREQUENCY



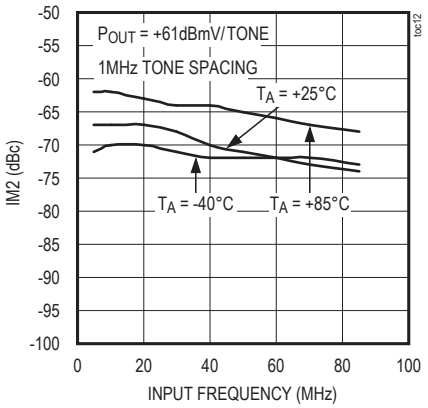
3RD-HARMONIC DISTORTION vs. INPUT FREQUENCY



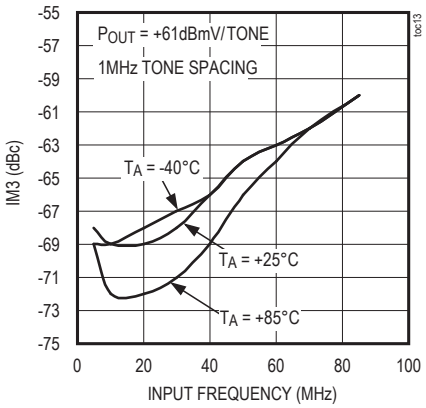
Typical Operating Characteristics (continued)

(MAX3519 EV kit, V_{CC} = +5V, V_{IN} = 33dBmV, f_{IN} = 42MHz, Z_{LOAD} = 75Ω, T_A = +25°C, power code = 3, unless otherwise noted.)

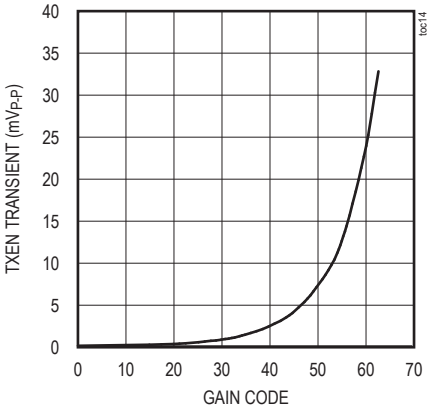
IM2 vs. INPUT FREQUENCY ($f_1 + f_2$)



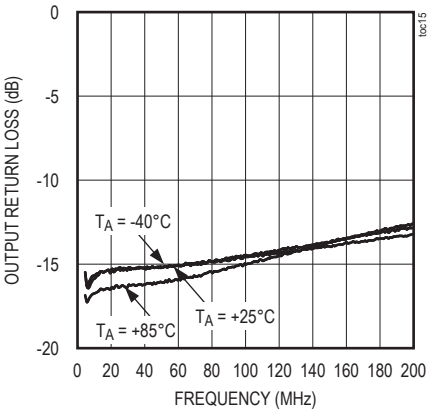
IM3 vs. INPUT FREQUENCY ($2f_1 - f_2$)



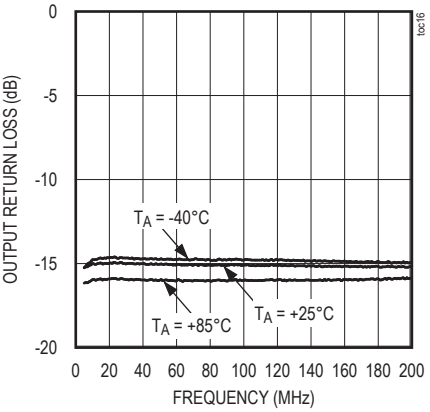
TXEN TRANSIENT vs. GAIN CODE



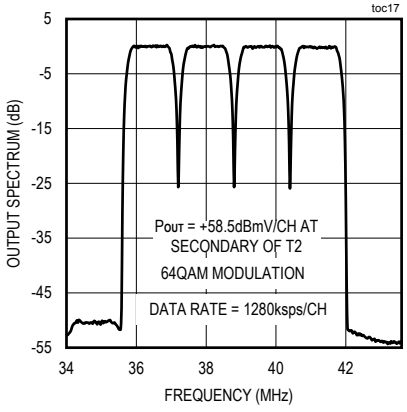
OUTPUT RETURN LOSS vs. FREQUENCY



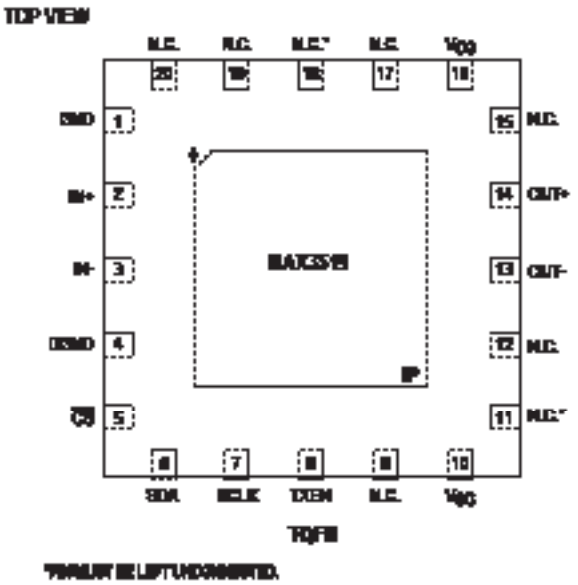
OUTPUT RETURN LOSS vs. FREQUENCY (TRANSMIT DISABLE MODE)



42MHz FOUR-CHANNEL OUTPUT SPECTRUM



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	IN+	Positive PGA Input
3	IN-	Negative PGA Input
4	DGND	Digital Ground
5	$\overline{CS}$	Serial Interface Enable
6	SDA	Serial Interface Data
7	SCLK	Serial Interface Clock
8	TXEN	Transmit Enable. TXEN = high places device in transmit mode
9, 12, 15 17, 19, 20	N.C.	No Connection
10	V_{CC}	Supply Voltage for Serial Interface
11, 18	N.C.*	Test Connection. Must be left open for normal operation.
13	OUT-	Negative Output
14	OUT+	Positive Output
16	V_{CC}	Supply Voltage for Programmable-Gain Amplifier (PGA)
—	EP	Exposed Pad. Connect to ground.

Detailed Description

Programmable-Gain Amplifier

The programmable-gain amplifier (PGA) provides 63dB of output level control in 1dB steps. The gain of the PGA is determined by a 6-bit gain code (GC5–GC0) programmed through the serial data interface (Table 1 and Table 2). Specified performance is achieved when the input is driven differentially.

Four power codes (PC1–PC0) allow the PGA to be used with reduced bias current when distortion performance can be relaxed. In addition, for each power code, bias current is automatically reduced with gain code for maximum efficiency.

The PGA features a differential Class A output stage capable of driving four +58dBmV QPSK modulated signals, or a single +64dBmV QPSK modulated signal into a 75Ω load. This architecture provides superior even-order distortion performance but requires that a transformer be used to convert to a single-ended output. In transmit-disable mode, the output amplifiers are powered down, resulting in low output noise, while maintaining impedance match.

3-Wire Serial Interface (SPI) and Control Registers

The MAX3519 includes two programmable registers for initializing the part and setting the gain and power consumption. The 4 MSBs are address bits; the 8 least significant bits (LSBs) are used for register data. Data is shifted MSB first.

Note: The registers must be written 100µs after the device is powered up, and no earlier. Once a new set of register data is clocked in, the corresponding power code and/or gain code does not take effect until $\overline{CS}$ transitions from low to high.

Applications Information

Power Codes

The MAX3519 is designed to exceed the stringent linearity requirements of DOCSIS 3.0 using power code (PC) 3. For DOCSIS 2.0, PC = 1 is recommended, which results in substantial supply current reduction. The full range of gain codes can be used in any power code. The gain difference between power codes is typically less than 0.1dB.

Table 1. Register Description

REGISTER NAME	REGISTER ADDRESS	DATA 8 BITS							
		B7	B6	B5	B4	B3	B2	B1	B0
Power/Gain	0000	PC1	PC0	GC5	GC4	GC3	GC2	GC1	GC0
Initialize	0001	0	0	0	0	0	0	0	0

Table 2. Reg 00 Gain Control

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
PC[1:0]	7,6	11	Sets the power code, which controls the bias current drawn by the device in transmit mode: 11 - PC = 3, maximum current draw . . . 00 - PC = 0, minimum current draw (See the *Typical Operating Characteristics*.)
GC[5:0]	5,4,3,2,1,0	111101	Sets the gain code, which determines the voltage gain of the amplifier: 11 1111 - GC = 63, voltage gain = 33dB (typ). 11 1110 - GC = 62, voltage gain = 32dB (typ). . . . 00 0011 - GC = 03, voltage gain = -27dB (typ). (See the *AC Electrical Characteristics*.)

Table 3. Initialize Register

BIT NAME	BIT LOCATION (0 = LSB)	RECOMMENDED DEFAULT	FUNCTION
—	7,6,5,4,3,2,1,0	0000 0000	Must be programmed to 0000 0000 upon power-up for specified performance.

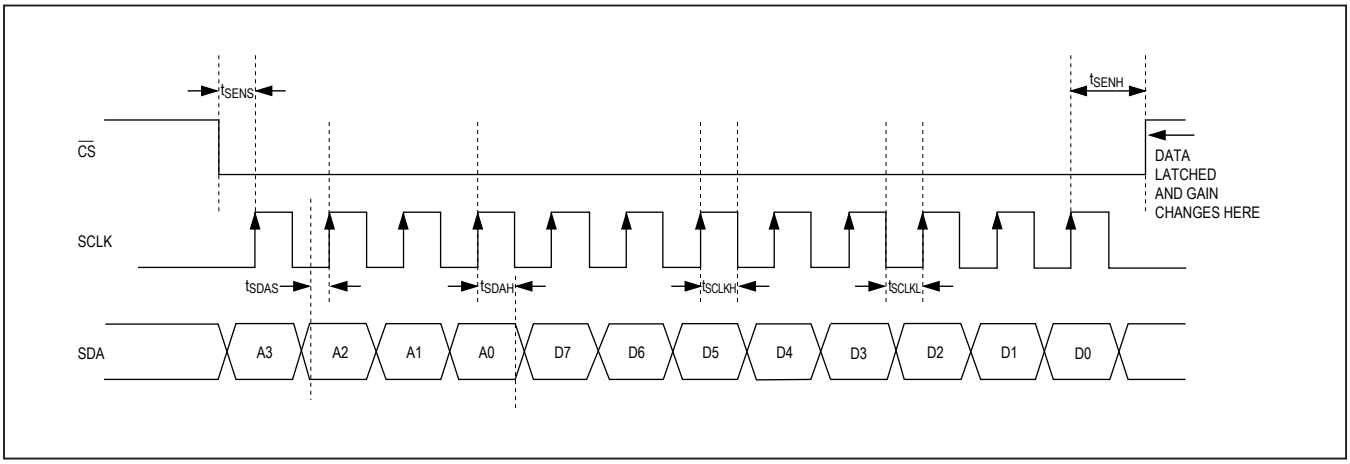


Figure 1. SPI 3-Wire Interface Timing Diagram

Transmit Disable Mode

Between bursts in a DOCSIS system, the MAX3519 should be put in transmit-disable mode by setting TXEN low. The output transient on the cable is kept well below the DOCSIS requirement during the TXEN transitions.

If a gain or power change is required, new values of PC and GC should be clocked in during transmit-disable mode (TXEN low). The new operating point of the MAX3519 is set when $\overline{CS}$ transitions high during the time between bursts.

Output Transformer

The MAX3519 output circuits are open-collector differential amplifiers. On-chip resistors across the collectors provide a nominal output impedance of 75Ω in transmit mode and transmit-disable mode. To match the output of the MAX3519 to a single-ended 75Ω load, a 1:1 transformer is required. This transformer must have adequate bandwidth to cover the intended application. Note that some RF transformers specify bandwidth with a 50Ω source on the primary and a matching resistance on the secondary winding. Operating in a 75Ω system tends to shift the low-frequency edge of the transformer bandwidth specification up by a factor of 1.5 due to primary inductance. Keep this in mind when specifying a transformer.

Bias to the output stage is provided through the center tap on the transformer primary. This greatly diminishes the on/off transients present at the output when switching between transmit and transmit-disable modes. Commercially available transformers typically have adequate balance between half-windings to achieve substantial transient cancellation.

Finally, keep in mind that transformer core inductance varies with temperature. Adequate primary inductance must be present to sustain broadband output capability as temperatures vary.

Input Circuit

To achieve rated performance, the inputs of the MAX3519 must be driven differentially with an appropriate input level. The differential input impedance is 200Ω. Most applications require an anti-alias filter preceding the device. The filter should be designed to match this 200Ω impedance.

The MAX3519 has sufficient gain to produce an output level of +64dBmV QPSK when driven with a +33dBmV input signal. If an input level greater than +34dBmV is used, the 3rd-order distortion performance will degrade slightly.

Layout Issues

A well-designed printed circuit board (PCB) is an essential part of an RF circuit. For best performance, pay attention to power-supply layout issues as well as the output circuit layout. Please refer to the MAX3519 Evaluation kit documentation for detailed information regarding the recommended PCB layout and typical bill of materials.

No Connect Pins

Pins 11 and 18 must be left open, not connected to supply or ground or any other node in the circuit. Pins 9, 12, 15, 17, 19, and 20 should be connected to ground.

Output Circuit Layout

The differential implementation of the device output has the benefit of significantly reducing even-order distortion, the most significant of which is 2nd-harmonic distortion. The degree of distortion cancellation depends on the amplitude and phase balance of the overall circuit. It is important to keep the trace lengths from the output pins equal.

Power-Supply Layout

For minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the circuit. At the end of each of these traces is a decoupling capacitor that provides a very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin. The power-supply traces must be capable of carrying the maximum current without significant voltage drop.

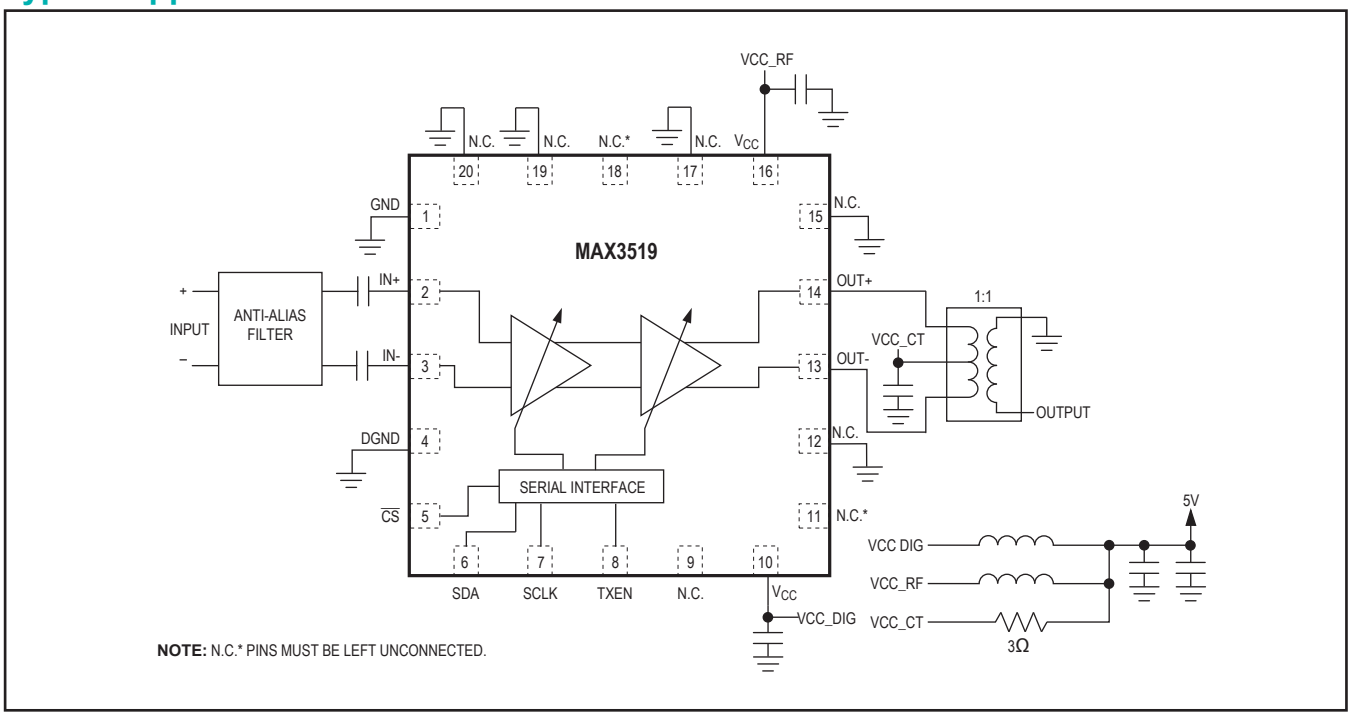
The output transformer center tap node, VCC_CT, must be connected to supply through a 3Ω resistor to reduce the supply voltage on OUT+ and OUT-. This resistor must be rated to dissipate 250mW at +85°C.

Exposed Pad Thermal Considerations

The exposed pad (EP) of the MAX3519's 20-pin TQFN package provides a low thermal resistance path to the die. It is important that the PCB on which the MAX3519 is mounted be designed to conduct heat from this contact. In addition, the EP should be provided with a low-inductance path to electrical ground.

It is recommended that the EP be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Typical Application Circuit



Chip Information

PROCESS: SiGe BiCMOS

Ordering Information

PART	TEMP RANGE	PIN PACKAGE
MAX3519ETP+	-40°C to +85°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+5	**21-0140**	**90-0010**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	1/16	Updated *Pin Description* table	7

