#### **ABSOLUTE MAXIMUM RATINGS**

V <sub>DD</sub> to GND LX to GND	
HDRV to LX	
BST to LX	0.3V to +6V
HI to GND	0.3V to +15V
dV/dt at LX	50V/ns
Peak Current into HDRV (< 100ns)	±2A
Continuous Current into HDRV	
Continuous Power Dissipation ( $T_A = +7$	0°C)
6-Pin SOT23 (derate 8.7mW/°C above	e +70°C)695.7mW

Thermal Resistance (Note 1)

Junction-to-Ambient Thermal Resistance (0JA)	115°C/W
Junction-to-Case Thermal Resistance $(\theta_{JC})$	80°C/W
Operating Temperature Range40°C to	) +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range65°C to	o +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations, refer to <u>www.maxim-ic.com/thermal-tutorial.</u>

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{DD} = V_{BST} = 5V, V_{LX} = V_{GND} = 0V, T_A = T_J = -40^{\circ}C$  to +125°C, unless otherwise noted. Typical values are at  $T_A = T_J = +25^{\circ}C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	COND	TIONS	MIN	ТҮР	MAX	UNITS
Operating Supply Voltage	V <sub>DD</sub>			4.6		5.5	V
V <sub>DD</sub> Quiescent Supply Current	I <sub>DD</sub>	No switching		40	75	μA	
BST Quiescent Supply Current	I <sub>BST</sub>	No switching			65	125	μA
BST Operating Supply Current	I <sub>BSTO</sub>	f <sub>SW</sub> = 500kHz, no loa	.d		0.3	1.3	mA
V <sub>DD</sub> Undervoltage Lockout Threshold	V <sub>DD_UVLO</sub>	V <sub>DD</sub> rising		3.92	4.22	4.56	V
V <sub>DD</sub> Undervoltage Lockout Threshold Hysteresis					0.2		V
BST-to-LX Undervoltage Lockout Threshold	V <sub>BST_</sub> UVLO	BST rising		3.54	3.82	4.1	V
BST-to-LX Undervoltage Lockout Threshold Hysteresis					0.2		V
LOGIC INPUT (HI)							
HI Logic-High Threshold	V <sub>IH</sub>			3.9			V
HI Logic-Low Threshold	VIL					1.8	V
HI Logic-Input Hysteresis					0.9		V
HI Input Current	I <sub>IN</sub>	HI = GND		-2		+2	μA
HI Input Resistance	R <sub>IN</sub>				300		kΩ
DRIVER							
LX Withstand Voltage	V <sub>LX_MAX</sub>					60	V
BST Withstand Voltage	V <sub>BST_MAX</sub>					65	V
LX Pulldown Current		$V_{LX} = 2.5V$		500	740	1100	μA
Driver Output Resistance (Sourcing)	R <sub>ON_HP</sub>	V <sub>BST</sub> - V <sub>LX</sub> = 4.5V, 100mA sourcing	$T_A = +25^{\circ}C$ $T_A = +125^{\circ}C$		1 1.25	1.5 2	Ω
Driver Output Resistance (Sinking)	R <sub>ON_HN</sub>	$V_{BST} - V_{LX} = 4.5V,$ 100mA sinking	$T_A = +25^{\circ}C$ $T_A = +125^{\circ}C$		0.75	1	Ω

2

#### ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = V_{BST} = 5V, V_{LX} = V_{GND} = 0V, T_A = T_J = -40^{\circ}C$  to +125°C, unless otherwise noted. Typical values are at T\_A = T\_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS	
Peak Output Current (Sourcing)	I <sub>PK_HP</sub>	V <sub>HDRV</sub> = 0V		2.5		A	
Peak Output Current (Sinking)	I <sub>PK_HN</sub>	V <sub>HDRV</sub> = 5V		2.5		A	
SWITCHING CHARACTERISTICS							
Rise Time	t <sub>R</sub>	No-load capacitor		1.5			
		$C_{L} = 1000 pF$	6			ns	
		C <sub>L</sub> = 5000pF		18		]	
		No-load capacitor		1.5			
Fall Time	tF	C <sub>L</sub> = 1000pF	6			ns	
		$C_{L} = 5000 pF$		16		]	
Turn-On Propagation Delay	t <sub>D_ON</sub>	Figure 1, C <sub>L</sub> = 1000pF (Note 3)		11	25	ns	
Turn-Off Propagation Delay	tD_OFF	Figure 1, C <sub>L</sub> = 1000pF (Note 3)		11	25	ns	

Note 2: All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design.

Note 3: Guaranteed by design.

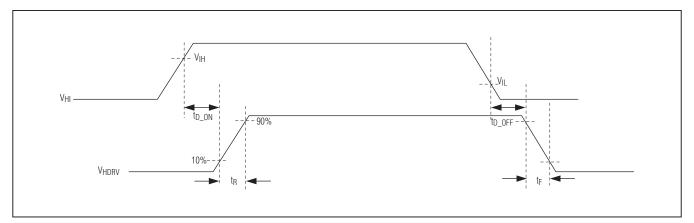
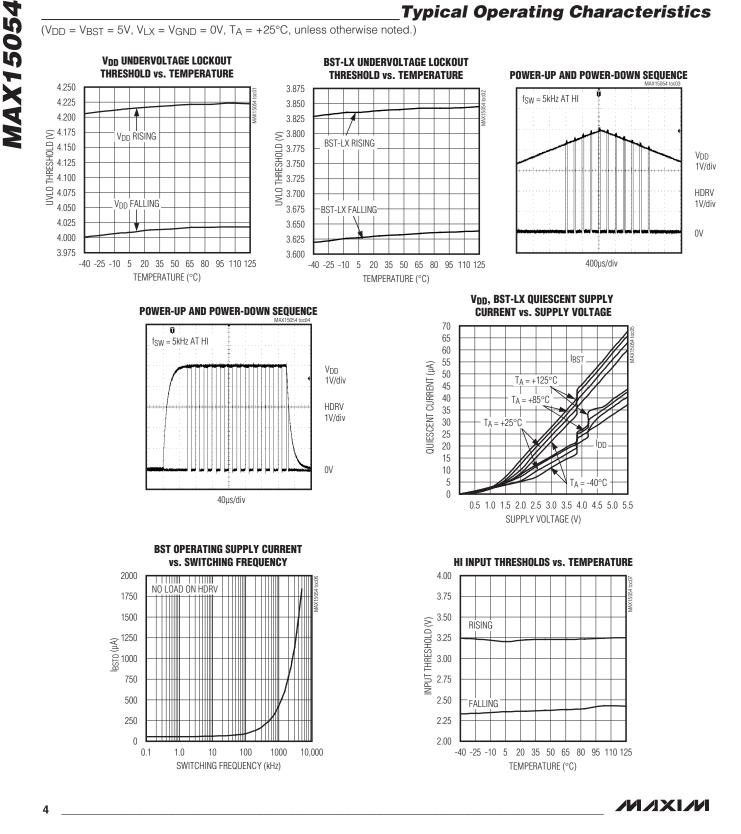
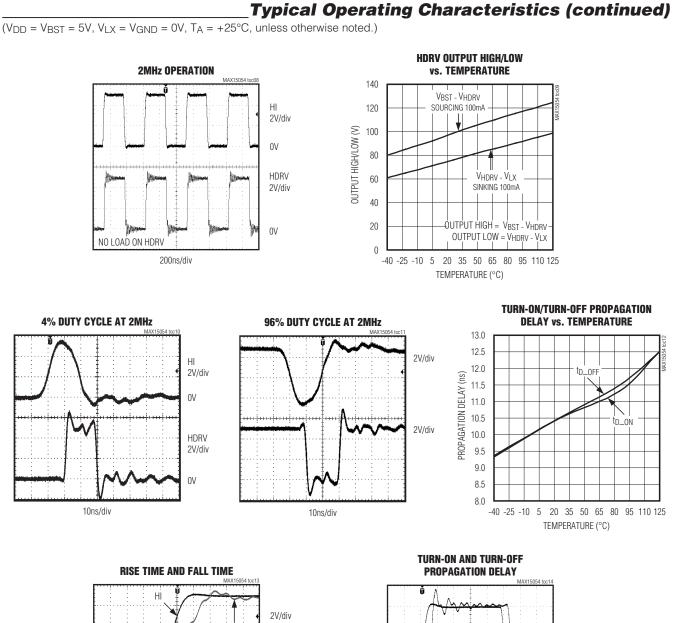


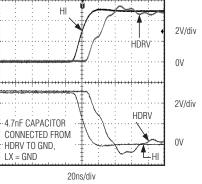
Figure 1. Turn-On/Turn-Off Propagation Delay

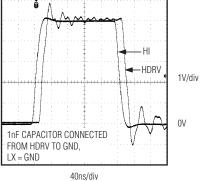
**Typical Operating Characteristics** 

 $(V_{DD} = V_{BST} = 5V, V_{LX} = V_{GND} = 0V, T_A = +25^{\circ}C, unless otherwise noted.)$ 







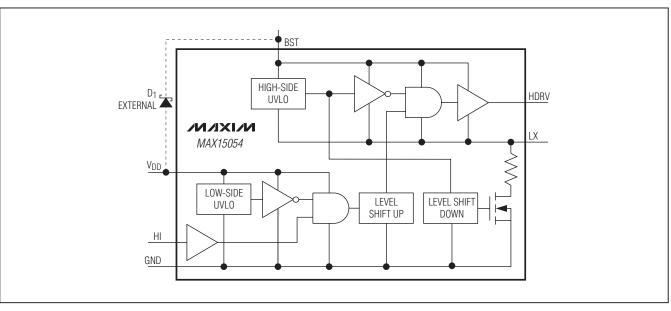


MAX15054

**Pin Description** 

**Functional Diagram** 

PIN	NAME	FUNCTION			
1	н	5V CMOS Logic Input. HI is referenced to GND and is capable of withstanding voltages up to 13.5V for any $V_{DD}$ voltage.			
2	GND	Ground			
3	V <sub>DD</sub>	Input Supply Voltage. Valid supply voltage ranges from 4.6V to 5.5V. Bypass $V_{DD}$ to GND with a 0.1 $\mu$ F ceramic capacitor as close as possible to the device.			
4	BST	Boost Flying Capacitor Connection. Connect a minimum of a $0.1\mu$ F ceramic capacitor between BST and LX for the high-side MOSFET driver supply. Connect a bootstrap Schottky diode between V <sub>DD</sub> and BST.			
5	HDRV	High-Side Gate-Driver Output. Driver output to drive the high-side external MOSFET gate.			
6	LX	Source Connection for High-Side MOSFET. LX also serves as a return terminal for the high-side driver.			



### **Detailed Description**

The MAX15054 n-channel MOSFET driver controls an external high-side MOSFET in high-voltage, high-current applications. This driver operates with a supply voltage of 4.6V to 5.5V, and consumes only 300µA of supply current during typical switching operations ( $f_{SW} = 500 \text{kHz}$ ) and no-load conditions. The MAX15054 provides 2.5A (typ) sink/source peak current and is capable of operating with large capacitive loads and with switching frequencies up to 2MHz. The device is used to drive the high-side MOSFET without requiring an isolation device such as an optocoupler or a drive transformer.

The high-side driver is controlled by a CMOS logic referenced to ground and is powered by a bootstrap circuit formed by an external diode and capacitor. Undervoltage lockout (UVLO) protection is provided for both the high- and low-side driver supplies (BST and VDD) and includes a UVLO hysteresis of 0.2V (typ).

The MAX15054's fast switching times and very short propagation delays (11ns, typ) are ideal for highfrequency applications. Internal logic circuitry prevents shoot-through during output state changes and minimizes package power dissipation.

6

**MAX15054** 

#### Undervoltage Lockout

The MAX15054 drives an external high-side MOSFET. Both the high- and low-side supplies feature separate UVLO protection that monitors each driver's input supply voltage (BST-LX and V<sub>DD</sub>). The low-side supply UVLO threshold (V<sub>DD</sub>\_UVLO) is referenced to GND and pulls the driver output low when V<sub>DD</sub> falls below 4V (typ) irrespective of the high-side UVLO condition.

The high-side driver UVLO threshold (VBST\_UVLO) is referenced to LX, and pulls HDRV low when VBST falls below 3.6V (typ) with respect to LX. After the MAX15054 is first energized (VDD > VDD\_UVLO), the bootstrap capacitor (CBST) between BST and LX is not charged, and HDRV does not switch since the BST-to-LX voltage is below VBST\_UVLO. An internal charging circuit charges the BST-LX supply through an external Schottky diode and within a short time CBST charges through VDD and causes VBST to exceed VBST\_UVLO. HDRV then starts switching and follows HI. The hysteresis is 0.2V (typ) for both UVLO thresholds.

**Output Driver** The MAX15054 driver contains low on-resistance p-channel and n-channel devices in a totem pole configuration for the driver output stage. This allows for rapid turn-on and turn-off of high gate-charge (Qg) external switching MOSFETs. The driver exhibits low drain-to-source resistance (RDS(ON)) that decreases for lower operating temperatures. Lower RDS(ON) means higher source and sink currents from the device as the external MOSFET gate capacitance charges and discharges at a quicker rate, resulting in faster switching speeds. The peak source and sink current provided by the driver is 2.5A (typ).

Propagation delay from the logic input (HI) to the driver output is 12ns (typ) (Figure 1). The internal driver also contains break-before-make logic to eliminate shootthrough conditions that cause unnecessarily high operating supply currents, efficiency reduction, and voltage spikes at VDD.

Voltage from HDRV to LX is approximately equal to V<sub>DD</sub> minus the diode drop of the bootstrap diode when in a high state, and zero when in a low state.

#### **Bootstrap Diode**

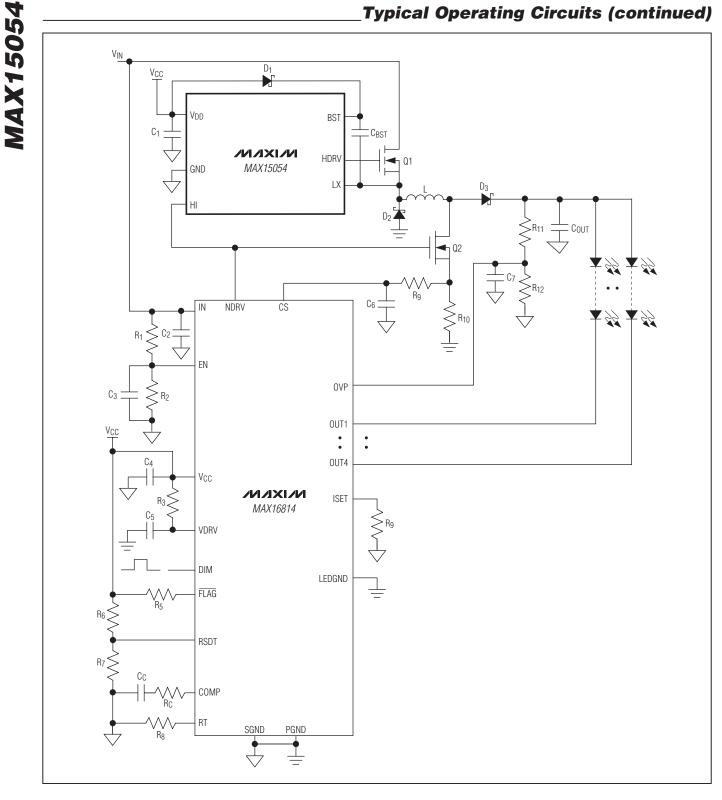
Connect an external Schottky diode between V<sub>DD</sub> and BST, in conjunction with an external bootstrap capacitor (C<sub>BST</sub>), to provide the voltage required to turn on the MOSFET (see the *Typical Operating Circuits*). The diode charges the bootstrap capacitor from V<sub>DD</sub> when the high-side switch is off, and isolates V<sub>DD</sub> when HDRV is pulled high when the driver turns on.

#### **Bootstrap Capacitor**

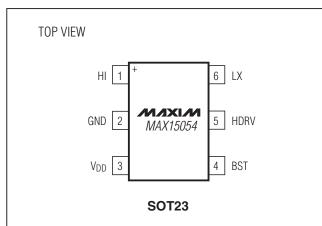
The bootstrap capacitor (C<sub>BST</sub>) between BST and LX is used to ensure adequate charge is available to switch the high-side MOSFET. This capacitor is charged from V<sub>DD</sub> by an external bootstrap diode when the MOSFET is off. The bootstrap capacitor value should be selected carefully to avoid oscillations during turn-on and turnoff at the HDRV output. Choose a capacitor value at least 20 times greater than the total gate capacitance of the MOSFET being switched. Use a low-ESR ceramic capacitor (typically a minimum  $0.1\mu$ F is needed). The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of C<sub>BST</sub>, I<sub>BST</sub> (125µA, max), and V<sub>BST\_UVLO</sub>.

#### Driver Logic Input (HI)

The MAX15054 features a 5V CMOS logic input. The required logic-input levels are independent of V<sub>DD</sub> and are capable of withstanding up to 13.5V. For example, the MAX15054 can be powered by a 5V supply while the logic inputs are provided from 12V logic. Additionally, HI is protected against voltage spikes up to 15V, regardless of the V<sub>DD</sub> voltage. The logic input has 900mV hysteresis to avoid double pulsing during signal transition. The logic input is a high-impedance input ( $300k\Omega$ , typ) and should not be left unconnected to ensure the input logic state is at a known level. With the logic input unconnected, HDRV pulls low as V<sub>DD</sub> rises above the UVLO threshold. The PWM output from the controller must assume a proper state while powering up the device.



8



#### Pin Configuration

\_Chip Information

**MAX15054** 

PROCESS: BICMOS

### \_Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** 

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SOT23	U6+1	<u>21-0058</u>

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 \_

© 2009 Maxim Integrated Products