ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- V_{DD}, OV_{DD} ..... –0.3V to 2V
- V_{CC} ..... –0.3V to 5.5V

Analog Input Voltage (CHn^+, CHn^-, $\overline{SHDNn}$) (Note 3) ..... –0.3V to V_{CC}

Analog Input Voltage (PAR/$\overline{SER}$, SENSE) (Note 4) ..... –0.3V to (V_{DD} + 0.2V)

Digital Input Voltage (ENC$^+$, ENC$^-$, $\overline{CS}$, SDI, SCK) (Note 5) ..... –0.3V to 3.9V

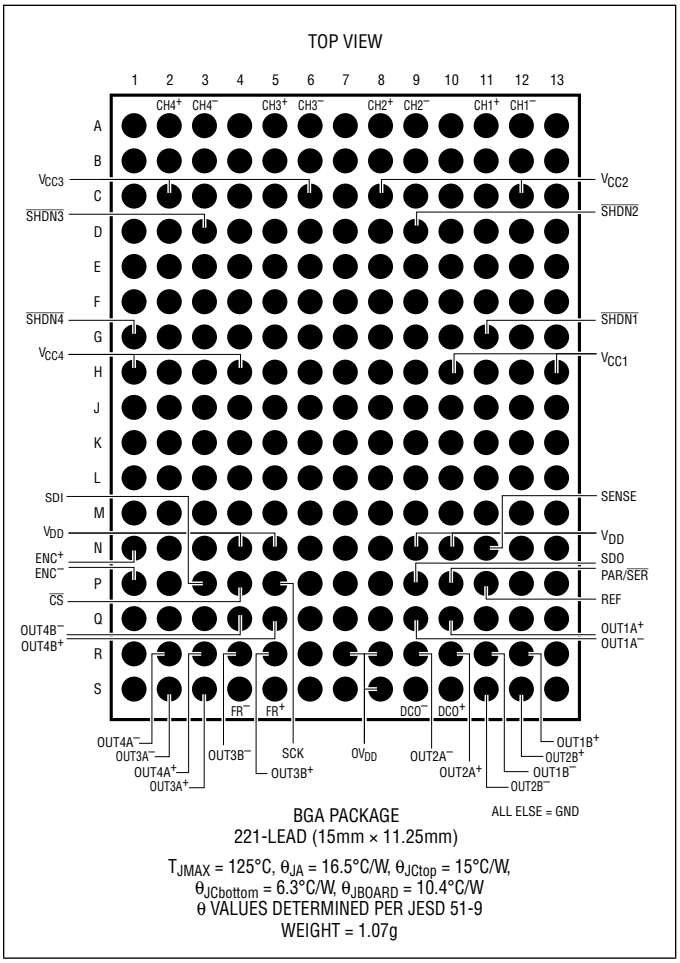
SDO (Note 5) ..... –0.3V to 3.9V

Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)

Operating Temperature Range
- LTM9012C ..... 0°C to 70°C
- LTM9012I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

http://www.linear.com/product/LTM9012#orderinfo

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9012CY-AB#PBF	LTM9012CY-AB#PBF	LTM9012YAB	221-Lead (15mm × 11.25mm) Plastic BGA	0°C to 70°C
LTM9012IY-AB#PBF	LTM9012IY-AB#PBF	LTM9012YAB	221-Lead (15mm × 11.25mm) Plastic BGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	Differential Analog Input (Note 7)	●	–5	±1.2	5	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.3	0.9	LSB
Offset Error	(Note 8)	●	–37	±3	37	mV
Gain Error	Internal Reference External Reference	 ●	 –3.6	–1.3 –1.3	 3.0	%FS %FS
Offset Drift				±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±35 ±25		ppm/°C ppm/°C
Gain Matching	External Reference			±0.2		%FS
Offset Matching				±3		mV
Transition Noise	External Reference			1.2		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Differential Analog Input Range ($CH^+ – CH^-$) at –1dBFS	LTM9012-AB	●		0.2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($CH^+ + CH^-$)/2	Differential Analog Input (Note 9)			0 to 1.5		V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
R_{IN}	Differential Input Resistance	LTM9012-AB			100		Ω
$I_{IN(P/S)}$	Input Leakage Current	$0 < PAR/\overline{SER} < V_{DD}$	●	–3		3	µA
$I_{IN(SENSE)}$	Input Leakage Current	0.625V < SENSE < 1.3V	●	–6		6	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.15		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				90		dB
BW-3dB	3dB Corner of Internal Lowpass Filter				90		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	70MHz Input	●	66.5	68.3		dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	70MHz Input	●	66.9	78		dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	70MHz Input	●	76.9	86		dBFS
S/N+D	Signal-to-Noise Plus Distortion Ratio	70MHz Input	●	64.7	66.7		dBFS
	Crosstalk, Near Channel	10MHz (Note 12)			70		dBc
	Crosstalk, Far Channel	10MHz (Note 12)			90		dBc

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INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		1.225	1.250	1.275	V
V_{REF} Output Temperature Drift				±25		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA			7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V			0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC+, ENC–)							
Differential Encode Mode (ENC– Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 9)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 9)	 ●	 1.1	1.2	 1.6	V V
V_{IN}	Input Voltage Range	ENC+, ENC– to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 3)			10		kΩ
C_{IN}	Input Capacitance				3.5		pF
Single-Ended Encode Mode (ENC– Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V			1.26		V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V			0.54		V
V_{IN}	Input Voltage Range	ENC+ to GND			0 to 3.6		V
R_{IN}	Input Resistance	(See Figure 4)			30		kΩ
C_{IN}	Input Capacitance				3.5		pF
Digital Inputs ($\overline{CS}$, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance				3		pF
SDO Output (Serial Programming Mode. Open-Drain Output. Requires 2k Pull-Up Resistor if SDO is Used)							
R_{OH}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance				3		pF
Digital Input ($\overline{SHDN}$)							
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V	●		0.97	1.4	V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.3V	●	0.6	0.95		V
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	$V_{\overline{SHDN}}$ = 0V to 0.5V	●	90	150	210	kΩ
Digital Data Outputs							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	247 125	350 175	454 250	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	1.125 1.125	1.250 1.250	1.375 1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

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POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	ADC Supply Voltage	(Note 10)	●	1.7	1.8	1.9	V
OV_{DD}	ADC Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	V
V_{CC}	Amplifier Supply Voltage	(Note 10)	●	2.7	3.3	3.6	V
I_{VDD}	ADC Supply Current	Sine Wave Input	●		298	320	mA
I_{OVDD}	ADC Output Supply Current	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode	● ●		27 49	31 54	mA mA
I_{VCC}	Amplifier Supply Current		●		208	224	mA
P_{DISS}		2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode	● ●		1271 1311	1473 1517	mW mW
P_{SLEEP}					3		mW
P_{NAP}					85		mW
$P_{DIFFCLK}$	Power Decrease with Single-Ended Encode Mode Enabled				20		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 10, Note 11)	●	5		125	MHz
t_{ENCL}	ENC Low Time (Note 9)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	ns ns
t_{ENCH}	ENC High Time (Note 9)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	ns ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
Digital Data Outputs (R_{TERM} = 100Ω Differential, C_L = 2pF to GND on Each Output)							
t_{SER}	Serial Data Bit Period	2-Lanes, 16-Bit Serialization 2-Lanes, 14-Bit Serialization 2-Lanes, 12-Bit Serialization 1-Lane, 16-Bit Serialization 1-Lane, 14-Bit Serialization 1-Lane, 12-Bit Serialization			$1/(8•f_S)$ $1/(7•f_S)$ $1/(6•f_S)$ $1/(16•f_S)$ $1/(14•f_S)$ $1/(12•f_S)$		sec sec sec sec sec sec
t_{FRAME}	FR to DCO Delay	(Note 9)	●	$0.35•t_{SER}$	$0.5•t_{SER}$	$0.65•t_{SER}$	sec
t_{DATA}	DATA to DCO Delay	(Note 9)	●	$0.35•t_{SER}$	$0.5•t_{SER}$	$0.65•t_{SER}$	sec
t_{PD}	Propagation Delay	(Note 9)	●	$0.7n + 2•t_{SER}$	$1.1n + 2•t_{SER}$	$1.5n + 2•t_{SER}$	sec
t_R	Output Rise Time	Data, DCO, FR, 20% to 80%			0.17		ns
t_F	Output Fall Time	Data, DCO, FR, 20% to 80%			0.17		ns
	DCO Cycle-Cycle Jitter	t_{SER} = 1ns			60		ps_{P-P}
	Pipeline Latency				6		Cycles
SPI Port Timing (Note 9)							
t_{SCK}	SCK Period	Write Mode Read Back Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Read Back Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

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ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND (unless otherwise noted).

Note 3: Input pins are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs CH*n*$^+$, CH*n*$^-$ are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 4: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below GND or above V_{DD} without latchup.

Note 5: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents greater than 100mA below GND without latchup.

Note 6: V_{CC} = 3.3V, V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz, 2-lane output mode, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $200mV_{P-P}$ with differential drive, unless otherwise noted.

Note 7: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

Note 9: Guaranteed by design, not subject to test.

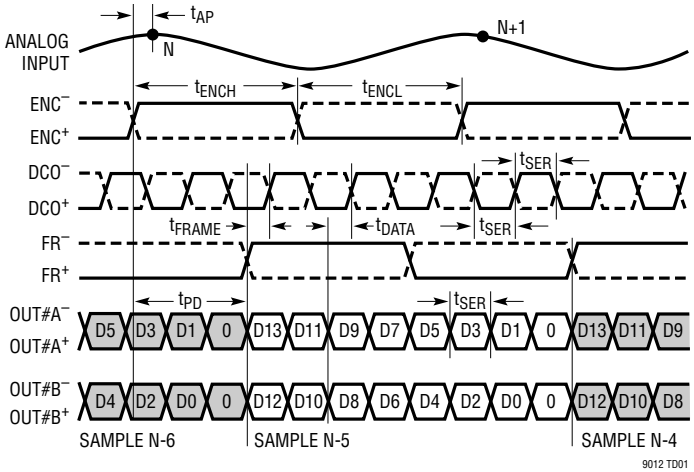
Note 10: Recommended operating conditions.

Note 11: The maximum sampling frequency depends on the speed grade of the part and also which serialization mode is used. The maximum serial data rate is 1000Mbps so t_{SER} must be greater than or equal to 1ns.

Note 12: Near-channel crosstalk refers to CH1 and CH2. Far channel crosstalk refers to CH1 to CH4.

TIMING DIAGRAMS

2-Lane Output Mode, 16-Bit Serialization*



*SEE THE DIGITAL OUTPUTS SECTION

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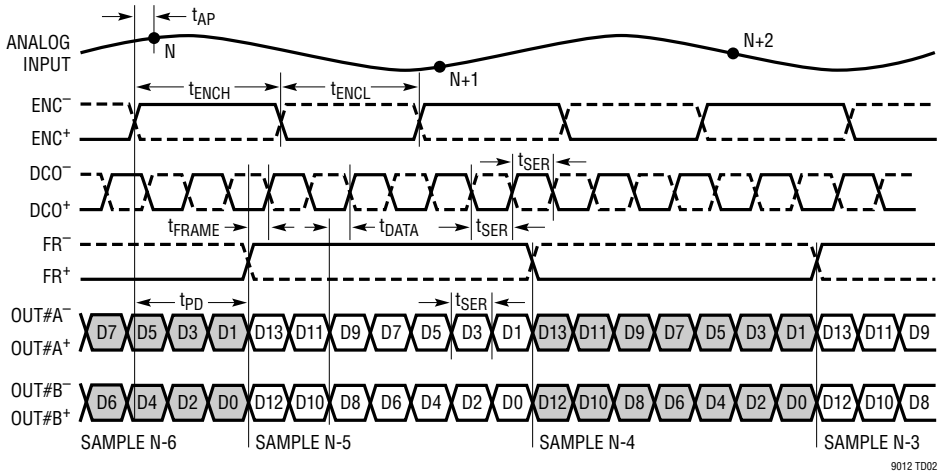
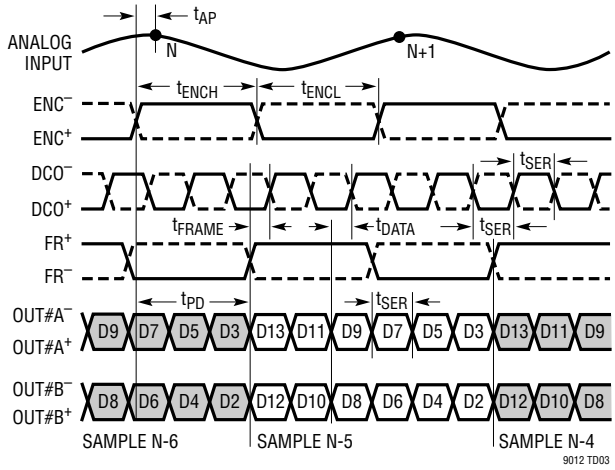
TIMING DIAGRAMS

2-Lane Output Mode, 14-Bit Serialization



NOTE THAT IN THIS MODE FR+/FR– HAS TWO TIMES THE PERIOD OF ENC+/ENC–

2-Lane Output Mode, 12-Bit Serialization



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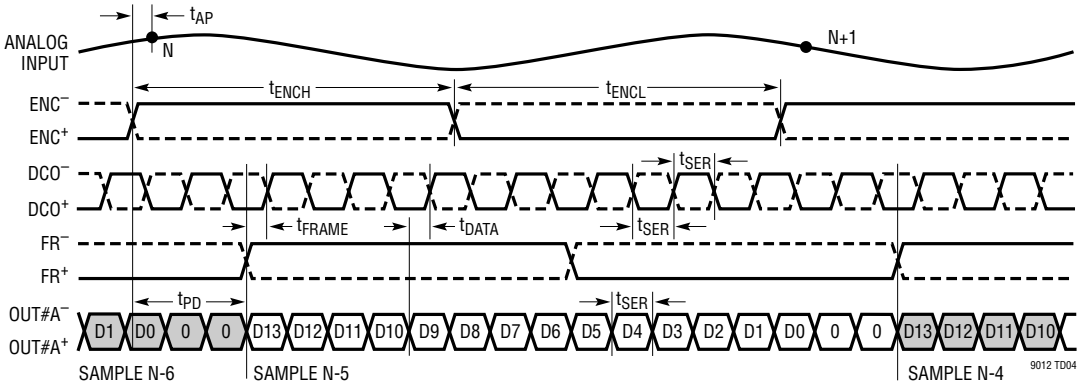
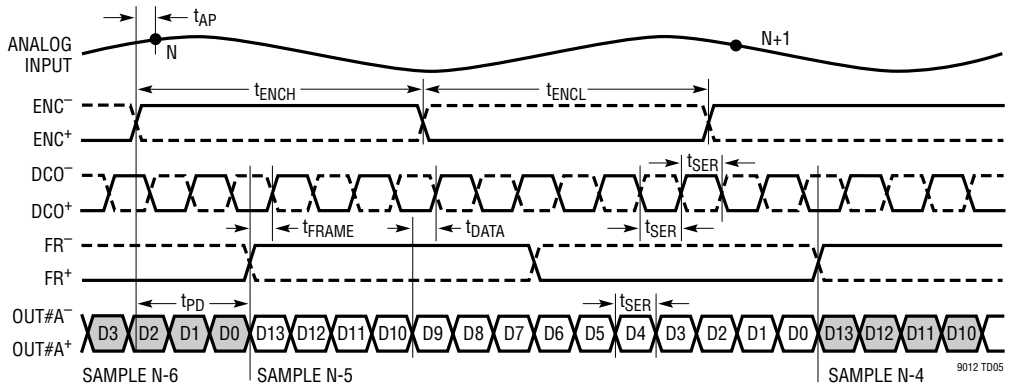
TIMING DIAGRAMS

1-Lane Output Mode, 16-Bit Serialization



OUT#B+, OUT#B– ARE DISABLED

1-Lane Output Mode, 14-Bit Serialization



OUT#B+, OUT#B– ARE DISABLED

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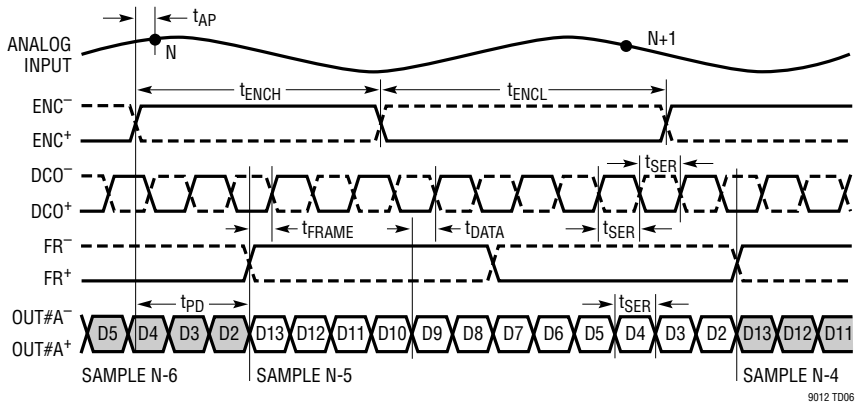
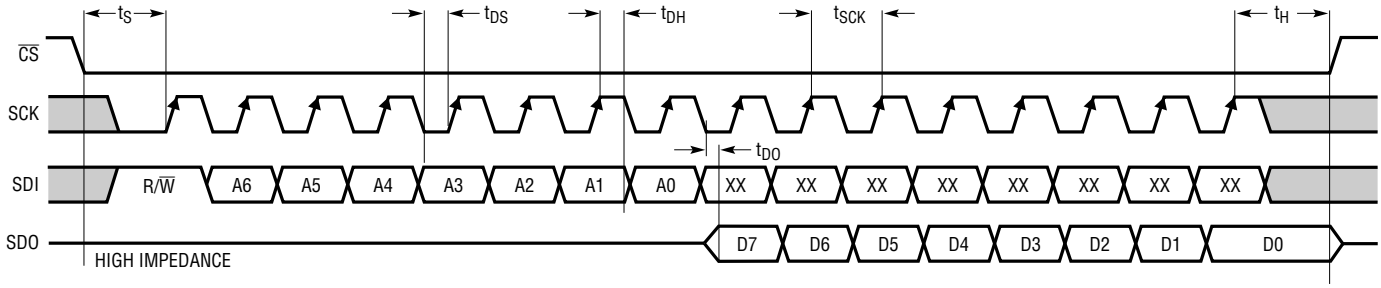
TIMING DIAGRAMS

1-Lane Output Mode, 12-Bit Serialization

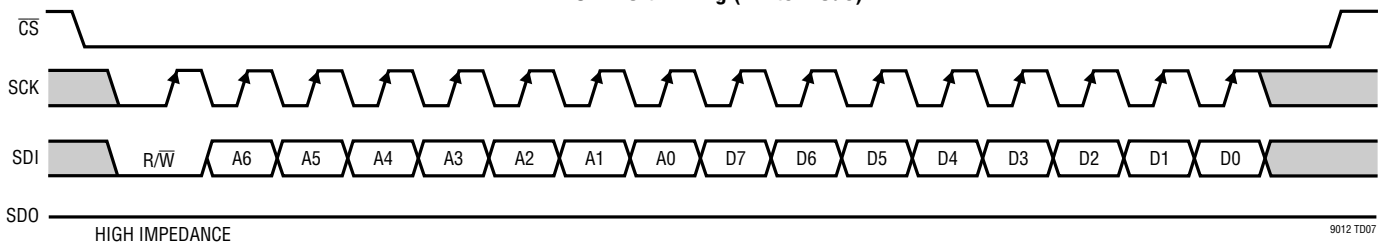


OUT#B+, OUT#B– ARE DISABLED

SPI Port Timing (Readback Mode)



SPI Port Timing (Write Mode)



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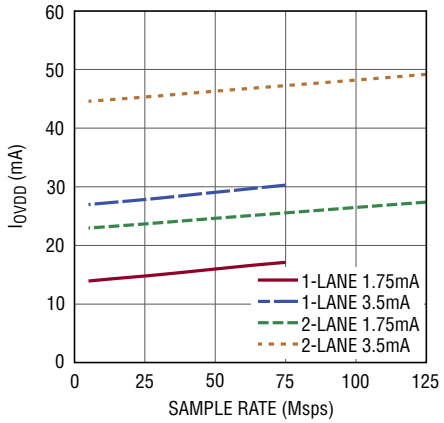
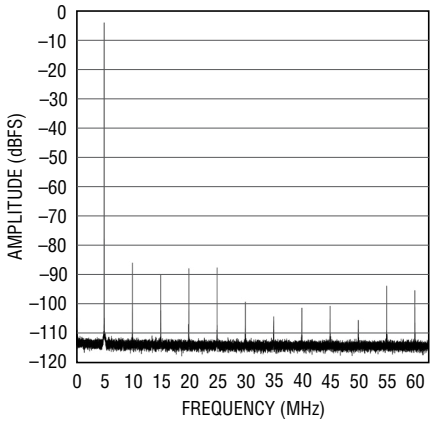
TYPICAL PERFORMANCE CHARACTERISTICS

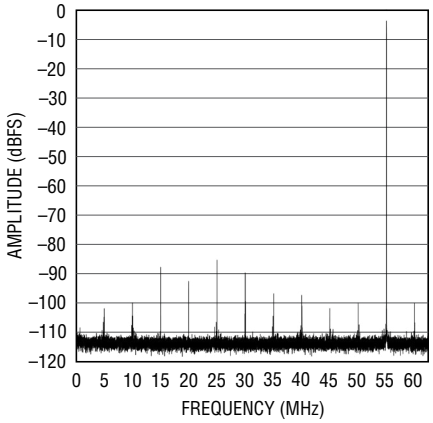
I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input –1dBFS



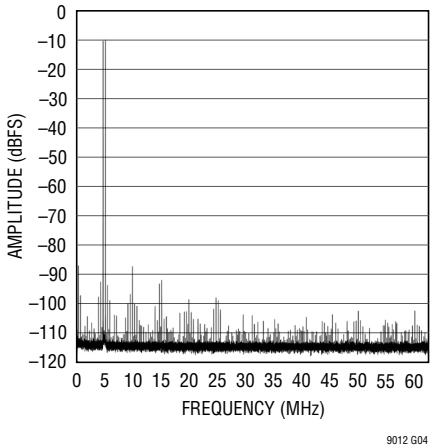
64K Point FFT, f_{IN} = 5MHz, –1dBFS, SENSE = V_{DD}



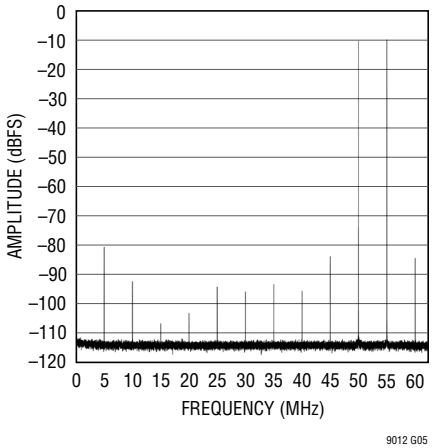
64K Point FFT, f_{IN} = 70MHz, –1dBFS, SENSE = V_{DD}



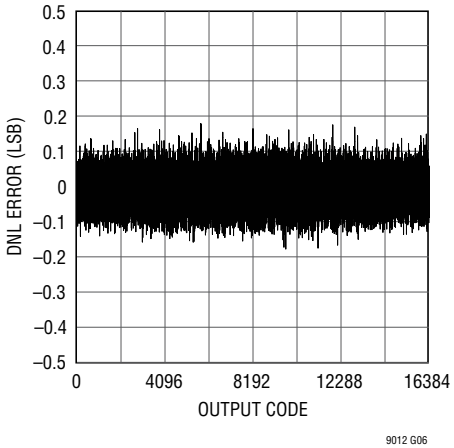
64K Point 2-Tone FFT, f_{IN} = 4.8MHz and f_{IN} = 5.2MHz, –7dBFS per Tone, SENSE = V_{DD}



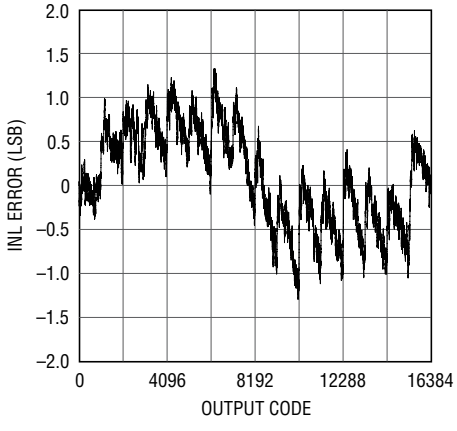
64K Point 2-Tone FFT, f_{IN} = 70MHz and f_{IN} = 75MHz, –7dBFS per Tone, SENSE = V_{DD}



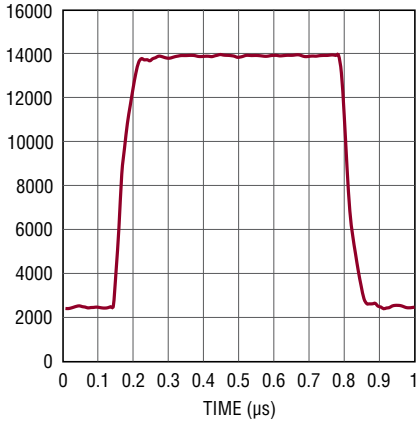
Differential Non-Linearity (DNL) vs Output Code



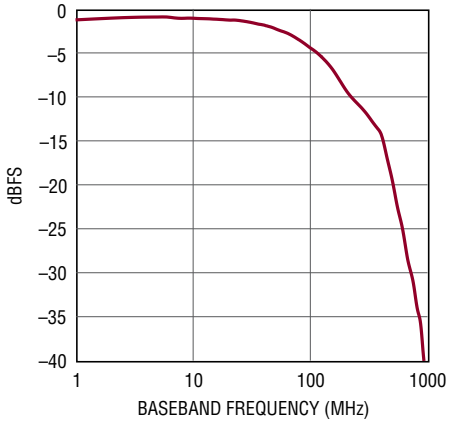
Integral Non-Linearity (INL) vs Output Code



Pulse Response



Frequency Response



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PIN FUNCTIONS

V_{CC1} (H10, H13): Channel 1 Amplifier Supply. V_{CC} is internally bypassed to ground with 0.1µF in parallel with 0.01µF ceramic capacitors, additional bypass capacitance is optional. The recommended operating voltage is 3.3V.

V_{CC2} (C8, C12): Channel 2 Amplifier Supply. V_{CC} is internally bypassed to ground with 0.1µF in parallel with 0.01µF ceramic capacitors, additional bypass capacitance is optional. The recommended operating voltage is 3.3V.

V_{CC3} (C2, C6): Channel 3 Amplifier Supply. V_{CC} is internally bypassed to ground with 0.1µF in parallel with 0.01µF ceramic capacitors, additional bypass capacitance is optional. The recommended operating voltage is 3.3V.

V_{CC4} (H1, H4): Channel 4 Amplifier Supply. V_{CC} is internally bypassed to ground with 0.1µF in parallel with 0.01µF ceramic capacitors, additional bypass capacitance is optional. The recommended operating voltage is 3.3V.

V_{DD} (N4, N5, N9, N10): ADC Analog Supply. V_{DD} is internally bypassed to ground with 0.1µF ceramic capacitors, additional bypass capacitance is optional. The recommended operating voltage is 1.8V.

OV_{DD} (R7, R8, S8): ADC Digital Output Supply. OV_{DD} is internally bypassed to ground with 0.1µF ceramic capacitors, additional bypass capacitance is optional. The recommended operating voltage is 1.8V.

GND: Ground. Use multiple vias close to pins.

$CH1^+$ (A11): Channel 1 Noninverting Analog Input.

$CH1^-$ (A12): Channel 1 Inverting Analog Input.

$CH2^+$ (A8): Channel 2 Noninverting Analog Input.

$CH2^-$ (A9): Channel 2 Inverting Analog Input.

$CH3^+$ (A5): Channel 3 Noninverting Analog Input.

$CH3^-$ (A6): Channel 3 Inverting Analog Input.

$CH4^+$ (A2): Channel 4 Noninverting Analog Input.

$CH4^-$ (A3): Channel 4 Inverting Analog Input.

$\overline{SHDN1}$ (G11): Channel 1 Amplifier Shutdown. Connecting $\overline{SHDN1}$ to V_{CC} or floating results in normal (active) operating mode. Connecting $\overline{SHDN1}$ to GND results in a low power shutdown state on amplifier 1.

$\overline{SHDN2}$ (D9): Channel 2 Amplifier Shutdown. Connecting $\overline{SHDN2}$ to V_{CC} or floating results in normal (active) operating mode. Connecting $\overline{SHDN2}$ to GND results in a low power shutdown state on amplifier 2.

$\overline{SHDN3}$ (D3): Channel 3 Amplifier Shutdown. Connecting $\overline{SHDN3}$ to V_{CC} or floating results in normal (active) operating mode. Connecting $\overline{SHDN3}$ to GND results in a low power shutdown state on amplifier 3.

$\overline{SHDN4}$ (G1): Channel 4 Amplifier Shutdown. Connecting $\overline{SHDN4}$ to V_{CC} or floating results in normal (active) operating mode. Connecting $\overline{SHDN4}$ to GND results in a low power shutdown state on amplifier 4.

ENC^+ (N1): Encode Input. Conversion starts on the rising edge.

ENC^- (P1): Encode Complement Input. Conversion starts on the falling edge.

$\overline{CS}$ (P4): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$ is the serial interface chip select input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ selects 2-lane or 1-lane output mode. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

SCK (P5): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK selects 3.5mA or 1.75mA LVDS output currents. SCK can be driven with 1.8V to 3.3V logic.

SDI (P3): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDI is the serial interface data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power down the part. SDI can be driven with 1.8V to 3.3V logic.

SDO (P9): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V – 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDO is an input that enables internal 100Ω termination resistors. When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

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PIN FUNCTIONS

PAR/$\overline{\text{SER}}$ (P10): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{\text{CS}}$, SCK, SDI and SDO become a serial interface that controls the A/D operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{\text{CS}}$, SCK, SDI and SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{\text{SER}}$ should be connected directly to ground or the V_{DD} of the part and not be driven by a logic signal.

V_{REF} (P11): Reference Voltage Output. V_{REF} is internally bypassed to ground with a 2.2µF ceramic capacitor, nominally 1.25V.

SENSE (N11): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±0.1V input range. Connecting SENSE to ground selects the internal reference and a ±0.05V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of ±0.08 • V_{SENSE}. SENSE is internally bypassed to ground with a 0.1µF ceramic capacitor.

LVDS Outputs

All pins in this section are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

OUT1A$^-$/OUT1A$^+$, OUT1B$^-$/OUT1B$^+$ (Q9/Q10, R11/R12): Serial data outputs for Channel 1. In 1-lane output mode only OUT1A$^-$/OUT1A$^+$ are used.

OUT2A$^-$/OUT2A$^+$, OUT2B$^-$/OUT2B$^+$ (R9/R10, S11/S12): Serial data outputs for Channel 2. In 1-lane output mode only OUT2A$^-$/OUT2A$^+$ are used.

OUT3A$^-$/OUT3A$^+$, OUT3B$^-$/OUT3B$^+$ (S2/S3, R4/R5): Serial data outputs for Channel 3. In 1-lane output mode only OUT3A$^-$/OUT3A$^+$ are used.

OUT4A$^-$/OUT4A$^+$, OUT4B$^-$/OUT4B$^+$ (R2/R3, Q4/Q5): Serial data outputs for Channel 4. In 1-lane output mode only OUT4A$^-$/OUT4A$^+$ are used.

FR$^-$/FR$^+$ (S4/S5): Frame Start Output.

DCO$^-$/DCO$^+$ (S9/S10): Data Clock Output.

PIN CONFIGURATION TABLE

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	CH4$^+$	CH4$^-$	GND	CH3$^+$	CH3$^-$	GND	CH2$^+$	CH2$^-$	GND	CH1$^+$	CH1$^-$	GND
B	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
C	GND	V_{CC3}	GND	GND	GND	V_{CC3}	GND	V_{CC2}	GND	GND	GND	V_{CC2}	GND
D	GND	GND	$\overline{\text{SHDN3}}$	GND	GND	GND	GND	GND	$\overline{\text{SHDN2}}$	GND	GND	GND	GND
E	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
G	$\overline{\text{SHDN4}}$	GND	GND	GND	GND	GND	GND	GND	GND	GND	$\overline{\text{SHDN1}}$	GND	GND
H	V_{CC4}	GND	GND	V_{CC4}	GND	GND	GND	GND	GND	V_{CC1}	GND	GND	V_{CC1}
J	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
K	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
L	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
M	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
N	ENC$^+$	GND	GND	V_{DD}	V_{DD}	GND	GND	GND	V_{DD}	V_{DD}	SENSE	GND	GND
P	ENC–	GND	SDI	$\overline{\text{CS}}$	SCK	GND	GND	GND	SDO	PAR/$\overline{\text{SER}}$	REF	GND	GND
Q	GND	GND	GND	OUT4B$^-$	OUT4B$^+$	GND	GND	GND	OUT1A$^-$	OUT1A$^+$	GND	GND	GND
R	GND	OUT4A$^-$	OUT4A$^+$	OUT3B$^-$	OUT3B$^+$	GND	OVDD	OVDD	OUT2A$^-$	OUT2A$^+$	OUT1B$^-$	OUT1B$^+$	GND
S	GND	OUT3A$^-$	OUT3A$^+$	FR$^-$	FR$^+$	GND	GND	OVDD	DCO$^-$	DCO$^+$	OUT2B$^-$	OUT2B$^+$	GND

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BLOCK DIAGRAM

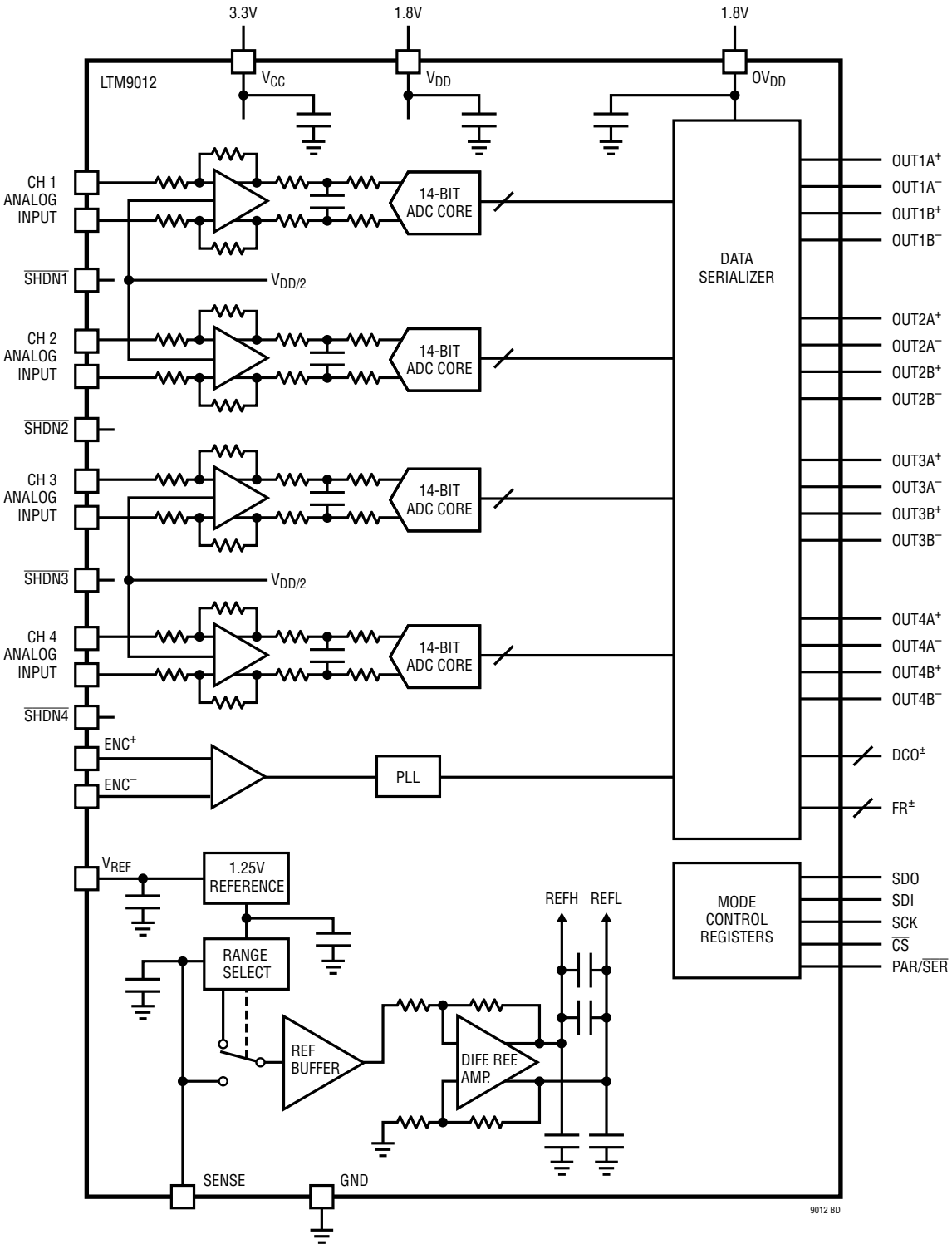

Figure 1. Block Diagram

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APPLICATIONS INFORMATION

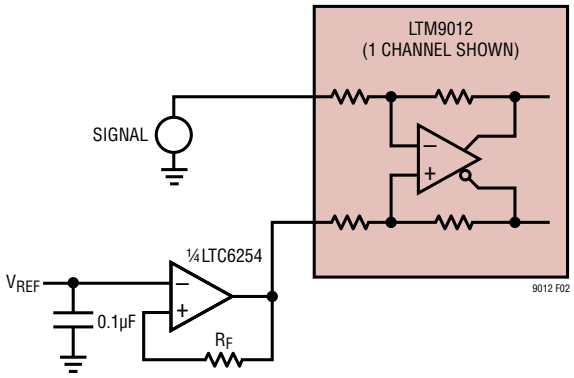
CONVERTER OPERATION

The LTM9012 is a low power, 4-channel, 14-bit, 125Msps A/D converter that is powered by a 1.8V ADC supply and 3.3V driver supplies. Each input includes a fixed gain, differential amplifier. The analog inputs can be driven differentially or single-ended. The encode input can be driven differentially for optimal jitter performance, or single-ended for lower power consumption. The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). Many additional features can be chosen by programming the mode control registers through a serial SPI port.

Analog Inputs

The analog inputs for each channel of the LTM9012 consist of a differential amplifier with fixed gain followed by a lowpass filter. The 10x gain version has 49.9Ω series resistance in each input.

The differential input can support single-ended operation by connecting the inverting input to a fixed DC voltage or ground. However, if ground is used, there will be a 6dB loss of dynamic range. For maximum dynamic range, connect the inverting inputs of the LTM9012 to a DC voltage equal to the median of the voltage excursions of the non-inverting input. An op amp provides an excellent means of providing a low impedance voltage source capable of sourcing and sinking small amounts of current. Note the value of this DC voltage should fall between the limits of allowable input common mode voltages. See Figure 2 for an example.



SET V_{REF} EQUAL TO THE DC MEDIAN OF THE SIGNAL VOLTAGE

Figure 2. Single-Ended Operation

The gain of the LTM9012 may also be decreased from the nominal value by adding resistance in series with the signal inputs. The internal op amps are fed by 49.9Ω series resistors and employ 511Ω feedback resistors. The voltage gain of the stage is set by the ratio of the feedback resistance to the total series resistance. Unity gain, for example, can be realized by adding a 464Ω resistor in series with each input.

Reference

The LTM9012 has an internal 1.25V voltage reference. For a 2V input range using the internal reference with a unity gain internal amplifier configuration, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE.

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be $1.6 \bullet V_{SENSE}$.

The reference is shared by all four ADC channels, so it is not possible to independently adjust the input range of individual channels.

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 3), and the single-ended encode mode (Figure 4).

The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figure 5 and Figure 6). The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC^- should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC^+ should have fast rise and fall times.

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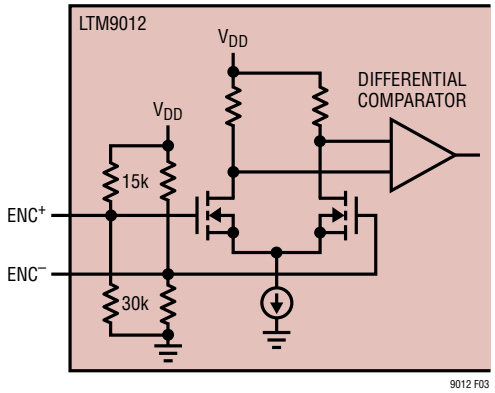


Figure 3. Equivalent Encode Input Circuit for Differential Encode Mode

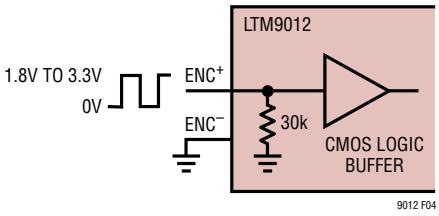
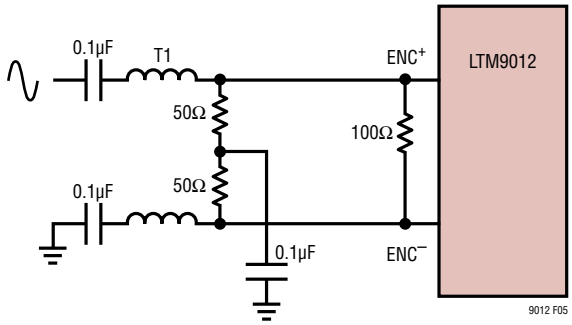


Figure 4. Equivalent Encode Input Circuit for Single-Ended Encode Mode



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 5. Sinusoidal Encode Drive

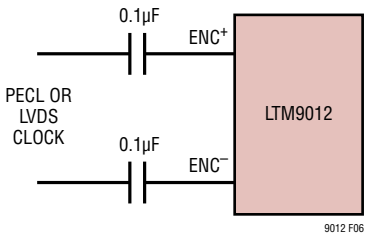


Figure 6. PECL or LVDS Encode Drive

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC– is connected to ground and ENC+ is driven with a square wave encode input. ENC+ can be taken above V_{DD} (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The ENC+ threshold is 0.9V. For good jitter performance ENC+ should have fast rise and fall times.

Clock PLL and Duty Cycle Stabilizer

The encode clock is multiplied by an internal phase-locked loop (PLL) to generate the serial digital output data. If the encode signal changes frequency or is turned off, the PLL requires 25µs to lock onto the input clock.

A clock duty cycle stabilizer circuit allows the duty cycle of the applied encode signal to vary from 30% to 70%. In the serial programming mode it is possible to disable the duty cycle stabilizer, but this is not recommended. In the parallel programming mode the duty cycle stabilizer is always enabled.

DIGITAL OUTPUTS

The digital outputs of the LTM9012 are serialized LVDS signals. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). The data can be serialized with 16-, 14-, or 12-bit serialization (see the Timing Diagrams for details). Note that with 12-bit serialization the two LSBs are not available—this mode is included for compatibility with potential 12-bit versions of these parts.

The output data should be latched on the rising and falling edges of the data clock out (DCO). A data frame output (FR) can be used to determine when the data from a new conversion result begins. In the 2-lane, 14-bit serialization mode, the frequency of the FR output is halved.

The maximum serial data rate for the data outputs is 1Gbps, so the maximum sample rate of the ADC will depend on the serialization mode as well as the speed grade of the

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ADC (see Table 1). The minimum sample rate for all serialization modes is 5Msps.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OV_{DD} which is isolated from the A/D core power.

Programmable LVDS Output Current

The default output driver current is 3.5mA. This current can be adjusted by control register A2 in the serial programming mode. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA. In the parallel programming mode the SCK pin can select either 3.5mA or 1.75mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A2. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing. In the parallel programming mode the SDO pin enables internal termination. Internal termination should only be used with 1.75mA, 2.1mA or 2.5mA LVDS output current modes.

DATA FORMAT

Table 2 shows the relationship between the analog input voltage and the digital data output bits. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A1.

Table 2. Output Codes vs Input Voltage

CH*n*⁺ TO CH*n*⁻ (0.2V RANGE)	D13 TO D0 (OFFSET BINARY)	D13 TO D0 (2's COMPLEMENT)
>0.1000000V	11 1111 1111 1111	01 1111 1111 1111
+0.0999878V	11 1111 1111 1111	01 1111 1111 1111
+0.0999756V	11 1111 1111 1110	01 1111 1111 1110
+0.0000122V	10 0000 0000 0001	00 0000 0000 0001
+0.0000000V	10 0000 0000 0000	00 0000 0000 0000
–0.0000122V	01 1111 1111 1111	11 1111 1111 1111
–0.0000244V	01 1111 1111 1111	11 1111 1111 1110
–0.0999878V	00 0000 0000 0000	10 0000 0000 0001
–0.1000000V	00 0000 0000 0000	10 0000 0000 0000
<–0.1000000V	00 0000 0000 0000	10 0000 0000 0000

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied —an exclusive-OR operation is applied between the LSB and all other bits. The FR and DCO outputs are not affected.

Table 1. Maximum Sampling Frequency for All Serialization Modes. The Sampling Frequency for Potential Slower Speed Grades Cannot Exceed $f_{SAMPLE(MAX)}$.

SERIALIZATION MODE		MAXIMUM SAMPLING FREQUENCY, f_S (MHz)	DCO FREQUENCY	FR FREQUENCY	SERIAL DATA RATE
2-Lane	16-Bit Serialization	125	4 • f_S	f_S	8 • f_S
2-Lane	14-Bit Serialization	125	3.5 • f_S	0.5 • f_S	7 • f_S
2-Lane	12-Bit Serialization	125	3 • f_S	f_S	6 • f_S
1-Lane	16-Bit Serialization	62.5	8 • f_S	f_S	16 • f_S
1-Lane	14-Bit Serialization	71.4	7 • f_S	f_S	14 • f_S
1-Lane	12-Bit Serialization	83.3	6 • f_S	f_S	12 • f_S

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The output randomizer is enabled by serially programming mode control register A1.

Digital Output Test Pattern

To allow in-circuit testing of the digital interface to the A/D, there is a test mode that forces the A/D data outputs (D13-D0) of all channels to known values. The digital output test patterns are enabled by serially programming mode control registers A3 and A4. When enabled, the test patterns override all other formatting modes: 2's complement and randomizer.

Output Disable

The digital outputs may be disabled by serially programming mode control register A2. The current drive for all digital outputs including DCO and FR are disabled to save power or enable in-circuit testing. When disabled the common mode of each output pair becomes high impedance, but the differential impedance may remain low.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire chip is powered down, resulting in 3mW power consumption. Sleep mode is enabled by mode control register A1 (serial programming mode), or by SDI (parallel programming mode). The amount of time required to recover from sleep mode depends on the size of the bypass capacitors on V_{REF}, REFH, and REFL. For the internal capacitor values and no additional external capacitance, the A/D will stabilize after 2ms.

In nap mode any combination of A/D channels can be powered down while the internal reference circuits and the PLL stay active, allowing faster wakeup than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50µs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Nap mode is enabled by mode control register A1 in the serial programming mode.

Driver Amplifier Shutdown ($\overline{SHDN}$)

The ADC drivers may be placed in shutdown mode to conserve power independently from the ADC core. Each ADC driver has an independent $\overline{SHDN}$ pin but it is expected that all four will be tied together.

DEVICE PROGRAMMING MODES

The operating modes of the LTM9012 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK, SDI and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. When used as an input, SDO should be driven through a 1k series resistor. Table 3 shows the modes set by $\overline{CS}$, SCK, SDI and SDO.

Table 3. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

PIN	DESCRIPTION
$\overline{CS}$	**2-Lane/1-Lane Selection Bit** 0 = 2-Lane, 16-Bit Serialization Output Mode 1 = 1-Lane, 14-Bit Serialization Output Mode
SCK	**LVDS Current Selection Bit** 0 = 3.5mA LVDS Current Mode 1 = 1.75mA LVDS Current Mode
SDI	**Power Down Control Bit** 0 = Normal Operation 1 = Sleep Mode
SDO	**Internal Termination Selection Bit** 0 = Internal Termination Disabled 1 = Internal Termination Enabled

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

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The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams sections). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed, then SDO can be left floating and no pull-up resistor is needed. Table 4 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command

Table 4. Serial Programming Mode Register Map (PAR/$\overline{SER}$ = GND)

REGISTER A0: RESET REGISTER (ADDRESS 00h) WRITE ONLY

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7 **RESET** Software Reset Bit
0 = Not Used
1 = Software Reset. All mode control registers are reset to 00h. The ADC is momentarily placed in Sleep mode.
This bit is automatically set back to zero at the end of the SPI Write command. The Reset register is Write only.
Data read back from the reset register will be random.

Bits 6-0 Unused, Don't Care Bits.

REGISTER A1: FORMAT AND POWER-DOWN REGISTER (ADDRESS 01h with $\overline{CS}$ = GND)

D7	D6	D5	D4	D3	D2	D1	D0
DCSOFF	RAND	TWOSCOMP	SLEEP	NAP_4	NAP_3	NAP_2	NAP_1

Bit 7 **DCSOFF** Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer On
1 = Clock Duty Cycle Stabilizer Off. This is not recommended.

Bit 6 **RAND** Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

Bit 5 **TWOSCOMP** Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format

Bits 4-0 **SLEEP: NAP_X** Sleep/Nap Mode Control Bits
00000 = Normal Operation
0XXX1 = Channel 1 in Nap Mode
0XX1X = Channel 2 in Nap Mode
0X1XX = Channel 3 in Nap Mode
01XXX = Channel 4 in Nap Mode
1XXXX = Sleep Mode. Channels 1, 2, 3 and 4 are Disabled
Note: Any combination of these channels can be placed in Nap mode.

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REGISTER A2: OUTPUT MODE REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE2	OUTMODE1	OUTMODE0

Bits 7-5 **ILVDS2:ILVDS0** LVDS Output Current Bits

000 = 3.5mA LVDS Output Driver Current

001 = 4.0mA LVDS Output Driver Current

010 = 4.5mA LVDS Output Driver Current

011 = Not Used

100 = 3.0mA LVDS Output Driver Current

101 = 2.5mA LVDS Output Driver Current

110 = 2.1mA LVDS Output Driver Current

111 = 1.75mA LVDS Output Driver Current

Bit 4 **TERMON** LVDS Internal Termination Bit

0 = Internal Termination Off

1 = Internal Termination On. LVDS Output Driver Current is 2× the Current Set by ILVDS2:ILVDS0. Internal termination should only be used with 1.75mA, 2.1mA or 2.5mA LVDS output current modes.

Bit 3 **OUTOFF** Output Disable Bit

0 = Digital Outputs are Enabled.

1 = Digital Outputs are Disabled.

Bits 2-0 **OUTMODE2:OUTMODE0** Digital Output Mode Control Bits

000 = 2-Lanes, 16-Bit Serialization

001 = 2-Lanes, 14-Bit Serialization

010 = 2-Lanes, 12-Bit Serialization

011 = Not Used

100 = Not Used

101 = 1-Lane, 14-Bit Serialization

110 = 1-Lane, 12-Bit Serialization

111 = 1-Lane, 16-Bit Serialization

REGISTER A3: TEST PATTERN MSB REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
OUTTEST	X	TP13	TP12	TP11	TP10	TP9	TP8

Bit 7 **OUTTEST** Digital Output Test Pattern Control Bit

0 = Digital Output Test Pattern Off

1 = Digital Output Test Pattern On

Bit 6 Unused, Don't Care Bit.

Bit 5-0 **TP13:TP8** Test Pattern Data Bits (MSB)

TP13:TP8 Set the Test Pattern for Data Bit 13(MSB) Through Data Bit 8.

REGISTER A4: TEST PATTERN LSB REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

Bit 7-0 **TP7:TP0** Test Pattern Data Bits (LSB)

TP7:TP0 Set the Test Pattern for Data Bit 7 Through Data Bit 0(LSB).

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APPLICATIONS INFORMATION

must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset is complete, bit D7 is automatically set back to zero.

GROUNDING AND BYPASSING

The LTM9012 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane in the first layer beneath the ADC is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

Bypass capacitors are integrated inside the package; additional capacitance is optional.

The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

LAYOUT RECOMMENDATIONS

The pin assignments of the LTM9012 allow a flow-through layout that makes it possible to use multiple parts in a small area when a large number of ADC channels are required. The LTM9012 has similar layout rules to other BGA packages. The layout can be implemented with 6mil blind vias and 5mil traces. The pinout has been designed to minimize the space required to route the analog and digital traces. The analog and digital traces can essentially be routed within the width of the package. This allows multiple packages to be located close together for high channel count applications. Trace lengths for the analog inputs and digital outputs should be matched as well as possible. Table 5 lists the trace lengths for the analog inputs and digital outputs inside the package from the die pad to the package pad. These should be added to the PCB trace lengths for best matching.

Figures 7 through Figure 11 show an example of a good PCB layout.

HEAT TRANSFER

Most of the heat generated by the LTM9012 is transferred from the die through the bottom side of the package through numerous ground pins onto the printed circuit board. For good electrical and thermal performance, these pins should be connected to the internal ground planes by an array of vias.

Table 5. Internal Trace Lengths

PIN	NAME	(mm)
Q9	$OUT1A^-$	0.535
Q10	$OUT1A^+$	0.350
R11	$OUT1B^-$	2.185
R12	$OUT1B^+$	2.216
R9	$OUT2A^-$	0.174
R10	$OUT2A^+$	0.667
S11	$OUT2B^-$	2.976
S12	$OUT2B^+$	2.972
S2	$OUT3A^-$	3.033
S3	$OUT3A^+$	3.031
R4	$OUT3B^-$	0.752
R5	$OUT3B^+$	0.370
R2	$OUT4A^-$	2.130
R3	$OUT4A^+$	2.125
Q4	$OUT4B^-$	0.332
Q5	$OUT4B^+$	0.527
A12	$CH1^-$	7.741
A11	$CH1^+$	7.723
A9	$CH2^-$	4.632
A8	$CH2^+$	4.629
A6	$CH3^-$	3.987
A5	$CH3^+$	3.988
A3	$CH4^-$	7.892
A2	$CH4^+$	7.896
P1	ENC^-	3.317
N1	ENC^+	3.325
P4	$\overline{CS}$	0.241
S9	DCO^-	1.912
S10	DCO^+	1.927
S4	FR^-	2.097
S5	FR^+	2.082
P10	PAR/$\overline{SER}$	0.226
P5	SCK	1.553
P9	SDO	0.957
P3	SDI	1.184

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APPLICATIONS INFORMATION

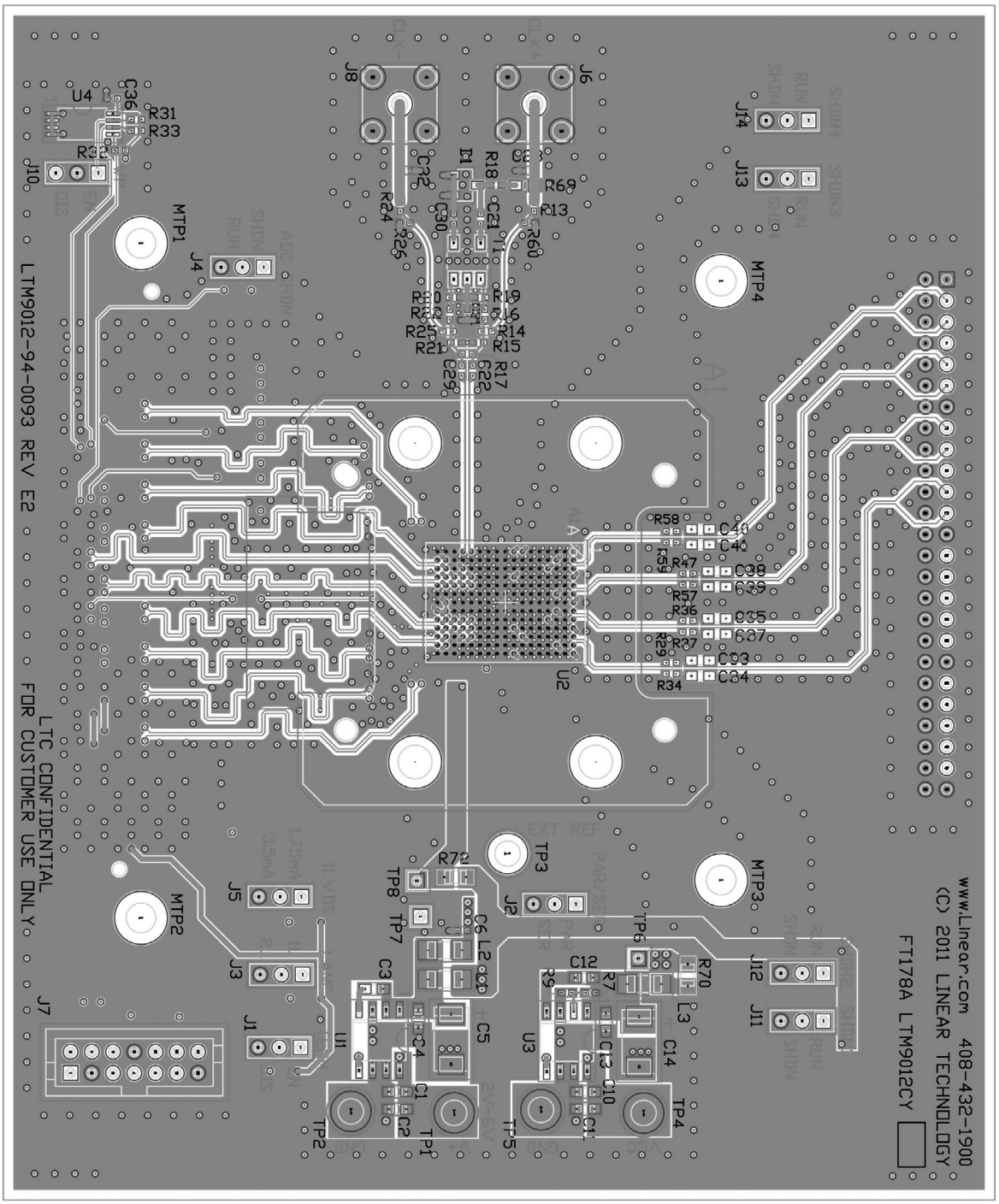

Figure 7. Layer 1 Component Side

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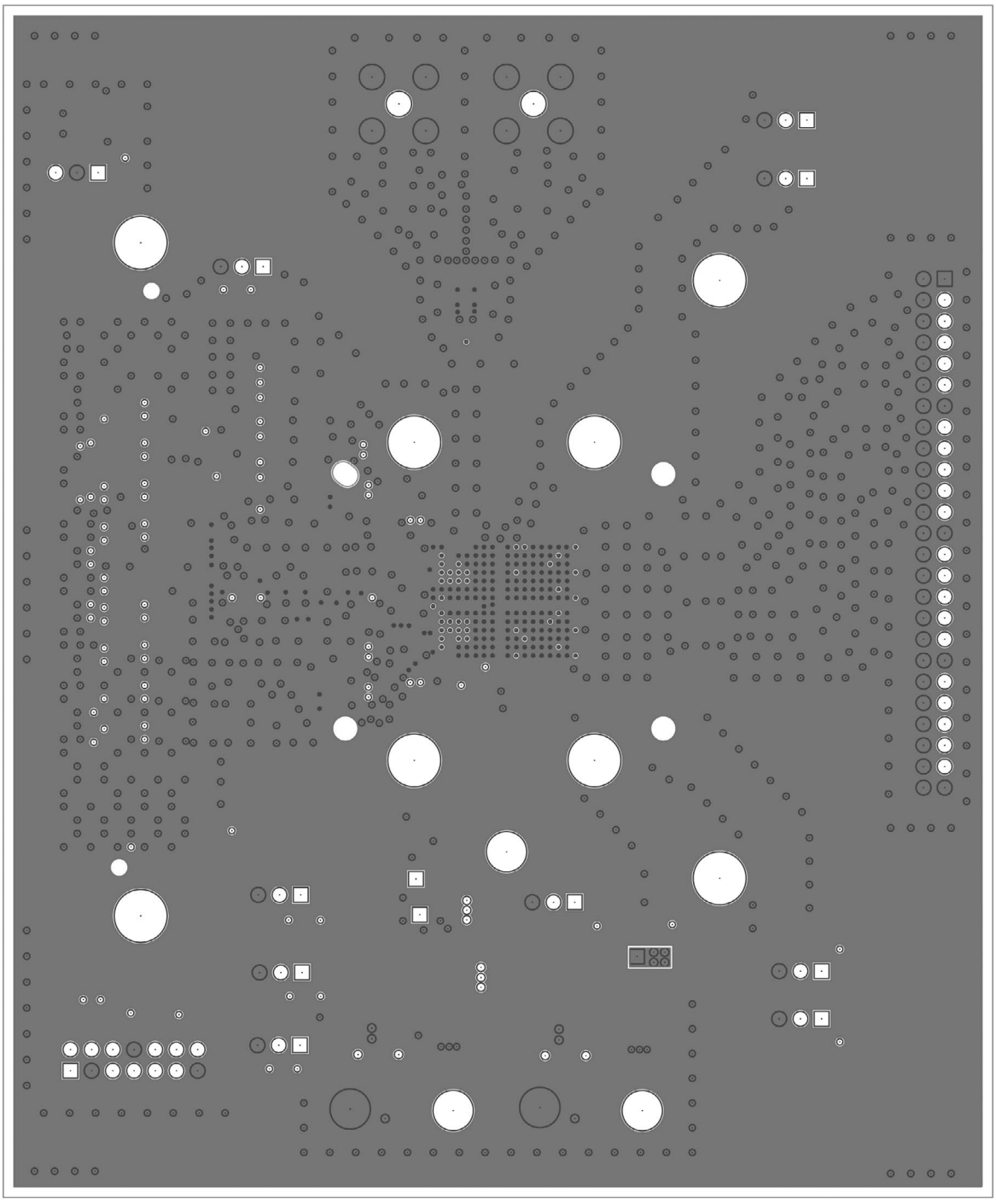

Figure 8. Layer 2

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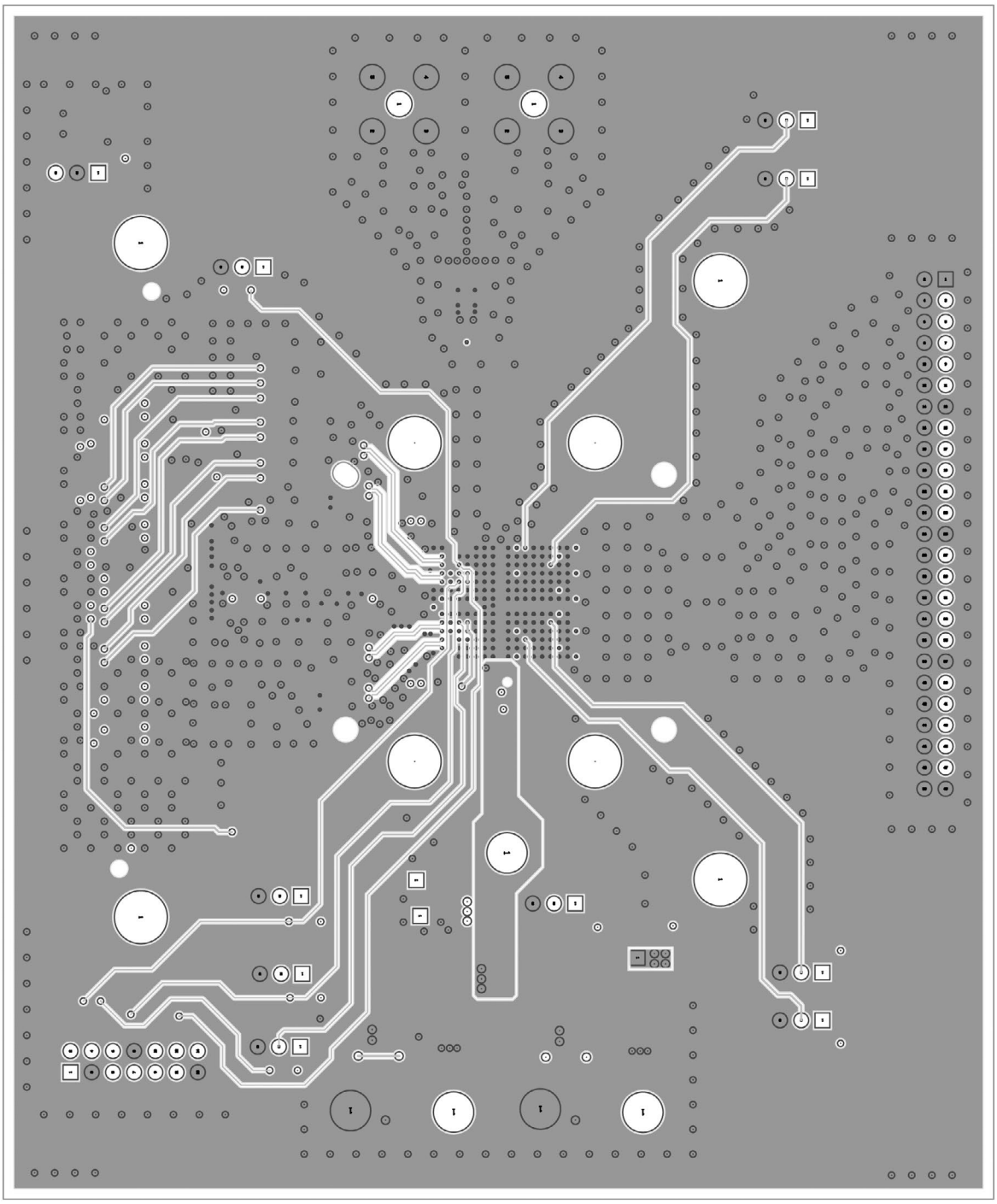

Figure 9. Layer 3

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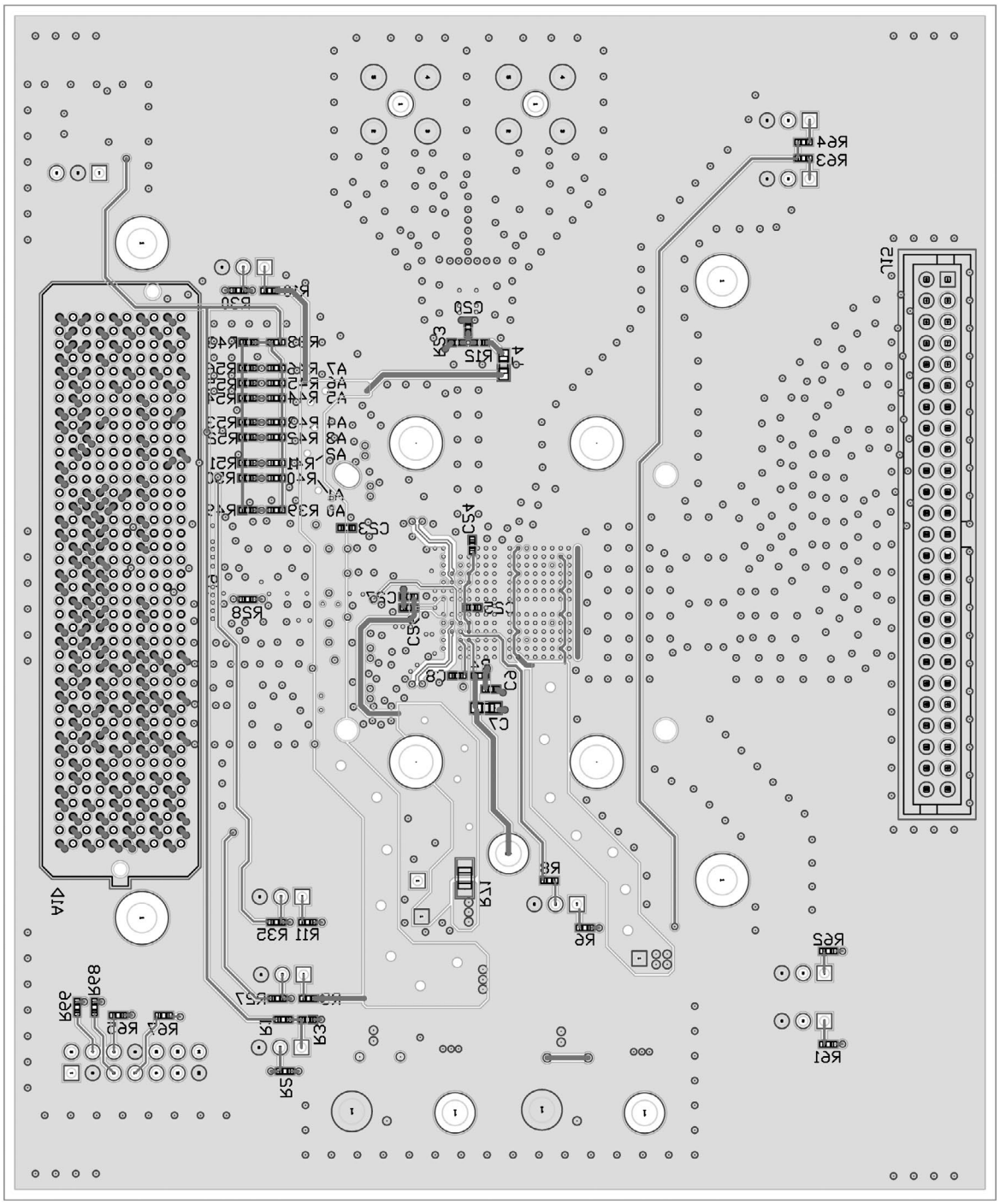

Figure 10. Back Side

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TYPICAL APPLICATION

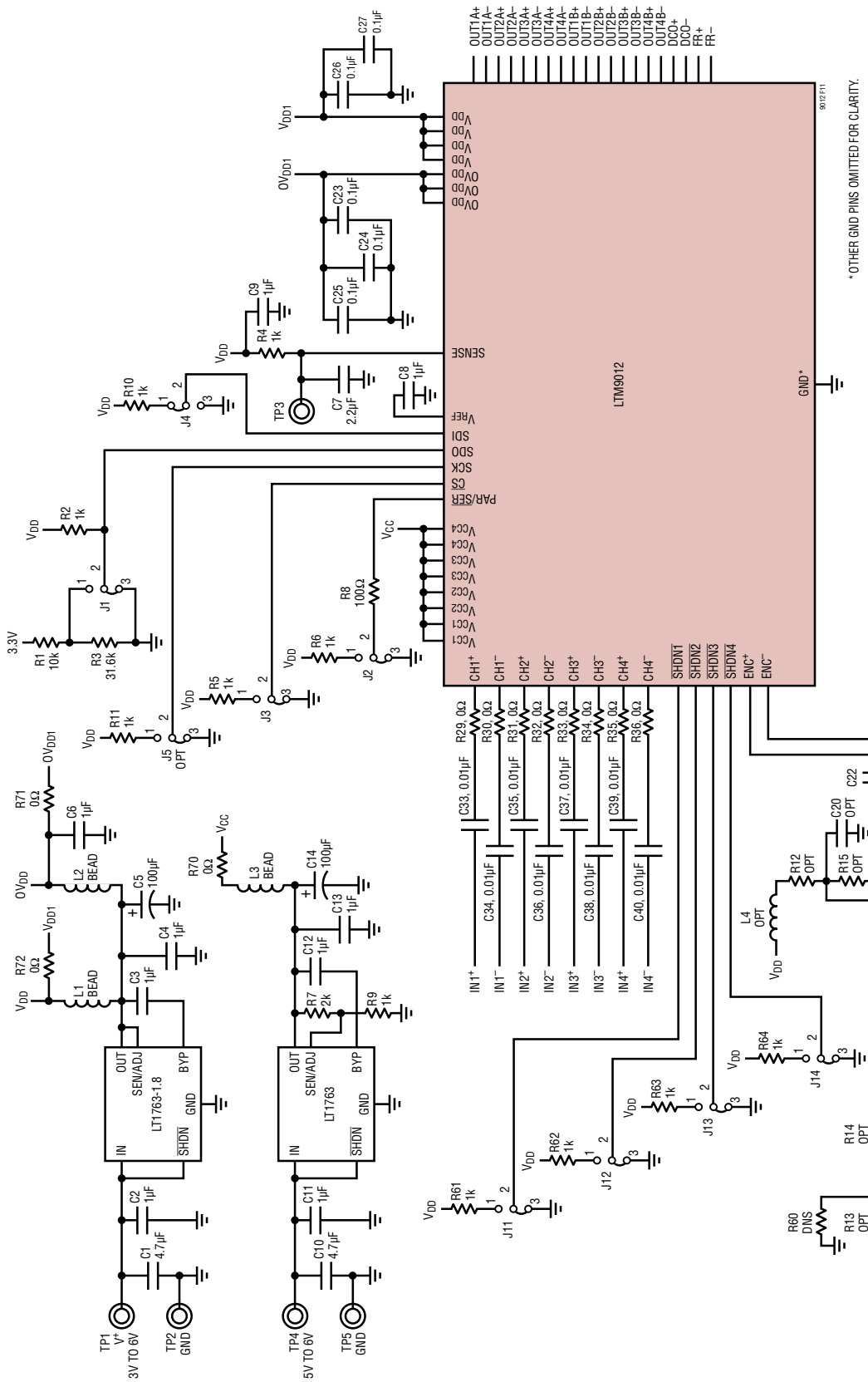

Figure 11. Simplified Schematic for Example Layout

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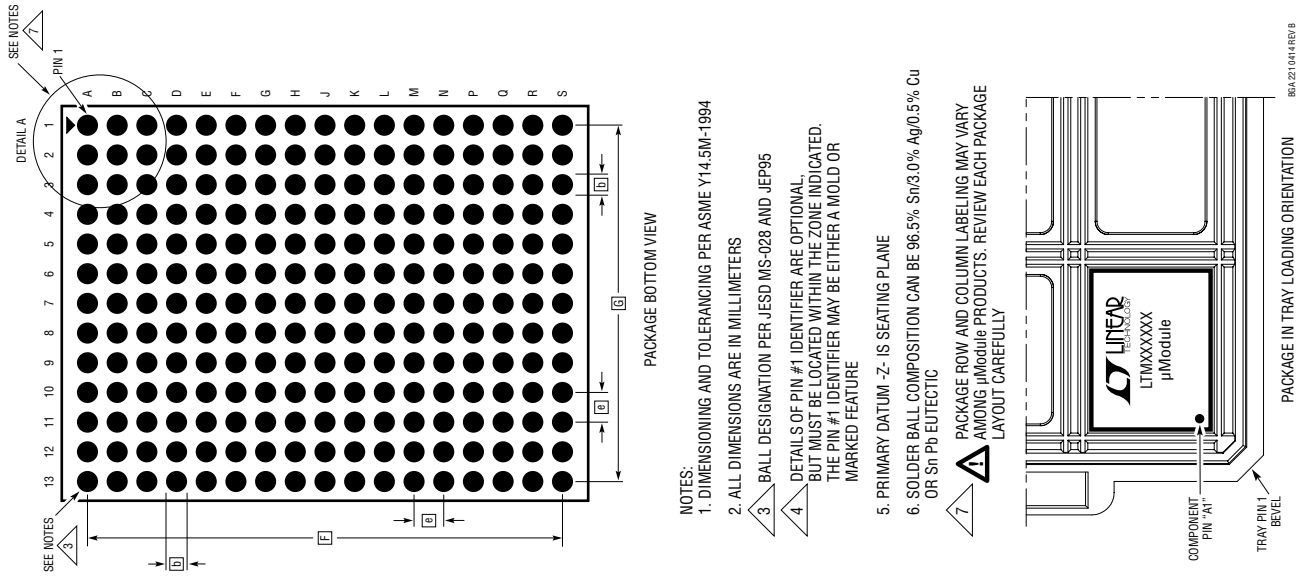
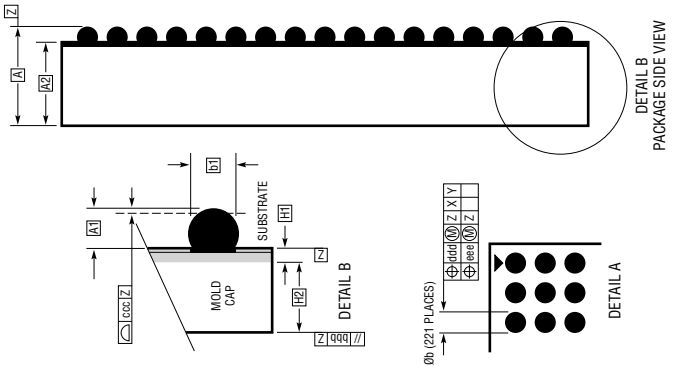
PACKAGE DESCRIPTION

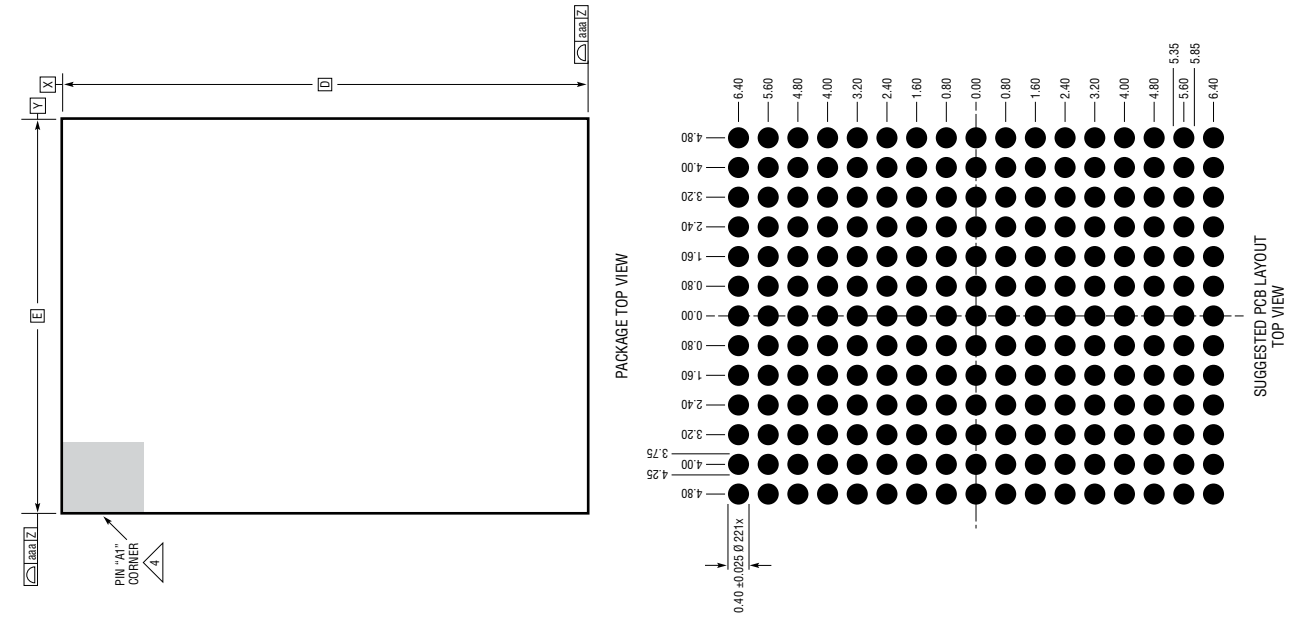
Please refer to http://www.linear.com/product/LTM9012#packaging for the most recent package drawings.



BGA Package
221-Lead (15mm × 11.25mm × 2.82mm)
(Reference LTC DWG# 05-08-1886 Rev B)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.67	2.82	2.97	
A1	0.35	0.40	0.45	
A2	2.32	2.42	2.52	
b	0.45	0.50	0.55	
b1	0.35	0.40	0.45	
D		15.0		
E		11.25		
e		0.80		
F		12.80		
G		9.60		
H1	0.37	0.42	0.47	
H2	1.95	2.00	2.05	
aaa			0.15	
bbb			0.10	
ccc			0.12	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 221				



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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/17	Corrected pin names	2, 12, 20, 25, 28

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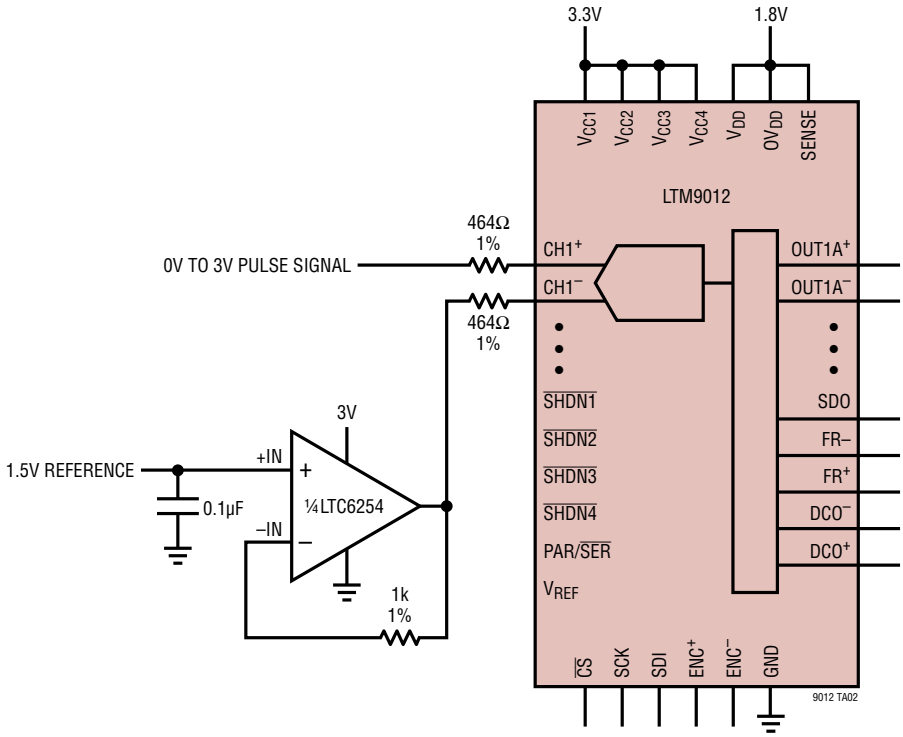
TYPICAL APPLICATION

Single-Ended Drive with Unity Gain Example



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2170-14/LTC2171-14/ LTC2172-14	14-Bit, 25Msps/40Msps/65Msps 1.8V Quad ADCs, Ultralow Power	178mW/234mW/360mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2173-14/LTC2174-14/ LTC2175-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Quad ADCs, Ultralow Power	376mW/450mW/558mW, 73.4 dB SNR, 88dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2263-14/LTC2264-14/ LTC2265-14	14-Bit, 25Msps/40Msps/65Msps 1.8V Dual ADCs, Ultralow Power	99mW/126mW/191mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTC2266-14/LTC2267-14/ LTC2268-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTM9009-14/LTM9010-14/ LTM9011-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Octal ADCs, Ultralow Power	752mW/900mW/1116mW, 73.1dB SNR, 88dB SFDR, Serial LVDS Outputs, 11.25mm × 9mm BGA-140

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