ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3, 4, 5)

Terminal Voltage

IN, OUT

t < 1ms and Duty Cycle < 1% ..... –0.3V to 7V

Steady State ..... –0.3V to 6V

BAT, $\overline{CHRG}$, HPWR, SUSP, WALL, $\overline{ACPR}$ ..... –0.3V to 6V

NTC, TIMER, PROG, CLPROG ..... –0.3V to (V_{CC} + 0.3V)

Pin Current (Steady State)

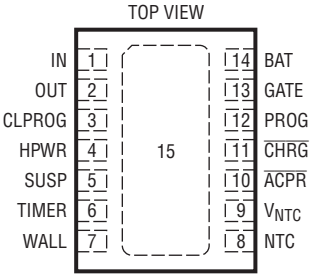
IN, OUT, BAT (Note 6) 2.5A

Operating Temperature Range ..... –40°C to 85°C

Maximum Operating Junction Temperature ..... 110°C

Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE CONNECTED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4085EDE-3#PBF	LTC4085EDE-3#TRPBF	40853	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4085EDE-4#PBF	LTC4085EDE-4#TRPBF	40854	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

LTC4085 Options

PART NUMBER	FLOAT VOLTAGE	NTC HOT THRESHOLD	UNDERVOLTAGE CURRENT LIMIT*
LTC4085	4.2V	29% V_{VNTC}	Yes
LTC4085-1	4.1V	32.6% V_{VNTC}	Yes
LTC4085-3	3.95V	32.6% V_{VNTC}	Yes
LTC4085-4	3.95V	32.6% V_{VNTC}	No

*Undervoltage current limit reduces charge current as V_{OUT} falls below approximately 4.45V.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 5). V_{IN} = 5V, V_{BAT} = 3.7V, HPWR = 5V, WALL = 0V, R_{PROG} = 100k, R_{CLPROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Voltage	IN and OUT		4.35		5.5	V
V_{BAT}	Input Voltage	BAT				4.3	V
I_{IN}	Input Supply Current	I_{BAT} = 0 (Note 7) Suspend Mode; SUSP = 5V Suspend Mode; SUSP = 5V, WALL = 5V, V_{OUT} = 4.8V	● ● ●		0.5 50 60	1.2 100 110	mA µA µA
I_{OUT}	Output Supply Current	V_{OUT} = 5V, V_{IN} = 0V, NTC = V_{NTC}	●		0.7	1.4	mA
I_{BAT}	Battery Drain Current	V_{BAT} = 4.05V, Charging Stopped Suspend Mode; SUSP = 5V V_{IN} = 0V, BAT Powers OUT, No Load	● ● ●		15 22 60	27 35 100	µA µA µA

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 5). V_{IN} = 5V, V_{BAT} = 3.7V, HPWR = 5V, WALL = 0V, R_{PROG} = 100k, R_{CLPROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{UVLO}	Input or Output Undervoltage Lockout	V_{IN} Powers Part, Rising Threshold V_{OUT} Powers Part, Rising Threshold	● ●	3.6 2.75	3.8 2.95	4 3.15	V V
ΔV_{UVLO}	Input or Output Undervoltage Lockout	V_{IN} Rising – V_{IN} Falling or V_{OUT} Rising – V_{OUT} Falling			130		mV
Current Limit							
I_{LIM}	Current Limit	R_{CLPROG} = 2k (0.1%), HPWR = 5V R_{CLPROG} = 2k (0.1%), HPWR = 0V	● ●	475 90	500 100	525 110	mA mA
$I_{IN(MAX)}$	Maximum Input Current Limit	(Note 8)			2.4		A
R_{ON}	ON Resistance V_{IN} to V_{OUT}	I_{OUT} = 100mA Load			215		mΩ
V_{CLPROG}	CLPROG Pin Voltage	R_{PROG} = 2k R_{PROG} = 1k	● ●	0.98 0.98	1 1	1.02 1.02	V V
I_{SS}	Soft Start Inrush Current	IN or OUT			5		mA/µs
V_{CLEN}	Input Current Limit Enable Threshold Voltage	(V_{IN} – V_{OUT}) V_{IN} Rising (V_{IN} – V_{OUT}) V_{IN} Falling		20	50 –60	80	mV mV
Battery Charger							
V_{FLOAT}	Regulated Output Voltage	I_{BAT} = 2mA I_{BAT} = 2mA, (0°C – 85°C)		3.915 3.910	3.95 3.95	3.985 3.990	V V
I_{BAT}	Current Mode Charge Current	R_{PROG} = 100k (0.1%), No Load R_{PROG} = 50k (0.1%), No Load	● ●	465 900	500 1000	535 1080	mA mA
$I_{BAT(MAX)}$	Maximum Charge Current	(Note 8)			1.5		A
V_{PROG}	PROG Pin Voltage	R_{PROG} = 100k R_{PROG} = 50k	● ●	0.98 0.98	1 1	1.02 1.02	V V
k_{EOC}	Ratio of End-of-Charge Current to Charge Current	V_{BAT} = V_{FLOAT} (3.95V)	●	0.085	0.1	0.11	mA/mA
I_{TRIKL}	Trickle Charge Current	V_{BAT} = 2V, R_{PROG} = 100k (0.1%)		35	50	60	mA
V_{TRIKL}	Trickle Charge Threshold Voltage		●	2.75	2.9	3	V
V_{CEN}	Charger Enable Threshold Voltage	(V_{OUT} – V_{BAT}) Falling; V_{BAT} = 4V (V_{OUT} – V_{BAT}) Rising; V_{BAT} = 4V			55 80		mV mV
V_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT} – V_{RECHRG}	●	60	95	130	mV
t_{TIMER}	TIMER Accuracy	V_{BAT} = 4.05V		–10		10	%
	Recharge Time	Percent of Total Charge Time			50		%
	Low Battery Trickle Charge Time	Percent of Total Charge Time, V_{BAT} < 2.8V			25		%
T_{LIM}	Junction Temperature in Constant Temperature Mode				105		°C
Internal Ideal Diode							
R_{FWD}	Incremental Resistance, V_{ON} Regulation	I_{BAT} = 100mA			125		mΩ
$R_{DIO(ON)}$	ON Resistance V_{BAT} to V_{OUT}	I_{BAT} = 600mA			215		mΩ
V_{FWD}	Voltage Forward Drop (V_{BAT} – V_{OUT})	I_{BAT} = 5mA I_{BAT} = 100mA I_{BAT} = 600mA	●	10	30 55 160	50	mV mV mV
V_{OFF}	Diode Disable Battery Voltage				2.8		V
I_{FWD}	Load Current Limit, for V_{ON} Regulation				550		mA
$I_{D(MAX)}$	Diode Current Limit				2.2		A

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 5). V_{IN} = 5V, V_{BAT} = 3.7V, HPWR = 5V, WALL = 0V, R_{PROG} = 100k, R_{CLPROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External Ideal Diode							
$V_{FWD,EDA}$	External Ideal Diode Forward Voltage	V_{GATE} = 1.85V; I_{GATE} = 0			20		mV
Logic							
V_{OL}	Output Low Voltage $\overline{CHRG}$, $\overline{ACPR}$	I_{SINK} = 5mA	●		0.1	0.4	V
V_{IH}	Input High Voltage	SUSP, HPWR Pin	●	1.2			V
V_{IL}	Input Low Voltage	SUSP, HPWR Pin	●			0.4	V
I_{PULLDN}	Logic Input Pull-Down Current	SUSP, HPWR			2		µA
$V_{CHG(SD)}$	Charger Shutdown Threshold Voltage on TIMER		●	0.14		0.4	V
$I_{CHG(SD)}$	Charger Shutdown Pull-Up Current on TIMER	V_{TIMER} = 0V	●	5	14		µA
V_{WAR}	Absolute Wall Input Threshold Voltage	V_{WALL} Rising Threshold	●	4.15	4.25	4.35	V
V_{WAF}	Absolute Wall Input Threshold Voltage	V_{WALL} Falling Threshold			3.12		V
V_{WDR}	Delta Wall Input Threshold Voltage	$V_{WALL} – V_{BAT}$ Rising Threshold			75		mV
V_{WDF}	Delta Wall Input Threshold Voltage	$V_{WALL} – V_{BAT}$ Falling Threshold	●	0	25	60	mV
I_{WALL}	Wall Input Current	V_{WALL} = 5V			75	150	µA
NTC							
V_{VNTC}	V_{NTC} Bias Voltage	I_{VNTC} = 500µA	●	4.4	4.85		V
I_{NTC}	NTC Input Leakage Current	V_{NTC} = 1V			0	±1	µA
V_{COLD}	Cold Temperature Fault Threshold Voltage Hysteresis	Rising Threshold Hysteresis			0.738 • V_{VNTC} 0.018 • V_{VNTC}		V V
V_{HOT}	Hot Temperature Fault Threshold Voltage Hysteresis	Falling Threshold Hysteresis			0.326 • V_{VNTC} 0.015 • V_{VNTC}		V V
V_{DIS}	NTC Disable Voltage	NTC Input Voltage to GND (Falling) Hysteresis	●	75	100 35	125	mV mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: V_{CC} is the greater of V_{IN}, V_{OUT} or V_{BAT}.

Note 3: All voltage values are with respect to GND.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 5: The LTC4085-3/LTC4085-4 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4085E-3/LTC4085E-4 is guaranteed to meet specified performance from 0° to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 6: Guaranteed by long term current density limitations.

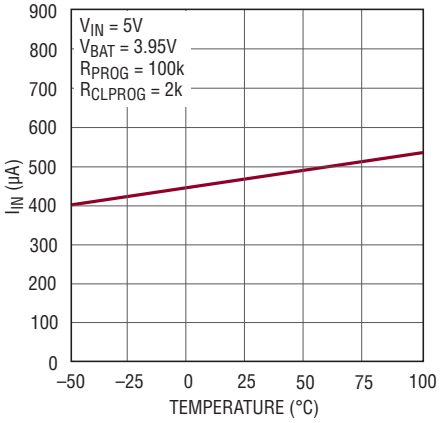
Note 7: Total input current is equal to this specification plus 1.002 • I_{BAT} where I_{BAT} is the charge current.

Note 8: Accuracy of programmed current may degrade for currents greater than 1.5A.

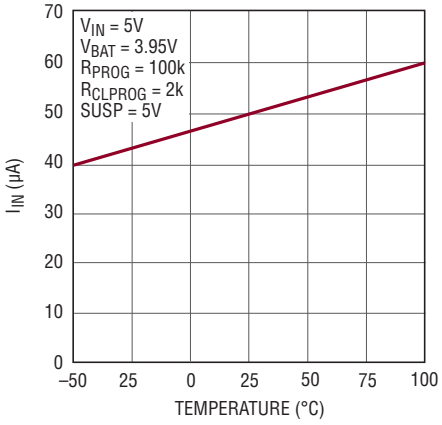
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

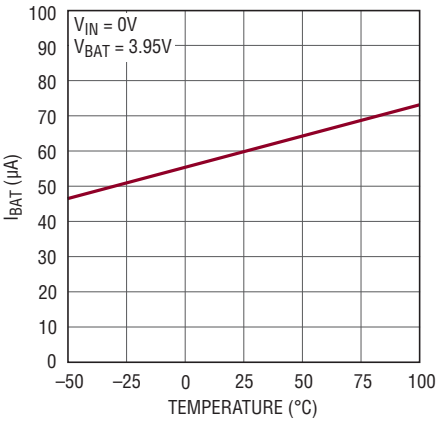
Input Supply Current vs Temperature



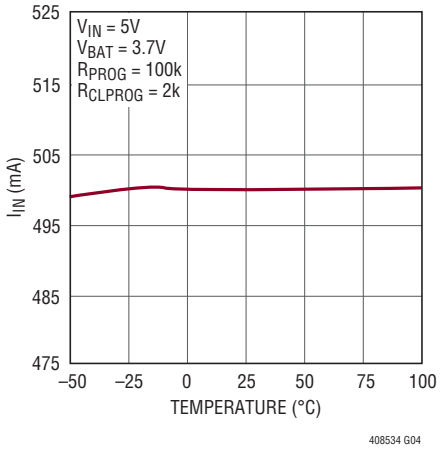
Input Supply Current vs Temperature (Suspend Mode)



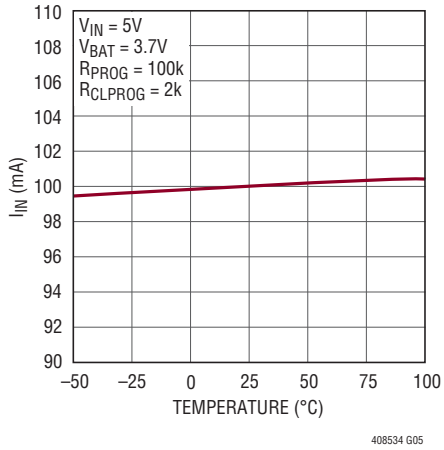
Battery Drain Current vs Temperature (BAT Powers OUT, No Load)



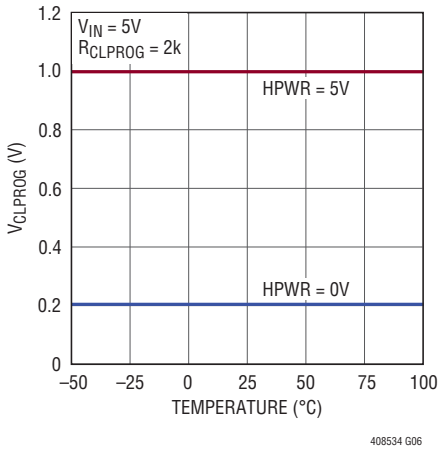
Input Current Limit vs Temperature, HPWR = 5V



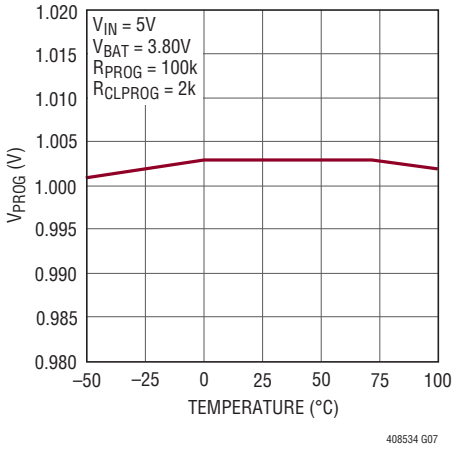
Input Current Limit vs Temperature, HPWR = 0V



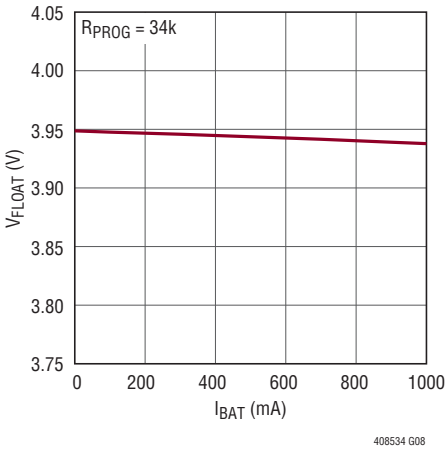
CLPROG Pin Voltage vs Temperature



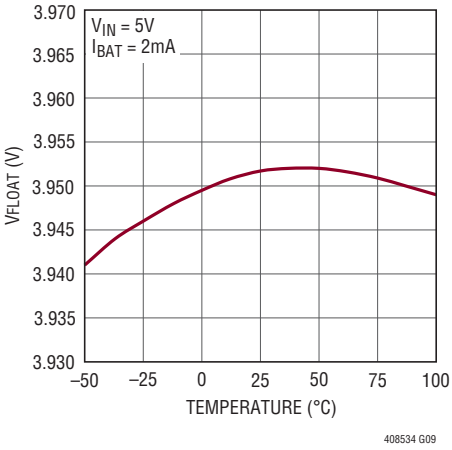
PROG Pin Voltage vs Temperature



V_{FLOAT} Load Regulation

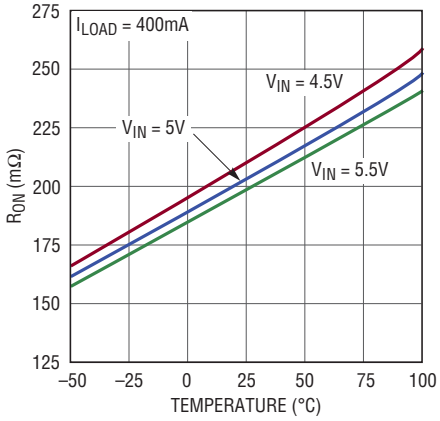


Battery Regulation (Float) Voltage vs Temperature



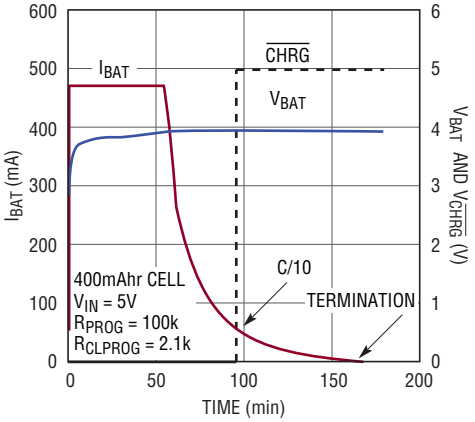
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Input R_{ON} vs Temperature



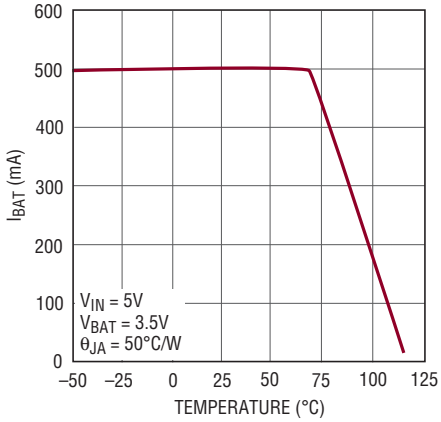
408534 G10

Battery Current and Voltage vs Time



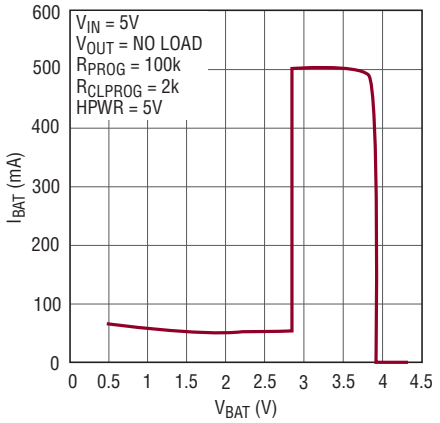
408534 G11

Charge Current vs Temperature (Thermal Regulation)



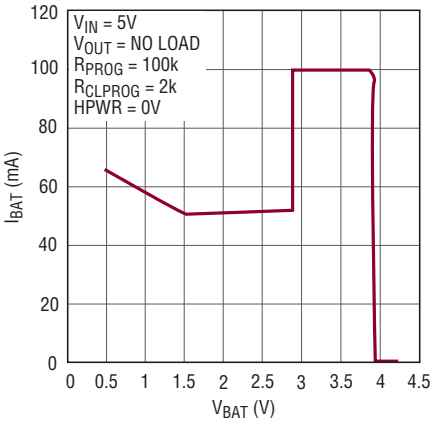
408534 G12

Charging from USB, I_{BAT} vs V_{BAT}



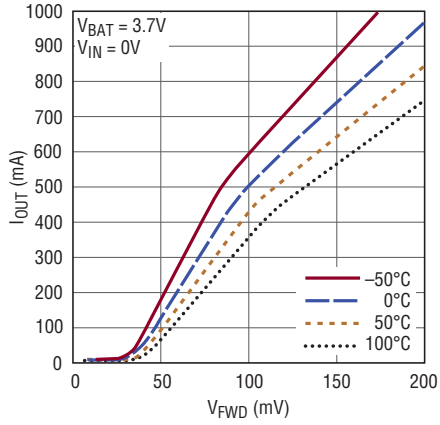
408534 G13

Charging from USB, Low Power, I_{BAT} vs V_{BAT}



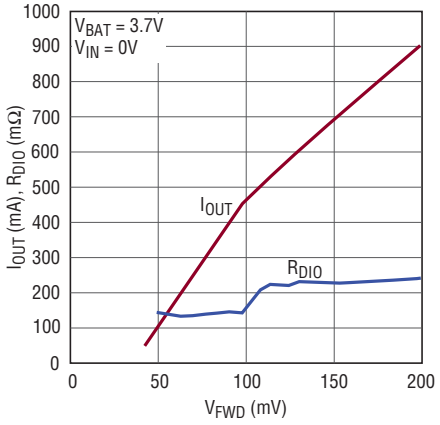
408534 G14

Ideal Diode Current vs Forward Voltage and Temperature (No External Device)



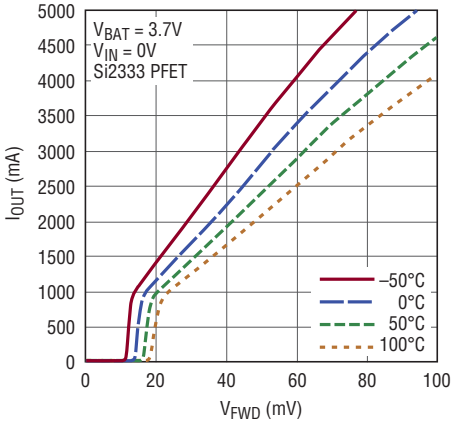
408534 G15

Ideal Diode Resistance and Current vs Forward Voltage (No External Device)



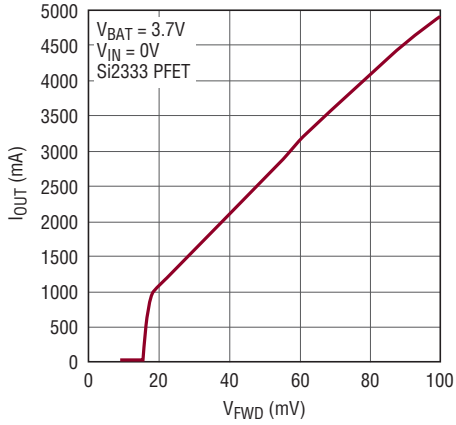
408534 G16

Ideal Diode Current vs Forward Voltage and Temperature with External Device



408534 G17

Ideal Diode Resistance and Current vs Forward Voltage with External Device

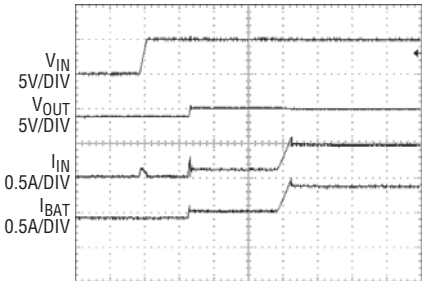


408534 G18

TYPICAL PERFORMANCE CHARACTERISTICS

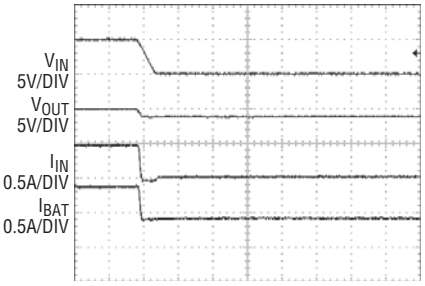
T_A = 25°C unless otherwise noted.

Input Connect Waveforms



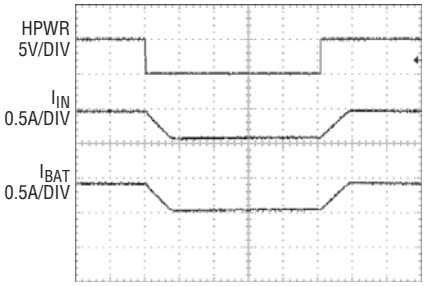
V_{BAT} = 3.85V
I_{OUT} = 100mA

Input Disconnect Waveforms



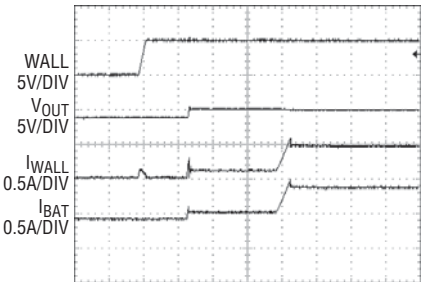
V_{BAT} = 3.85V
I_{OUT} = 100mA

Wall Connect Waveforms, V_{IN} = 0V



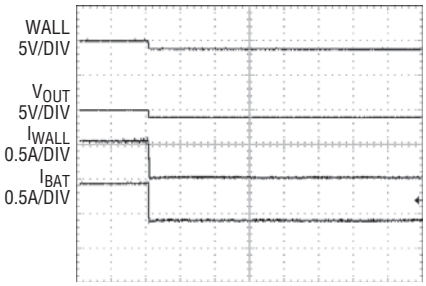
V_{BAT} = 3.85V
I_{OUT} = 50mA

Wall Disconnect Waveforms, V_{IN} = 0V



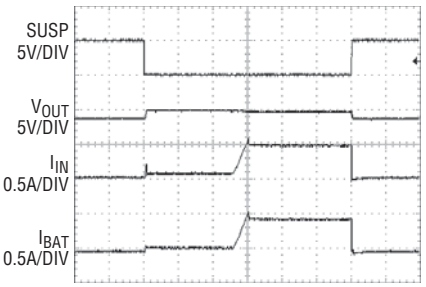
V_{BAT} = 3.85V
I_{OUT} = 100mA
R_{PROG} = 100k

Response to HPWR



V_{BAT} = 3.85V
I_{OUT} = 100mA
R_{PROG} = 100k

Response to Suspend



V_{BAT} = 3.85V
I_{OUT} = 50mA

PIN FUNCTIONS

IN (Pin 1): Input Supply. Connect to USB supply, V_{BUS}. Input current to this pin is limited to either 20% or 100% of the current programmed by the CLPROG pin as determined by the state of the HPWR pin. Charge current (to BAT pin) supplied through the input is set to the current programmed by the PROG pin but will be limited by the input current limit if charge current is set greater than the input current limit.

OUT (Pin 2): Voltage Output. This pin is used to provide controlled power to a USB device from either USB V_{BUS} (IN) or the battery (BAT) when the USB is not present. This pin can also be used as an input for battery charging when the USB is not present and a wall adapter is applied to this pin. OUT should be bypassed with at least 4.7µF to GND.

CLPROG (Pin 3): Current Limit Program and Input Current Monitor. Connecting a resistor, R_{CLPROG}, to ground programs the input to output current limit. The current limit is programmed as follows:

$$I_{CL}(A) = \frac{1000V}{R_{CLPROG}}$$

In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

The voltage on the CLPROG pin is always proportional to the current flowing through the IN to OUT power path. This current can be calculated as follows:

$$I_{IN}(A) = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

HPWR (Pin 4): High Power Select. This logic input is used to control the input current limit. A voltage greater than 1.2V on the pin will set the input current limit to 100% of the current programmed by the CLPROG pin. A voltage less than 0.4V on the pin will set the input current limit to 20% of the current programmed by the CLPROG pin. A 2µA pull-down is internally applied to this pin to ensure it is low at power up when the pin is not being driven externally.

SUSP (Pin 5): Suspend Mode Input. Pulling this pin above 1.2V will disable the power path from IN to OUT. The supply current from IN will be reduced to comply with the USB specification for suspend mode. Both the ability to charge the battery from OUT and the ideal diode function (from BAT to OUT) will remain active. Suspend mode will reset the charge timer if V_{OUT} is less than V_{BAT} while in suspend mode. If V_{OUT} is kept greater than V_{BAT}, such as when a wall adapter is present, the charge timer will not be reset when the part is put in suspend. A 2µA pull-down is internally applied to this pin to ensure it is low at power up when the pin is not being driven externally.

TIMER (Pin 6): Timer Capacitor. Placing a capacitor, C_{TIMER}, to GND sets the timer period. The timer period is:

$$t_{TIMER}(Hours) = \frac{C_{TIMER} \bullet R_{PROG} \bullet 3Hours}{0.1\mu F \bullet 100k}$$

Charge time is increased if charge current is reduced due to undervoltage current limit, load current, thermal regulation and current limit selection (HPWR).

Shorting the TIMER pin to GND disables the battery charging functions.

PIN FUNCTIONS

WALL (Pin 7): Wall Adapter Present Input. Pulling this pin above 4.25V will disconnect the power path from IN to OUT. The $\overline{ACPR}$ pin will also be pulled low to indicate that a wall adapter has been detected.

NTC (Pin 8): Input to the NTC Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery pack to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from V_{NTC} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

V_{NTC} (Pin 9): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

$\overline{ACPR}$ (Pin 10): Wall Adapter Present Output. Active low open drain output pin. A low on this pin indicates that the wall adapter input comparator has had its input pulled above the input threshold. This feature is disabled if no power is present on IN or OUT or BAT (i.e., below UVLO thresholds).

$\overline{CHRG}$ (Pin 11): Open-Drain Charge Status Output. When the battery is being charged, the $\overline{CHRG}$ pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below 10% of the programmed charge current (while in voltage mode) or the input supply or output supply is removed, the $\overline{CHRG}$ pin is forced to a high impedance state.

PROG (Pin 12): Charge Current Program. Connecting a resistor, R_{PROG}, to ground programs the battery charge current. The battery charge current is programmed as follows:

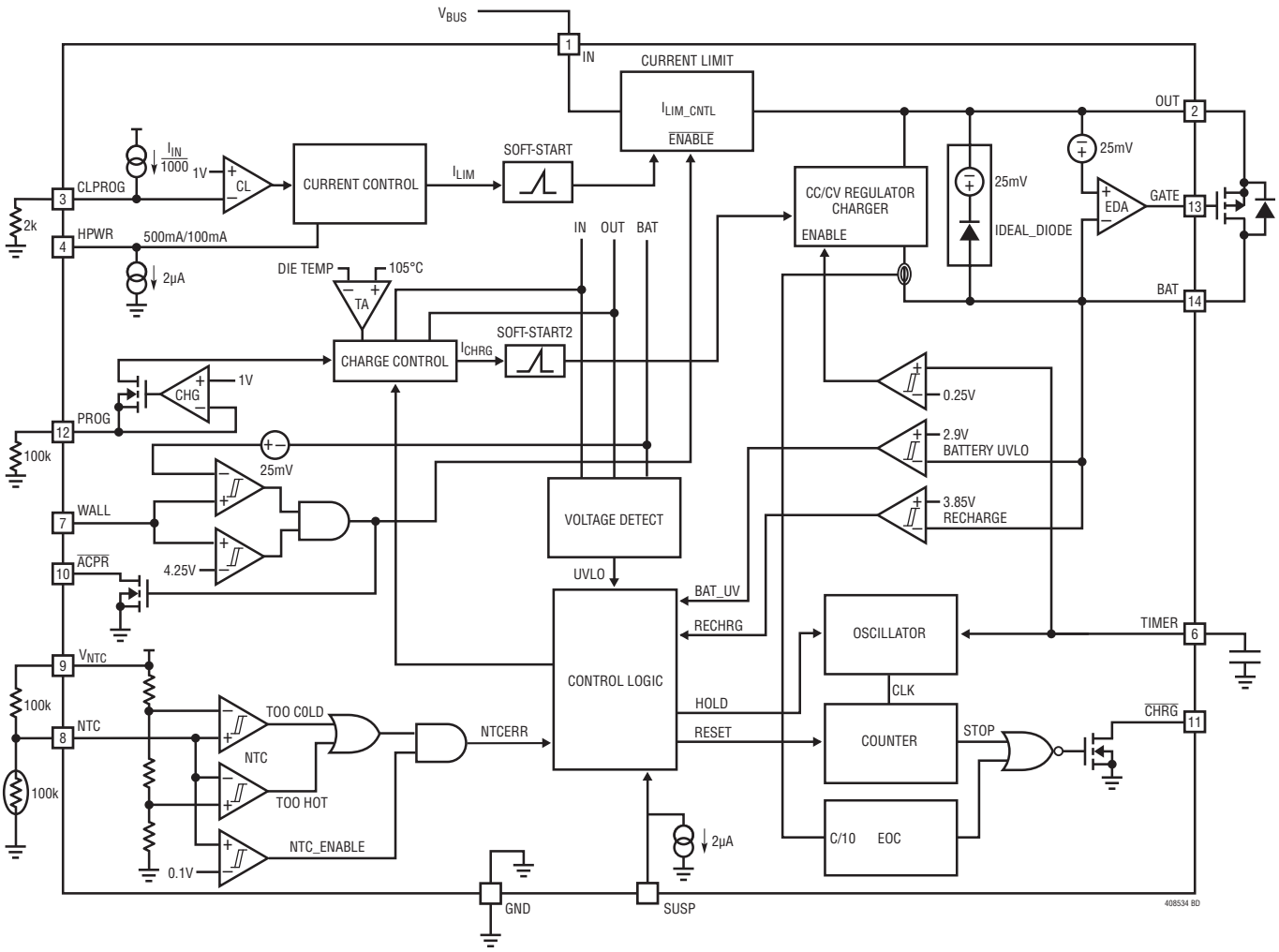
$$I_{CHG}(A) = \frac{50,000V}{R_{PROG}}$$

GATE (Pin 13): External Ideal Diode Gate Pin. This pin can be used to drive the gate of an optional external PFET connected between BAT and OUT. By doing so, the impedance of the ideal diode between BAT and OUT can be reduced. When not in use, this pin should be left floating. It is important to maintain a high impedance on this pin and minimize all leakage paths.

BAT (Pin 14): Connect to a single cell Li-Ion battery. This pin is used as an output when charging the battery and as an input when supplying power to OUT. When the OUT pin potential drops below the BAT pin potential, an ideal diode function connects BAT to OUT and prevents V_{OUT} from dropping significantly below V_{BAT}. A precision internal resistor divider sets the final float (charging) potential on this pin. The internal resistor divider is disconnected when IN and OUT are in undervoltage lockout.

GND (Pin 15): Ground. The exposed package pad is electrical ground and must be soldered to the PC board for proper functionality and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC4085 is a complete PowerPath controller for battery powered USB applications. The LTC4085 is designed to receive power from a USB source, a wall adapter, or a battery. It can then deliver power to an application connected to the OUT pin and a battery connected to the BAT pin (assuming that an external supply other than the battery is present). Power supplies that have limited current resources (such as USB V_{BUS} supplies) should be connected to the IN pin which has a programmable current limit. Battery charge current will be adjusted to ensure that the sum of the charge current and load current does not exceed the programmed input current limit.

An ideal diode function provides power from the battery when output/load current exceeds the input current limit or when input power is removed. Powering the load through the ideal diode instead of connecting the load directly to the battery allows a fully charged battery to remain fully charged until external power is removed. Once external power is removed the output drops until the ideal diode is forward biased. The forward biased ideal diode will then provide the output power to the load from the battery.

Furthermore, powering switching regulator loads from the OUT pin (rather than directly from the battery) results in shorter battery charge times. This is due to the fact that switching regulators typically require constant input power. When this power is drawn from the OUT pin voltage (rather than the *lower* BAT pin voltage) the current consumed by the switching regulator is lower leaving more current available to charge the battery.

The LTC4085 also has the ability to receive power from a wall adapter. Wall adapter power can be connected to the output (load side) of the LTC4085 through an external device such as a power Schottky or FET, as shown in Figure 1. The LTC4085 has the unique ability to use the output, which is powered by the wall adapter, as a path to charge the battery while providing power to the load. A wall adapter comparator on the LTC4085 can be configured to detect the presence of the wall adapter and shut off the connection to the USB to prevent reverse conduction out to the USB bus.

OPERATION

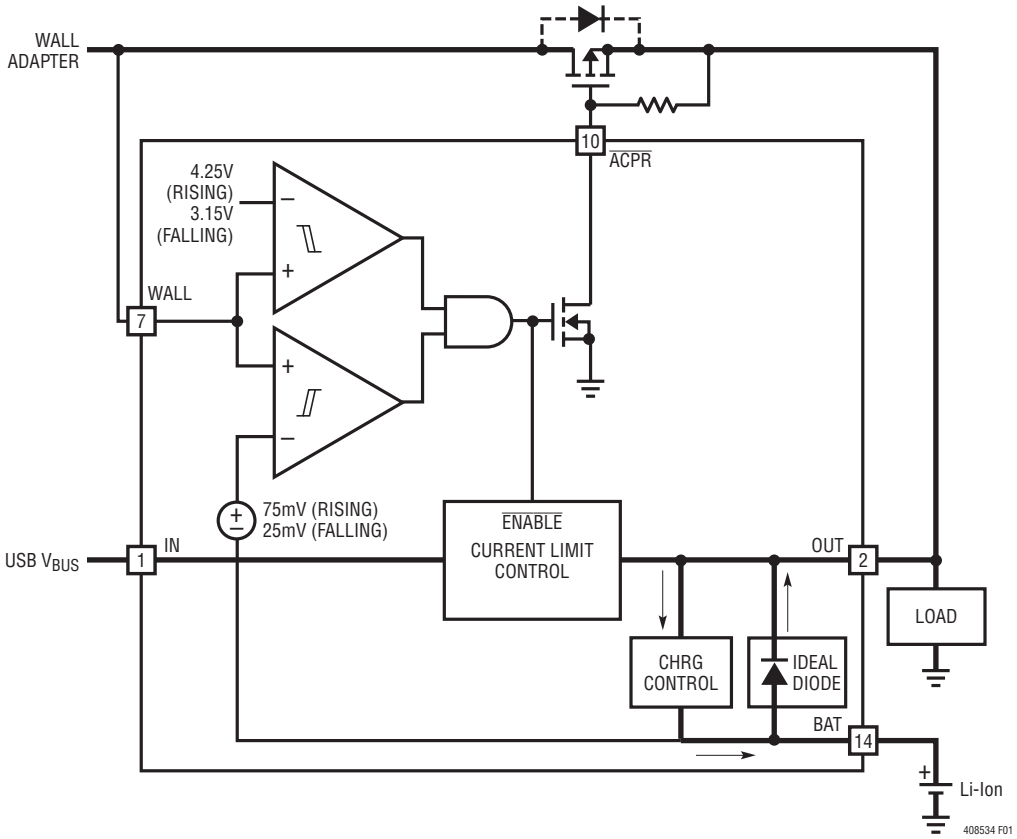


Figure 1: Simplified Block Diagram—PowerPath

OPERATION

Table 1. Operating Modes—PowerPath States
Current Limited Input Power (IN to OUT)

WALL PRESENT	SUSPEND	V_{IN} > 3.8V	V_{IN} > (V_{OUT} + 100mV)	V_{IN} > (V_{BAT} + 100mV)	CURRENT LIMIT ENABLED
Y	X	X	X	X	N
X	Y	X	X	X	N
X	X	N	X	X	N
X	X	X	N	X	N
X	X	X	X	N	N
N	N	Y	Y	Y	Y

Battery Charger (OUT to BAT)

WALL PRESENT	SUSPEND	V_{OUT} > 4.35V	V_{OUT} > (V_{BAT} + 100mV)	CHARGER ENABLED
X	X	N	X	N
X	X	X	N	N
X	X	Y	Y	Y

Ideal Diode (BAT to OUT)

WALL PRESENT	SUSPEND	V_{IN}	V_{BAT} > V_{OUT}	V_{BAT} > 2.8V	DIODE ENABLED
X	X	X	X	N	N
X	X	X	N	X	N
X	X	X	Y	Y	Y

Operating Modes—Pin Currents vs Programmed Currents (Powered from IN)

PROGRAMMING	OUTPUT CURRENT	BATTERY CURRENT	INPUT CURRENT
$I_{CL} = I_{CHG}$	$I_{OUT} < I_{CL}$ $I_{OUT} = I_{CL} = I_{CHG}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = 0$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$
$I_{CL} > I_{CHG}$	$I_{OUT} < (I_{CL} - I_{CHG})$ $I_{OUT} > (I_{CL} - I_{CHG})$ $I_{OUT} = I_{CL}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CHG}$ $I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = 0$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CHG} + I_{OUT}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$
$I_{CL} < I_{CHG}$	$I_{OUT} < I_{CL}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$

OPERATION

USB Current Limit and Charge Current Control

The current limit and charger control circuits of the LTC4085 are designed to limit input current as well as control battery charge current as a function of I_{OUT}. The programmed current limit, I_{CL}, is defined as:

$$I_{CL} = \left(\frac{1000}{R_{CLPROG}} \bullet V_{CLPROG} \right) = \frac{1000V}{R_{CLPROG}}$$

The programmed battery charge current, I_{CHG}, is defined as:

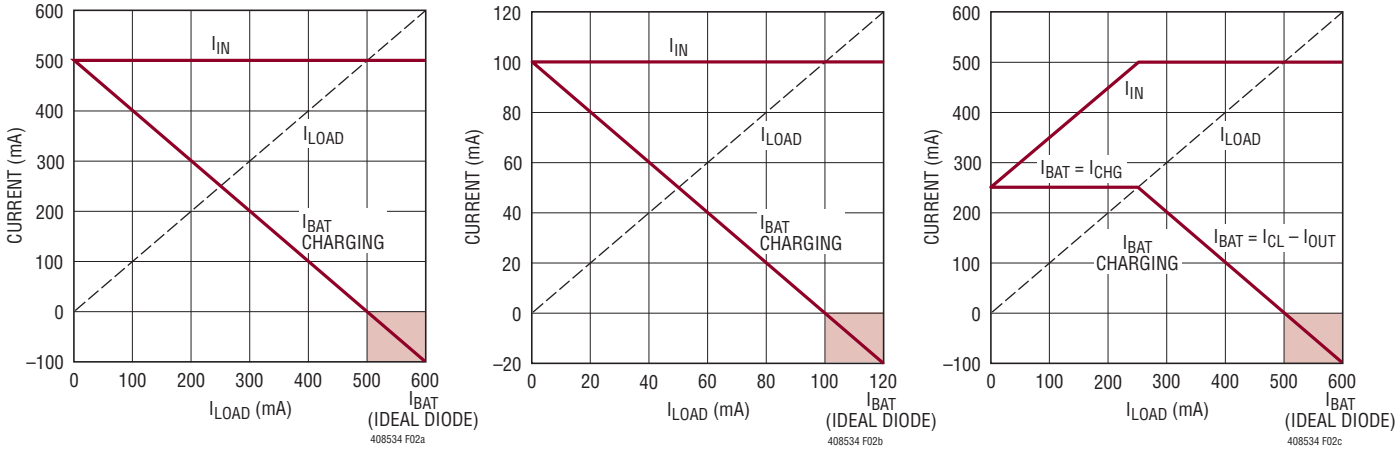
$$I_{CHG} = \left(\frac{50,000}{R_{PROG}} \bullet V_{PROG} \right) = \frac{50,000V}{R_{PROG}}$$

Input current, I_{IN}, is equal to the sum of the BAT pin output current and the OUT pin output current:

$$I_{IN} = I_{OUT} + I_{BAT}$$

The current limiting circuitry in the LTC4085 can and should be configured to limit current to 500mA for USB applications (selectable using the HPWR pin and programmed using the CLPROG pin).

The LTC4085 reduces battery charge current such that the sum of the battery charge current and the load current does not exceed the programmed input current limit (one-fifth of the programmed input current limit when HPWR is low, see Figure 2). The battery charge current goes to zero when load current exceeds the programmed input current limit (one-fifth of the limit when HPWR is low). If the load current is greater than the current limit, the output voltage will drop to just under the battery voltage where the ideal diode circuit will take over and the excess load current will be drawn from the battery.



(2a) High Power Mode/Full Charge R_{PROG} = 100k and R_{CLPROG} = 2k

(2b) Low Power Mode/Full Charge R_{PROG} = 100k and R_{CLPROG} = 2k

(2c) High Power Mode with I_{CL} = 500mA and I_{CHG} = 250mA R_{PROG} = 100k and R_{CLPROG} = 2k

Figure 2: Input and Battery Currents as a Function of Load Current

OPERATION

Programming Current Limit

The formula for input current limit is:

$$I_{CL} = \left(\frac{1000}{R_{CLPROG}} \bullet V_{CLPROG} \right) = \frac{1000V}{R_{CLPROG}}$$

where V_{CLPROG} is the CLPROG pin voltage and R_{CLPROG} is the total resistance from the CLPROG pin to ground.

For example, if typical 500mA current limit is required, calculate:

$$R_{CLPROG} = \frac{1V}{500mA} \bullet 1000 = 2k$$

In USB applications, the minimum value for R_{CLPROG} should be 2.1k. This will prevent the application current from exceeding 500mA due to LTC4085 tolerances and quiescent currents. A 2.1k CLPROG resistor will give a typical current limit of 476mA in high power mode (HPWR = 1) or 95mA in low power mode (HPWR = 0).

V_{CLPROG} will track the input current according to the following equation:

$$I_{IN} = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

For best stability over temperature and time, 1% metal film resistors are recommended.

Ideal Diode from BAT to OUT

The LTC4085 has an internal ideal diode as well as a controller for an optional external ideal diode. If a battery is the only power supply available or if the load current exceeds the programmed input current limit, then the battery will automatically deliver power to the load via an ideal diode circuit between the BAT and OUT pins. The ideal diode circuit (along with the recommended 4.7µF capacitor on the OUT pin) allows the LTC4085 to handle large transient loads and wall adapter or USB V_{BUS} connect/disconnect scenarios without the need for large bulk capacitors. The ideal diode responds within a few microseconds and prevents the OUT pin voltage from dropping significantly below the BAT pin voltage. A comparison of the I-V curve of the ideal diode and a Schottky diode can be seen in Figure 3.

If the input current increases beyond the programmed input current limit additional current will be drawn from the battery via the internal ideal diode. Furthermore, if power to IN (USB V_{BUS}) or OUT (external wall adapter) is removed, then all of the application power will be provided by the battery via the ideal diode. A 4.7µF capacitor at OUT is sufficient to keep a transition from input power to battery power from causing significant output voltage droop. The ideal diode consists of a precision amplifier that enables a large P-Channel MOSFET transistor whenever the voltage at OUT is approximately 20mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 200mΩ. If this is sufficient for the application then no external components are necessary. However, if more conductance is needed, an external PFET can be added from BAT to OUT. The GATE pin of the LTC4085 drives the gate of the PFET for automatic ideal diode control. The source of the external PFET should be connected to OUT and the drain should be connected to BAT. In order to help protect the external PFET in over-current situations, it should be placed in close thermal contact to the LTC4085.

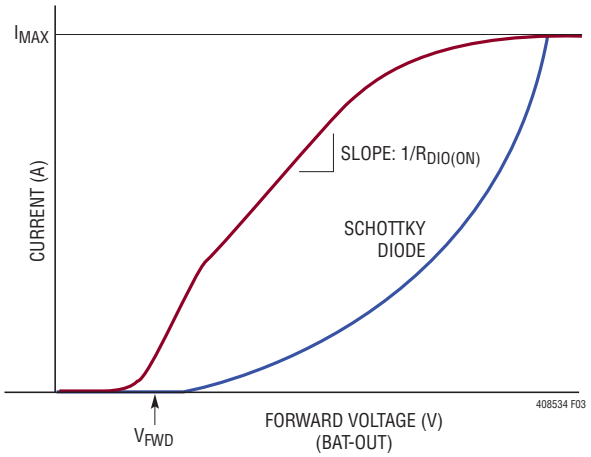


Figure 3. LTC4085 Schottky Diode vs Forward Voltage Drop

OPERATION

Battery Charger

The battery charger circuits of the LTC4085 are designed for charging single cell lithium-ion batteries. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage charge algorithm with programmable current and a programmable timer for charge termination. Charge current can be programmed up to 1.5A. The final float voltage accuracy is ±0.8% typical. No blocking diode or sense resistor is required when powering the IN pin. The $\overline{CHRG}$ open-drain status output provides information regarding the charging status of the LTC4085 at all times. An NTC input provides the option of charge qualification using battery temperature.

An internal thermal limit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature protects the LTC4085 from excessive temperature, and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LTC4085. Another benefit of the LTC4085 thermal limit is that charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

The charge cycle begins when the voltage at the OUT pin rises above the output UVLO level and the battery voltage is below the recharge threshold. No charge current actually flows until the OUT voltage is greater than the output UVLO level and 100mV above the BAT voltage. At the beginning of the charge cycle, if the battery voltage is below 2.8V, the charger goes into trickle charge mode to bring the cell voltage up to a safe level for charging. The charger goes into the fast charge constant-current mode once the voltage on the BAT pin rises above 2.8V. In constant-current mode, the charge current is set by R_{PROG}. When the battery approaches the final float voltage, the charge current begins to decrease as the LTC4085 switches to constant-voltage mode. When the charge current drops below 10% of the programmed charge current while in constant-voltage mode the $\overline{CHRG}$ pin assumes a high impedance state.

An external capacitor on the TIMER pin sets the total minimum charge time. When this time elapses the charge cycle terminates and the $\overline{CHRG}$ pin assumes a high impedance state, if it has not already done so. While charging in constant-current mode, if the charge current is decreased by thermal regulation or in order to maintain the programmed input current limit the charge time is automatically increased. In other words, the charge time is extended inversely proportional to charge current delivered to the battery. For Li-Ion and similar batteries that require accurate final float potential, the internal bandgap reference, voltage amplifier and the resistor divider provide regulation with ±0.8% accuracy.

Trickle Charge and Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is low (below 2.8V) the charger goes into trickle charge reducing the charge current to 10% of the full-scale current. If the low battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated and the $\overline{CHRG}$ pin output assumes a high impedance state. If for any reason the battery voltage rises above ~2.8V the charge cycle will be restarted. To restart the charge cycle (i.e. when the dead battery is replaced with a discharged battery), simply remove the input voltage and reapply it or cycle the TIMER pin to 0V.

OPERATION

Programming Charge Current

The formula for the battery charge current is:

$$I_{CHG} = (I_{PROG}) \bullet 50,000 = \frac{V_{PROG}}{R_{PROG}} \bullet 50,000$$

where V_{PROG} is the PROG pin voltage and R_{PROG} is the total resistance from the PROG pin to ground. Keep in mind that when the LTC4085 is powered from the IN pin, the programmed input current limit takes precedent over the charge current. In such a scenario, the charge current cannot exceed the programmed input current limit.

For example, if typical 500mA charge current is required, calculate:

$$R_{PROG} = \left(\frac{1V}{500mA}\right) \bullet 50,000 = 100k$$

For best stability over temperature and time, 1% metal film resistors are recommended. Under trickle charge conditions, this current is reduced to 10% of the full-scale value.

The Charge Timer

The programmable charge timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin. The charge time is typically:

$$t_{TIMER}(Hours) = \frac{C_{TIMER} \bullet R_{PROG} \bullet 3Hours}{0.1\mu F \bullet 100k}$$

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied or when leaving shutdown and the voltage on the battery is less than the recharge threshold. At power up or exiting shutdown with the battery voltage less than the recharge threshold the charge time is a full cycle. If the battery is greater than the recharge threshold the timer will not start and charging is prevented. If after power-up the battery voltage drops below the recharge threshold or if after a charge cycle the battery voltage is still below the recharge threshold the charge time is set to one half of a full cycle.

The LTC4085 has a feature that extends charge time automatically. Charge time is extended if the charge current in constant-current mode is reduced due to load current or thermal regulation. This change in charge time is inversely proportional to the change in charge current. As the LTC4085 approaches constant-voltage mode the charge current begins to drop. This change in charge current is due to normal charging operation and does not affect the timer duration.

Once a time-out occurs and the voltage on the battery is greater than the recharge threshold, the charge current stops, and the CHRG output assumes a high impedance state if it has not already done so.

Connecting the TIMER pin to ground disables the battery charger.

$\overline{\text{CHRG}}$ Status Output Pin

When the charge cycle starts, the $\overline{\text{CHRG}}$ pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. When the charge current drops below 10% of the programmed full charge current while in constant-voltage mode, the pin assumes a high impedance state (but charge current continues to flow until the charge time elapses). If this state is not reached before the end of the programmable charge time, the pin will assume a high impedance state when a time-out occurs. The $\overline{\text{CHRG}}$ current detection threshold can be calculated by the following equation:

$$I_{DETECT} = \frac{0.1V}{R_{PROG}} \bullet 50,000 = \frac{5000V}{R_{PROG}}$$

OPERATION

For example, if the full charge current is programmed to 500mA with a 100k PROG resistor the $\overline{CHRG}$ pin will change state at a battery charge current of 50mA.

Note: The end-of-charge (EOC) comparator that monitors the charge current latches its decision. Therefore, the first time the charge current drops below 10% of the programmed full charge current while in constant-voltage mode will toggle $\overline{CHRG}$ to a high impedance state. If, for some reason, the charge current rises back above the threshold the $\overline{CHRG}$ pin will not resume the strong pull-down state. The EOC latch can be reset by a recharge cycle (i.e. V_{BAT} drops below the recharge threshold) or toggling the input power to the part.

Current Limit Undervoltage Lockout

An internal undervoltage lockout circuit monitors the input voltage and disables the input current limit circuits until V_{IN} rises above the undervoltage lockout threshold. The current limit UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the current limit UVLO circuit disables the current limit (i.e. forces the input power path to a high impedance state) if V_{OUT} exceeds V_{IN}. If the current limit UVLO comparator is tripped, the current limit circuits will not come out of shutdown until V_{OUT} falls 50mV below the V_{IN} voltage.

Charger Undervoltage Lockout

An internal undervoltage lockout circuit monitors the V_{OUT} voltage and disables the battery charger circuits until V_{OUT} rises above the undervoltage lockout threshold. The battery charger UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the charger UVLO circuit keeps the charger shut down if V_{BAT} exceeds V_{OUT}. If the charger UVLO comparator is tripped, the charger circuits will not come out of shutdown until V_{OUT} exceeds V_{BAT} by 50mV. Finally, the LTC4085-3 will attempt to prevent a V_{OUT} UVLO condition by reducing charge current when V_{OUT} falls below approximately 4.45V. Charge current is reduced to zero when V_{OUT} falls to approximately 4.2V. The LTC4085-4 does not include this Undervoltage Current Limit feature.

Suspend

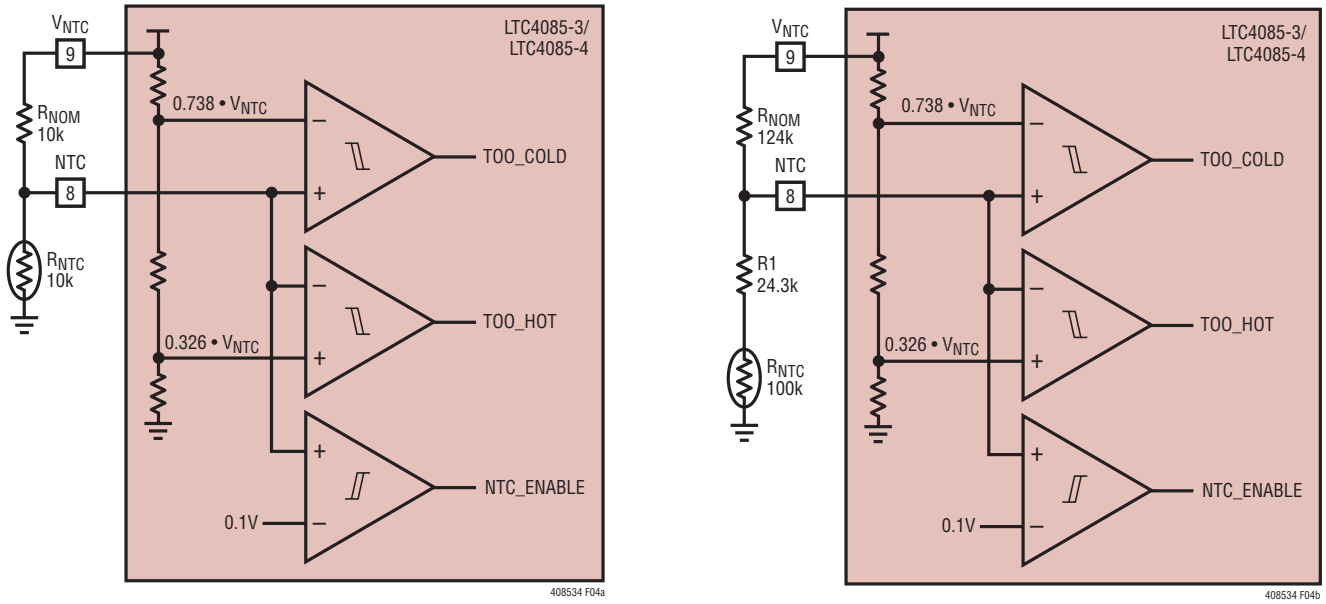
The LTC4085 can be put in suspend mode by forcing the SUSP pin greater than 1.2V. In suspend mode the ideal diode function from BAT to OUT is kept alive. If power is applied to the OUT pin externally (i.e., a wall adapter is present) then charging will be unaffected. Current drawn from the IN pin is reduced to 50µA. Suspend mode is intended to comply with the USB power specification mode of the same name.

NTC Thermistor—Battery Temperature Charge Qualification

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 4.

To use this feature, connect the NTC thermistor (R_{NTC}) between the NTC pin and ground and a resistor (R_{NOM}) from the NTC pin to VNTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (this value is 10k for a Vishay NTHS0603N02N1002J thermistor). The LTC4085 goes into hold mode when the resistance (R_{HOT}) of the NTC thermistor drops to 0.48 times the value of R_{NOM}, or approximately 4.8k, which should be at 45°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4085 is designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of R_{NOM}. This resistance is R_{COLD}. For a Vishay NTHS0603N02N1002J thermistor, this value is 28.2k which corresponds to approximately 0°C. The hot and cold comparators each have approximately 2°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin will disable the NTC function.

APPLICATIONS INFORMATION



(4a) (4b)

Figure 4. NTC Circuits

Alternate NTC Thermistors

The LTC4085 NTC trip points were designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's "R-T Curve 2." The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 2" characteristic in a variety of sizes. Furthermore, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 6.0 will also work (Vishay Dale R-T Curve 2 shows a ratio of 2.816/0.4839 = 5.82).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 1." Using these as indicated in the NTC Thermistor section will give temperature trip points of approximately 3°C and 42°C, a delta of 39°C. This delta in temperature can be moved in either direction by changing the value of R_{NOM} with respect to R_{NTC}. Increasing R_{NOM} will move both trip points to lower temperatures. Likewise, a decrease in R_{NOM} with respect to R_{NTC} will move the trip points to higher temperatures.

To calculate R_{NOM} for a shift to lower temperature, for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.816} \bullet R_{NTC} \text{ at } 25°C$$

where R_{COLD} is the resistance ratio of R_{NTC} at the desired cold temperature trip point. To shift the trip points to higher temperatures use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.484} \bullet R_{NTC} \text{ at } 25°C$$

where R_{HOT} is the resistance ratio of R_{NTC} at the desired hot temperature trip point.

The following example uses a 100k R-T Curve 1 Thermistor from Vishay Dale. The difference between the trip points is 39°C, from before—and the desired cold trip point of 0°C, would put the hot trip point at about 39°C. The R_{NOM} needed is calculated as follows:

$$R_{NOM} = \frac{R_{COLD}}{2.816} \bullet R_{NTC} \text{ at } 25°C =$$

$$\frac{3.266}{2.816} \bullet 100k\Omega = 116k\Omega$$

APPLICATIONS INFORMATION

The nearest 1% value for R_{NOM} is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 39°C, respectively. To extend the delta between the cold and hot trip points, a resistor (R1) can be added in series with R_{NTC} (see Figure 4). The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.816 - 0.484}$$

$$R1 = \left[\frac{0.484}{2.816 - 0.484}\right] \bullet \left[R_{COLD} - R_{HOT}\right] - R_{HOT}$$

where R_{NOM} is the value of the bias resistor, R_{HOT} and R_{COLD} are the values of R_{NTC} at the desired temperature trip points. Continuing the forementioned example with a desired hot trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.816 - 0.484}$$

$$= \frac{100k \bullet (3.266 - 0.3602)}{2.816 - 0.484}$$

$$= 124.6k, 124k \text{ nearest } 1\%$$

$$R1 = 100k \bullet \left[\left(\frac{0.484}{2.816 - 0.484}\right) \bullet \frac{}{(3.266 - 0.3602) - 0.3602}\right]$$

$$= 24.3k$$

The final solution is shown in Figure 4, where R_{NOM} = 124k, R1 = 24.3k and R_{NTC} = 100k at 25°C

Using the WALL Pin to Detect the Presence of a Wall Adapter

The WALL input pin identifies the presence of a wall adapter (the pin should be tied directly to the adapter output voltage). This information is used to disconnect the input pin, IN, from the OUT pin in order to prevent back conduction to whatever may be connected to the input. It also forces the $\overline{ACPR}$ pin low when the voltage at the WALL pin exceeds the input threshold. In order for the presence of a wall adapter to be acknowledged, both of the following conditions must be satisfied:

1. The WALL pin voltage exceeds V_{WAR} (approximately 4.25V); and
2. The WALL pin voltage exceeds V_{WDR} (approximately 75mV above V_{BAT})

The input power path (between IN and OUT) is re-enabled and the $\overline{ACPR}$ pin assumes a high impedance state when either of the following conditions is met:

1. The WALL pin voltage falls below V_{WDF} (approximately 25mV above V_{BAT}); or
2. The WALL pin voltage falls below V_{WAF} (approximately 3.12V)

Each of these thresholds is suitably filtered in time to prevent transient glitches on the WALL pin from falsely triggering an event.

Power Dissipation

The conditions that cause the LTC4085 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the part. For high charge currents and a wall adapter applied to V_{OUT}, the LTC4085 power dissipation is approximately:

$$P_D = (V_{OUT} - V_{BAT}) \bullet I_{BAT}$$

APPLICATIONS INFORMATION

Where, P_D is the power dissipated, V_{OUT} is the supply voltage, V_{BAT} is the battery voltage, and I_{BAT} is the battery charge current. It is not necessary to perform any worst-case power dissipation scenarios because the LTC4085 will automatically reduce the charge current to maintain the die temperature at approximately 105°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 105°C – P_D • \theta_{JA}$$

$$T_A = 105°C – (V_{OUT} – V_{BAT}) • I_{BAT} • \theta_{JA}$$

Example: Consider an LTC4085 operating from a wall adapter with 5V at V_{OUT} providing 0.8A to a 3V Li-Ion battery. The ambient temperature above which the LTC4085 will begin to reduce the 0.8A charge current, is approximately

$$T_A = 105°C – (5V – 3V) • 0.8A • 43°C/W$$

$$T_A = 105°C – 1.6W • 43°C/W = 105°C – 69°C = 36°C$$

The LTC4085 can be used above 36°C, but the charge current will be reduced below 0.8A. The charge current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{105°C – T_A}{(V_{OUT} – V_{BAT}) • \theta_{JA}}$$

Consider the above example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{BAT} = \frac{105°C – 55°C}{(5V – 3V) • 43°C/W} = \frac{50°C}{86°C/A} = 0.58A$$

Board Layout Considerations

In order to be able to deliver maximum charge current under all conditions, it is critical that the Exposed Pad on the backside of the LTC4085 package is soldered to the board. Correctly soldered to a 2500mm^2 double-sided 1oz. copper board the LTC4085 has a thermal resistance of approximately 43°C/W. Failure to make thermal contact between the Exposed Pad on the backside of the package and the copper board will result in thermal resistances far greater than 43°C/W. As an example, a correctly soldered LTC4085 can deliver over 1A to a battery from a 5V supply at room temperature. Without a backside thermal connection, this number could drop to less than 500mA.

V_{IN} and Wall Adapter Bypass Capacitor

Many types of capacitors can be used for input bypassing. However, caution must be exercised when using multilayer ceramic capacitors. Because of the self resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a hot power source. For more information, refer to Application Note 88.

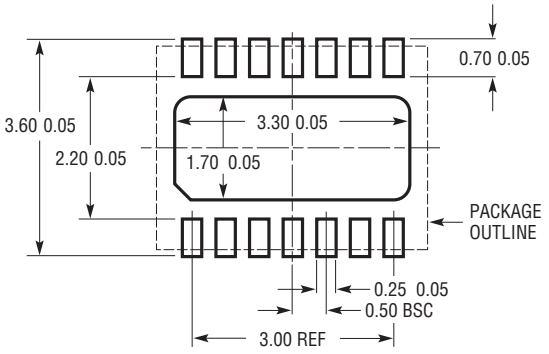
Stability

The constant-voltage mode feedback loop is stable without any compensation when a battery is connected. However, a 4.7µF capacitor with a 1Ω series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

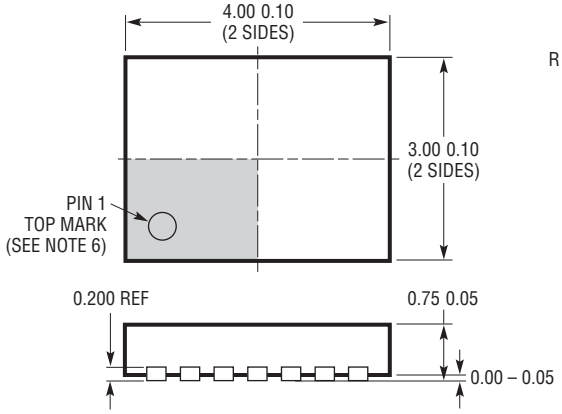
PACKAGE DESCRIPTION

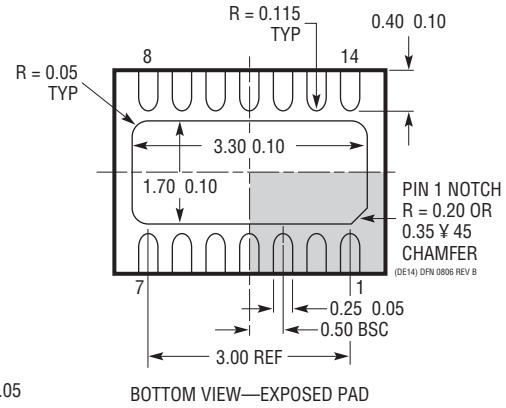
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

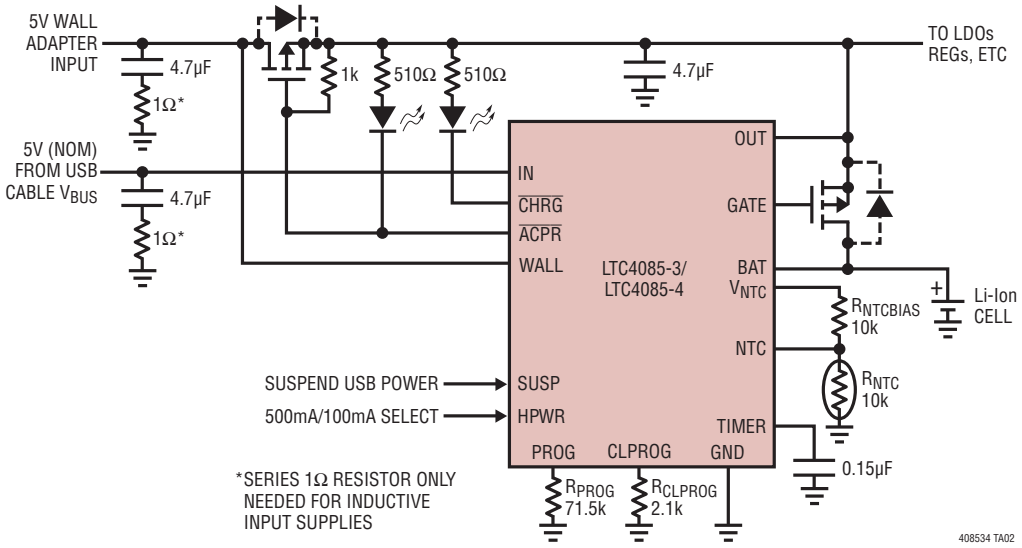
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/10	Updated Block Diagram	10
B	5/12	Added new part number LTC4085-4	throughout
		Added feature bullet for LTC4085-3 version	1
		Added table of product options	2
		Enhanced Note 5 to add testing conditions	4
		Enhanced Charger Undervoltage Lockout section for LTC4085-3 version	18

TYPICAL APPLICATION

USB Power Control Application with Wall Adapter Input



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Battery Chargers		
LTC4065/LTC4065A	Standalone Li-Ion Battery Chargers in 2 × 2 DFN	4.2V, ±0.6% Float Voltage, Up to 750mA Charge Current, 2mm × 2mm DFN, "A" Version has $\overline{\text{ACPR}}$ Function.
LTC4095	Standalone LSB Li-Ion Polymer Battery Charger 2mm × 2mm DFN	950µA Charge Current, Timer Termination +C/10 Detection Output, 4.2V ±0.6% Accurate Float Voltage 4 $\overline{\text{CHRG}}$ Pin Indicator States
Power Management		
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	Seamless Transition Between Power Souces: USB, Wall Adapter and Battery; 95% Efficient DC/DC Conversion
LTC4055	USB Power Controller and Battery Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode, 4mm × 4mm QFN16 Package
LTC4066	USB Power Controller and Battery Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 50mΩ Ideal Diode, 4mm × 4mm QFN24 Package
LTC4085	USB Power Manager with Ideal Diode Controller and Li-Ion Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ Option, 4mm × 3mm DFN14 Package
LTC4089/LTC4089-1/ LTC4089-5	High Voltage USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger	High Efficiency 1.2A Charger from 6V to 36V (40V max) Input Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation; 200mΩ Ideal Diode with <50mΩ option, 3mm × 4mm DFN-14 Package, Bat-Track™ Adaptive Output Control (LTC4089/-1); Fixed 5V Output (LTC4089-5) "-1" for 4.1V Float Voltage Batteries
LTC4090	High Voltage USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger	High Efficiency 1.2A Charger from 6V to 36V (60V max) Input Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation; 200mΩ Ideal Diode with <50mΩ option, 3mm × 4mm DFN-14 Package, Bat-Track Adaptive Output Control
LTC4411/LTC4412	Low Loss PowerPath Controller in ThinSOT	Automatic Switching Between DC Sources, Load Sharing, Replaces ORing Diodes

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