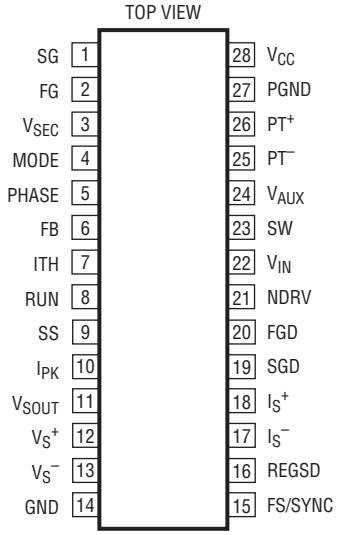
ABSOLUTE MAXIMUM RATINGS (Note 1)

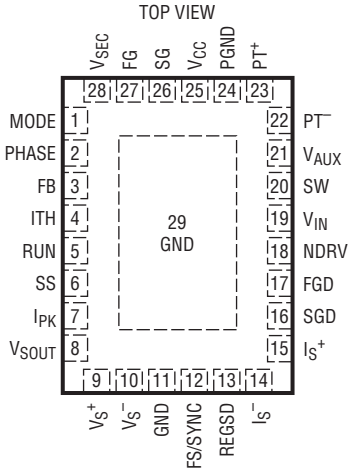
V_{CC} Voltage ..... –0.3V to 12V
V_{IN} Voltage ..... –0.3V to 33V
RUN Voltage ..... –0.3V to 33V
SW
  Low Impedance Source ..... –5V to 40V
  Current Fed ..... 2mA DC or 0.2A for <1µs Into Pin*
V_{AUX}, V_S^+, V_S^-, V_{SOUT}, NDRV Voltages ..... –0.3V to 16V
ITH, I_S^+, REGSD Voltages ..... –0.3V to 6V
PHASE Voltage ..... –0.3V to 6V
I_S^-, SGD, FGD Voltages ..... –0.3V to 12V
FS/SYNC, FB, MODE Voltages ..... –0.3V to 12V
V_{SEC} Voltage ..... –0.3V to 3V
I_{PK}, SS Voltages ..... –0.3V to 4V
Operating Junction Temperature Range (Notes 2,3)
  LTC3766E, LTC3766I ..... –40°C to 125°C
  LTC3766H ..... –40°C to 150°C
  LTC3766MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  GN Package ..... 300°C

*The LTC3766 contains an internal 50V clamp that limits the voltage on the SW pin.

PIN CONFIGURATION



GN PACKAGE
28-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

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ORDER INFORMATION

http://www.linear.com/product/LTC3766#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3766EGN#PBF	LTC3766EGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC3766IGN#PBF	LTC3766IGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC3766HGN#PBF	LTC3766HGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–40°C to 150°C
LTC3766MPGN#PBF	LTC3766MPGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–55°C to 150°C
LTC3766EUFD#PBF	LTC3766EUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3766IUFD#PBF	LTC3766IUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3766HUFD#PBF	LTC3766HUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
LTC3766MPUFD#PBF	LTC3766MPUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Regulated Feedback Voltage	(Note 4) ITH = 1.2V	●	0.592	0.600	0.608	V
I_{FB}	Feedback Input Current	(Note 4)			2	50	nA
$\Delta V_{FB(LINREG)}$	Feedback Voltage Line Regulation	V_{IN} = 5V to 32V, ITH = 1.2V			0.001		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	Measured in Servo Loop, ITH = 0.5V to 2V	●		–0.01	–0.1	%
V_{ISAVG}	Average Current Sense Threshold	Resistor Sense (RS) Mode Current Transformer (CT) Mode		47 0.66	55 0.73	63 0.80	mV V
V_{ISADJ}	Current Sense Ripple Compensation	RS Mode CT Mode V_{SW} = 10V, V_S^+ = 5V, FS/SYNC = V_{CC}, R_{IPK} = 23.7k			10 140		mV mV
V_{ISOC}	Overcurrent Shutdown Threshold	RS Mode: V_{IS}^- = 0V CT Mode: V_{IS}^- = V_{CC}		86 1.22	100 1.33	113 1.44	mV V
I_{SIN}	I_S^+ and I_S^- Input Current				280	500	nA
g_m	Error Amplifier g_m			2.2	2.7	3.2	mS
R_{EA}	Error Amplifier Output Resistance	(Note 7)			5		MΩ
$I_{SOFT(C)}$	Soft-Start Charge Current	V_{SS} = 2V		4	5	6	µA
$I_{SOFT(D)}$	Soft-Start Discharge Current	V_{SS} = 2V			3		µA
V_{RUNR}	RUN Pin On Threshold	V_{RUN} Rising	●	1.18	1.22	1.26	V
V_{RUNF}	RUN Pin Off Threshold	V_{RUN} Falling	●	1.13	1.17	1.21	V
I_{RUN}	RUN Pin Hysteresis Current	V_{RUN} = 0.5V		2.2	3.0	3.6	µA
$t_{ON(MIN)}$	Minimum Controllable On Time				200		ns
D_{MAX}	Maximum Duty Cycle	FGD = SGD = GND		77	79	81	%
$\Delta V_{SEC(TH)}$	Volt-Second Limit Threshold Accuracy	2V ≤ V_{SW} < 5V 5V ≤ V_{SW} ≤ 40V		–6 –4		6 4	% %
R_{VSDN}	Volt-Second Discharge Resistance				75		Ω
V_{SWCL}	SW Clamp Voltage	I_{SW} = 1mA		43	51	60	V
$\Delta V_{FB(OV)}$	Output Overvoltage Threshold	V_{FB} Rising		15	17	19	%

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Drivers and Control							
FG, SG R_{UP}	FG, SG Driver Pull-Up On-Resistance				1.5		Ω
FG, SG R_{DOWN}	FG, SG Driver Pull-Down On-Resistance				1.0		Ω
PT^+, PT^- R_{UP}	PT^+, PT^- Driver Pull-Up Resistance				1.5		Ω
PT^+,PT^- R_{DOWN}	PT^+, PT^- Driver Pull-Down Resistance				1.5		Ω
t_{FGD}	FGD Delay	R_{FGD} = 10kΩ R_{FGD} = 100kΩ		50 436	65 545	80 654	ns ns
t_{SGD}	SGD Delay	R_{SGD} = 15kΩ R_{SGD} = 50kΩ		60 195	75 230	90 265	ns ns
$V_{SW(REV)}$	SG Reverse Overcurrent SW Threshold	LV MODE HV MODE		66 140	73 148	79 156	mV mV
$I_{SW(REV)}$	SG Reverse Overcurrent Adjust Current	LV MODE HV MODE		–86 –34.5	–103 –42	–120 –49	µA µA
V_{CC} Supply							
V_{CCOP}	V_{CC} Operating Voltage Range			5		10	V
I_{CC}	Supply Current Normal Mode Shutdown	 $V_{FS/SYNC}$ = V_{CC} = 7V (Note 5) V_{RUN} = GND			 5 210		 mA µA
V_{UVLOR}	UV Lockout Rising	V_{CC} Rising, LV MODE V_{CC} Rising, HV MODE	● ●	4.6 7.7	4.7 7.9	4.8 8.1	V V
V_{UVLOF}	UV Lockout Falling	V_{CC} Falling, LV MODE V_{CC} Falling, HV MODE	● ●	3.8 6.7	3.9 6.9	4.0 7.1	V V
V_{REGSD}	REGSD Threshold Voltage	V_{REGSD} Rising			1.21		V
$I_{REGSD(C)}$	REGSD Charge Current	V_{REGSD} = 0.7V			13		µA
$I_{REGSD(D)}$	REGSD Discharge Current	V_{REGSD} = 0.7V			3		µA
V_{AUX} Supply							
V_{AUXOP}	V_{AUX} Operating Voltage Range			5		15	V
V_{CCVAUX}	Regulated V_{CC} Output Voltage	V_{AUX} = 15V, LV MODE V_{AUX} = 15V, HV MODE		6.7 8.1	7.0 8.5	7.3 8.9	V V
V_{AUXLR}	V_{CC} Load Regulation	I_{CC} = 0mA to 120mA, V_{AUX} = 8V, LV MODE			0.8	2	%
V_{AUXSWP}	V_{AUX} Switchover Voltage Rising	V_{AUX} Ramping Positive, LV MODE V_{AUX} Ramping Positive, HV MODE		4.50 7.65	4.70 8.00	4.88 8.35	V V
V_{AUXSWN}	V_{AUX} Switchover Voltage Falling	V_{AUX} Ramping Negative, LV MODE V_{AUX} Ramping Negative, HV MODE		4.30 7.35	4.50 7.70	4.70 8.05	V V
R_{AUX}	V_{AUX} Dropout Resistance	I_{CC} = 120mA, V_{AUX} = 4.9V			1.7	2.5	Ω
R_{PSL}	V_{AUX} Pre-Switchover Load	V_{AUX} = 4V			920		Ω
V_{IN} Supply							
V_{INOP}	V_{IN} Operating Voltage Range			5		32	V
V_{INCL}	V_{IN} Clamp Voltage	I_{VIN} = 2mA, V_{RUN} = GND		28	30	32	V
I_{CLMAX}	V_{IN} Clamp Current Limit	V_{IN} = 33V, V_{RUN} = GND		3.8	5.5	7.2	mA
V_{CCVIN}	Regulated V_{CC} Output Voltage	LV MODE (Note 6) HV MODE (Note 6)		6.7 8.1	7.2 8.5	7.3 8.9	V V
I_{IN}	Supply Current Operating Shutdown	 $V_{FS/SYNC}$ = V_{CC} V_{RUN} = GND			 900 450	 1200	 µA µA
V_{INUVLO}	V_{IN} Undervoltage Lockout	V_{IN} Rising		2.6	3.2	3.8	V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
$I_{FS/SYNC}$	FS/SYNC Pin Sourcing Current				20		µA
f_{HIGH}	Oscillator High Frequency Set Point	$V_{FS/SYNC} = V_{CC}$		234	275	316	kHz
Δf ($R_{FS/SYNC}$)	Oscillator Resistor Set Accuracy	18.75kΩ < $R_{FS/SYNC}$ < 125kΩ	●	–12		12	%
$f_{PLL(RANGE)}$	PLL Sync Frequency Range			100		500	kHz
Differential Amplifier							
A_{DA}	Gain	1.5V ≤ V_{SOUT} ≤ 15V, V_{IN} = 20V		0.99	1	1.01	V/V
$CMRR_{DA}$	Common Mode Rejection Ratio	V_{IN} = 20V			75		dB
R_{INP}	V_S^+ Input Resistance	V_{IN} = 20V			120		kΩ
R_{INM}	V_S^- Input Resistance	V_{IN} = 20V			160		kΩ
I_{OH}	Output Sourcing Current	V_{IN} = 20V, V_S^+ = 5V, V_{SOUT} = 2.5V	●	0.8	3.0		mA
V_{IN}-V_{OHST}	Output High Fault Threshold	V_S^+ Rising			1.2	1.5	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3766E is guaranteed to meet specifications from 0°C to 85°C with specifications over the –40°C to 125°C operating junction temperature range assured by design, characterization and correlation with statistical process controls. The LTC3766I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3766H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC3766MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$$

where θ_{JA} is 95°C/W for the SSOP and 43°C/W for the QFN package.

Note 4: The LTC3766 is tested in a feedback loop that servos V_{FB} to a voltage near the internal 0.6V reference voltage to obtain the specified ITH voltage (V_{ITH} = 1.2V).

Note 5: Operating supply current is measured in test mode. Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency. See Typical Performance Characteristics.

Note 6: The V_{IN} Regulator employs an external pass device to produce the regulated V_{CC} output voltage. The LTC3766 is tested using a 2N3904 NPN transistor as an external pass device.

Note 7: Guaranteed by design.

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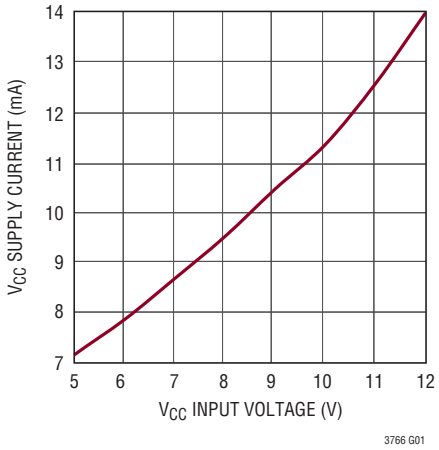
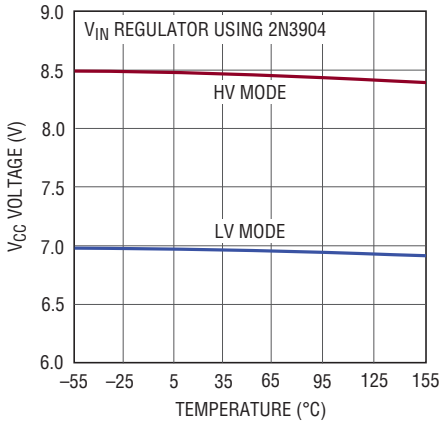
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} Supply Current vs V_{CC} Voltage



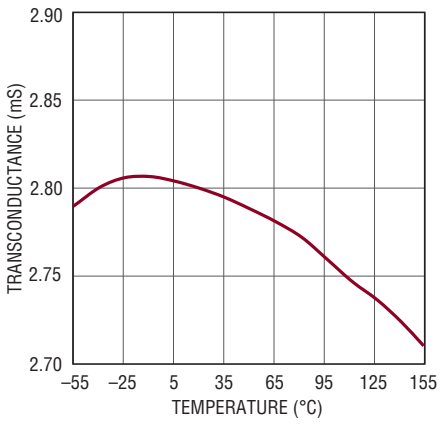
3766 G01

V_{CC} Regulator Output Voltage vs Temperature



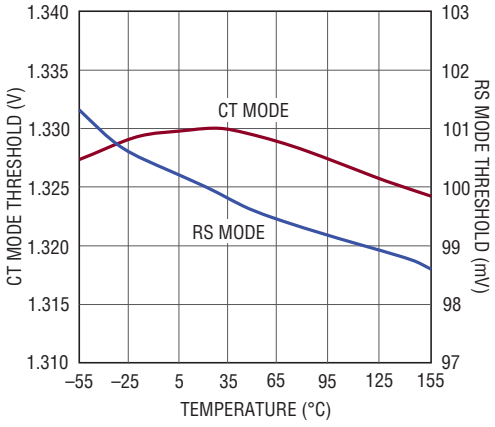
3766 G02

Error Amplifier Transconductance vs Temperature



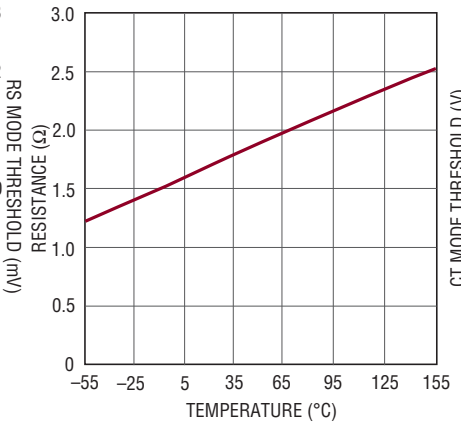
3766 G03

Overcurrent Shutdown Threshold vs Temperature



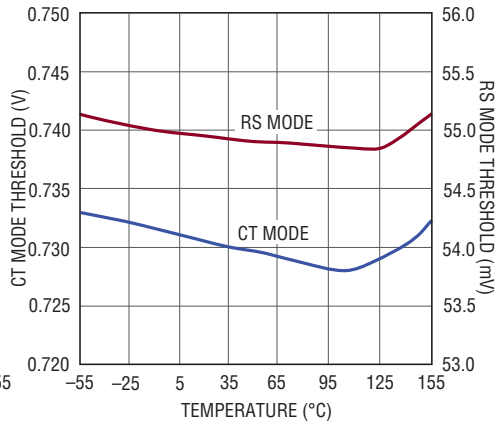
3766 G04

V_{AUX} Drop-Out Resistance vs Temperature



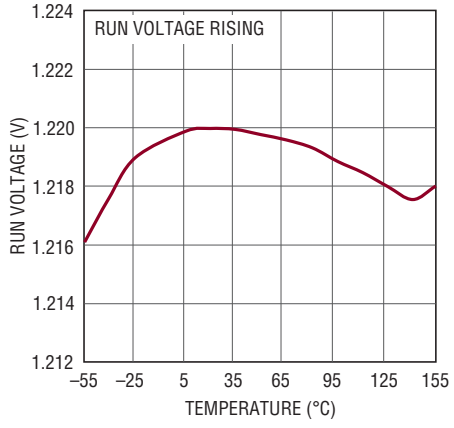
3766 G05

Average Current Sense Threshold vs Temperature



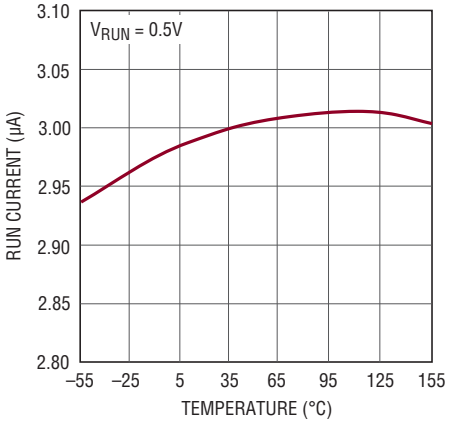
3766 G06

RUN Threshold vs Temperature



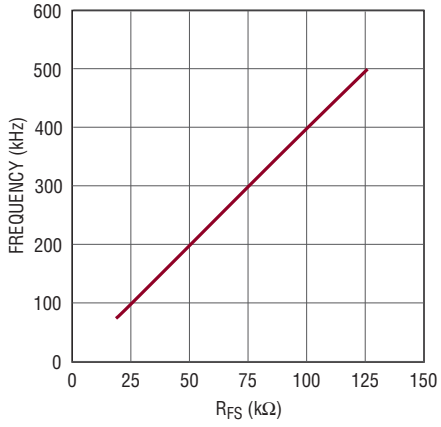
3766 G07

RUN Hysteresis Current vs Temperature



3766 G08

Oscillator Frequency vs R_{FS}



3766 G09

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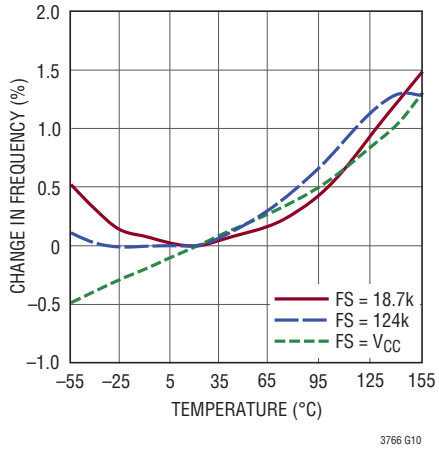
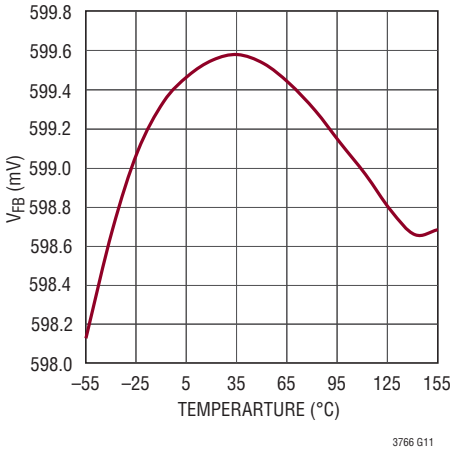
TYPICAL PERFORMANCE CHARACTERISTICS

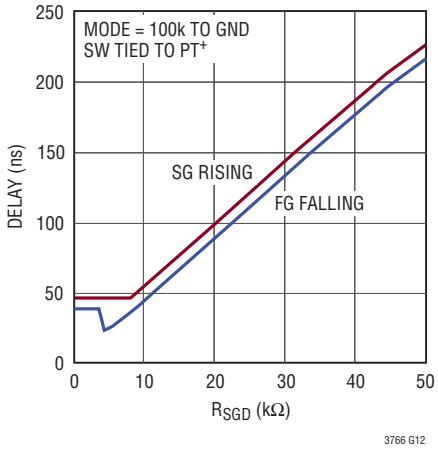
Oscillator Frequency vs Temperature



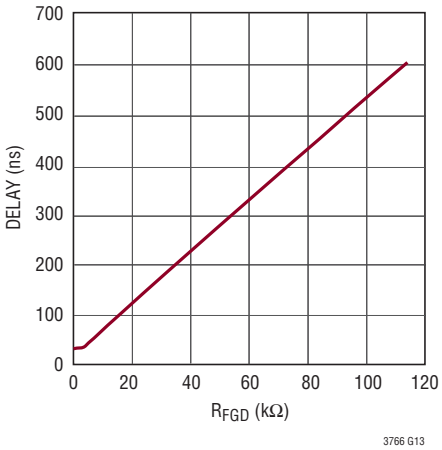
FB Voltage vs Temperature



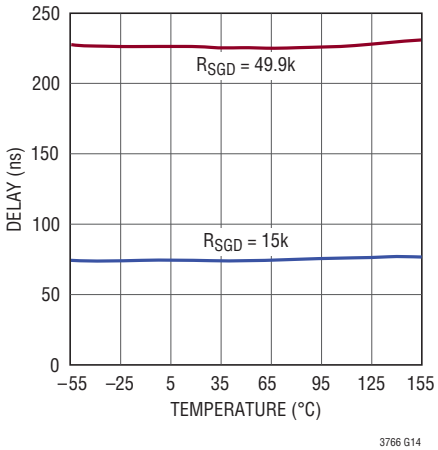
SGD Delay vs Resistance



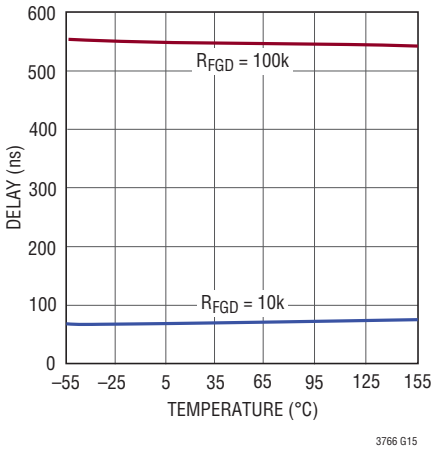
FGD Delay vs Resistance



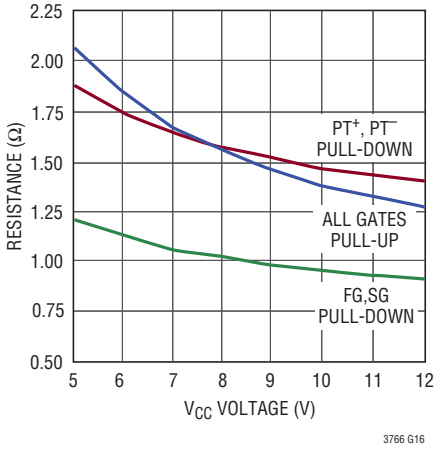
SGD Delay vs Temperature



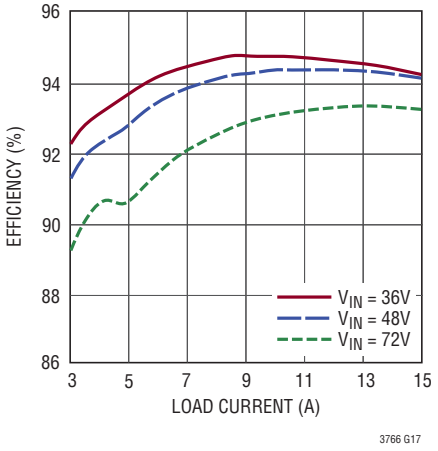
FGD Delay vs Temperature



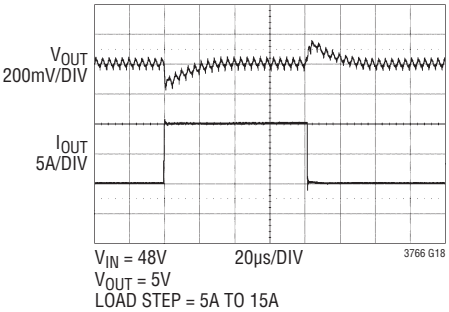
Gate Driver On-Resistance vs V_{CC} Voltage



Efficiency (Figure 39 Circuit)



Load Step (Figure 39 Circuit)



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PIN FUNCTIONS (SSOP/QFN)

SG (Pin 1/Pin 26): Gate Drive for the Synchronous MOSFET.

FG (Pin 2/Pin 27): Gate Drive for the Forward MOSFET.

V_{SEC} (Pin 3/Pin 28): Volt-Second Limit. Connect a resistor from SW to V_{SEC}, and a capacitor from V_{SEC} to GND to set the maximum volt-second product that is applied to the main power transformer. The PWM on-time is terminated when the V_{SEC} voltage exceeds the internally generated threshold. Tie to GND if not used.

MODE (Pin 4/Pin 1): For normal isolated applications using the LTC3765, tie to either GND or V_{CC} to set the operating voltage to either low voltage or high voltage modes respectively, as needed to drive the gates of the synchronous and forward MOSFETs. For nonisolated applications, tie to ground through either a 100k or 50k resistor to activate standalone mode (for low voltage or high voltage operation respectively). In this mode, the PT^+ pin may be directly connected to the gate of a primary-side MOSFET, and a reference clock signal is generated on the PT^- pin. In standalone mode, the FGD pin is ignored and the associated delay is set adaptively.

PHASE (Pin 5/Pin 2): Control Input to the Phase Selector. This pin determines the phasing of the internal controller CLK relative to the synchronizing signal at the FS/SYNC pin.

FB (Pin 6/Pin 3): The Inverting Input of the Main Loop Error Amplifier. Tie to V_{CC} or other voltage greater than 2.5V to enable slave mode in PolyPhase applications.

ITH (Pin 7/Pin 4): The Output of the Main Loop Error Amplifier. Place compensation components between the ITH pin and GND.

RUN (Pin 8/Pin 5): Run Control Input. Holding this pin below 1.22V will shut down the IC and reset the soft-start and REGSD pins to 0V.

SS (Pin 9/Pin 6): Soft-Start Inputs. A capacitor to ground sets the ramp time of the output voltage.

I_{PK} (Pin 10/Pin 7): Peak Current Limit Inductor Ripple Cancellation. This pin is used to adjust the peak current limit based on the amount of inductor current ripple, thereby providing a constant average output current during current limit. Place a resistor to GND that is proportional to the main output inductor. Leave this pin floating for constant peak current limit. Minimize parasitic capacitance on this pin.

V_{SOUT}, V_S^+, V_S^- (Pins 11, 12, 13/Pins 8, 9, 10): V_{SOUT} is the output of a precision, unity-gain differential amplifier. Tie V_S^+ and V_S^- to the output of the main DC/DC converter to achieve true remote differential sensing. Also, V_S^+ is used for directly sensing the output voltage for inductor ripple cancellation. Do not exceed the output sourcing current specification on the V_{SOUT} pin or a fault will be generated. See the Applications Information section for details.

GND (Pin 14/Pin 11, Exposed Pad Pin 29): Signal Ground and Kelvin Sense for SG Reverse Overcurrent. Connect to power ground at the source of the synchronous MOSFET. The exposed pad must be soldered to PCB ground for rated thermal performance.

FS/SYNC (Pin 15/Pin 12): Combination Frequency Set and Sync Pin. Tie to V_{CC} to run at 275kHz. Place a resistor to ground at this pin to set the frequency between 75kHz and 500kHz. To synchronize, drive this pin with a clock signal to achieve PLL synchronization from 100kHz to 500kHz. Sources 20µA of current.

REGSD (Pin 16/Pin 13): Regulator Shutdown Timer. Place a capacitor to ground to limit the time allowed for the high voltage linear regulator controller to operate. When the REGSD voltage exceeds 1.21V, the linear regulator is shut down. This pin sources 13µA of current when the linear regulator is active.

I_S^- (Pin 17/Pin 14): Negative Input to the Current Sense Circuit. Connect to the negative end of a low side current sense resistor. When using a current sense transformer, tie this pin to V_{CC} for single-ended sensing on I_S^+ with a higher maximum trip level.

I_S^+ (Pin 18/Pin 15): Positive Input to the Current Sense Circuit. Connect to the positive end of a low side current sense resistor or to the output of a current sense transformer.

SGD (Pin 19/Pin 16): Synchronous Gate Rising Edge Delay. A resistor to GND sets the delay from primary gate turn-off (PT^+ falling) to SG rising (and FG falling). This delay is used to optimize the dead time between the turn-off of the primary-side MOSFET and the turn-on of SG. Tie SGD to GND to set this delay adaptively based on the falling edge of the SW pin voltage. See Setting the Gate Driver Delays in the Applications Information section.

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PIN FUNCTIONS (SSOP/QFN)

FGD (Pin 20/Pin 17): Forward Gate Rising Edge Delay. A resistor to GND sets the delay from PT^+ rising to FG rising (and SG falling). This delay is used to optimize the dead time between the turn-off of SG and the turn-on of the primary-side MOSFET. In standalone mode (100k or 50k resistor on MODE), this dead time is set adaptively and the FGD pin can be grounded. See Setting the Gate Driver Delays in the Applications Information section.

NDRV (Pin 21/Pin 18): Drive Output for the External Pass Device of the High Voltage Linear Regulator Controller. Connect to the base (NPN) or gate (MOSFET) of an external N-type device. Tie to V_{CC} pin if only using the internal LDO (V_{AUX} pin).

V_{IN} (Pin 22/Pin 19): Connect to a higher voltage bias supply when using the linear regulator controller. The V_{IN} pin supplies bias to the internal standby and monitoring circuits, the linear regulator controller, and the differential amplifier. Tie to V_{AUX} pin if only using the internal LDO.

SW (Pin 23/Pin 20): Connect (Kelvin) to the drain of the synchronous MOSFET. This input is used for adaptive shoot-through prevention and leading-edge blanking, monitoring the high level SW node voltage and SG reverse-current protection. When SW is high, the voltage on this pin is internally measured for use in the inductor ripple cancellation and volt-second limit circuits. When SW is low and SG is high, this pin sources a small current and is used for SG reverse overcurrent protection. A resistor can be placed between the SW pin and the drain of the synchronous MOSFET to adjust the SG reverse-over current threshold. The SW pin is internally clamped to 50V.

V_{AUX} (Pin 24/Pin 21): Auxiliary Power Input. This is the power input to an internal LDO that is connected to V_{CC}. Whenever V_{AUX} is greater than 4.7V (or 8V for high voltage mode), this LDO will supply power to V_{CC}, bypassing the main linear regulator that is powered from V_{IN}. See V_{AUX} Connection in the Applications Information section. Do not exceed 16V on the V_{AUX} pin.

PT^-, PT^+ (Pin 25, 26/Pin 22, 23): Pulse Transformer Driver Outputs. For most applications, these connect to a pulse transformer through a series DC-blocking capacitor. The PWM information is multiplexed together with DC power and sent through the pulse transformer to the primary side. The PWM signal is then decoded by the LTC3765 active clamp forward controller and gate driver. In standalone mode (100k or 50k resistor on MODE), the PT^+ pin has a standard PWM signal and may be directly connected to the gate of a primary-side MOSFET, while a reference clock is generated on the PT^- pin.

PGND (Pin 27/Pin 24): Gate Driver Ground Pin. Connect to power ground at the source of the synchronous MOSFET.

V_{CC} (Pin 28/Pin 25): Main V_{CC} Input for All Driver and Control Circuitry.

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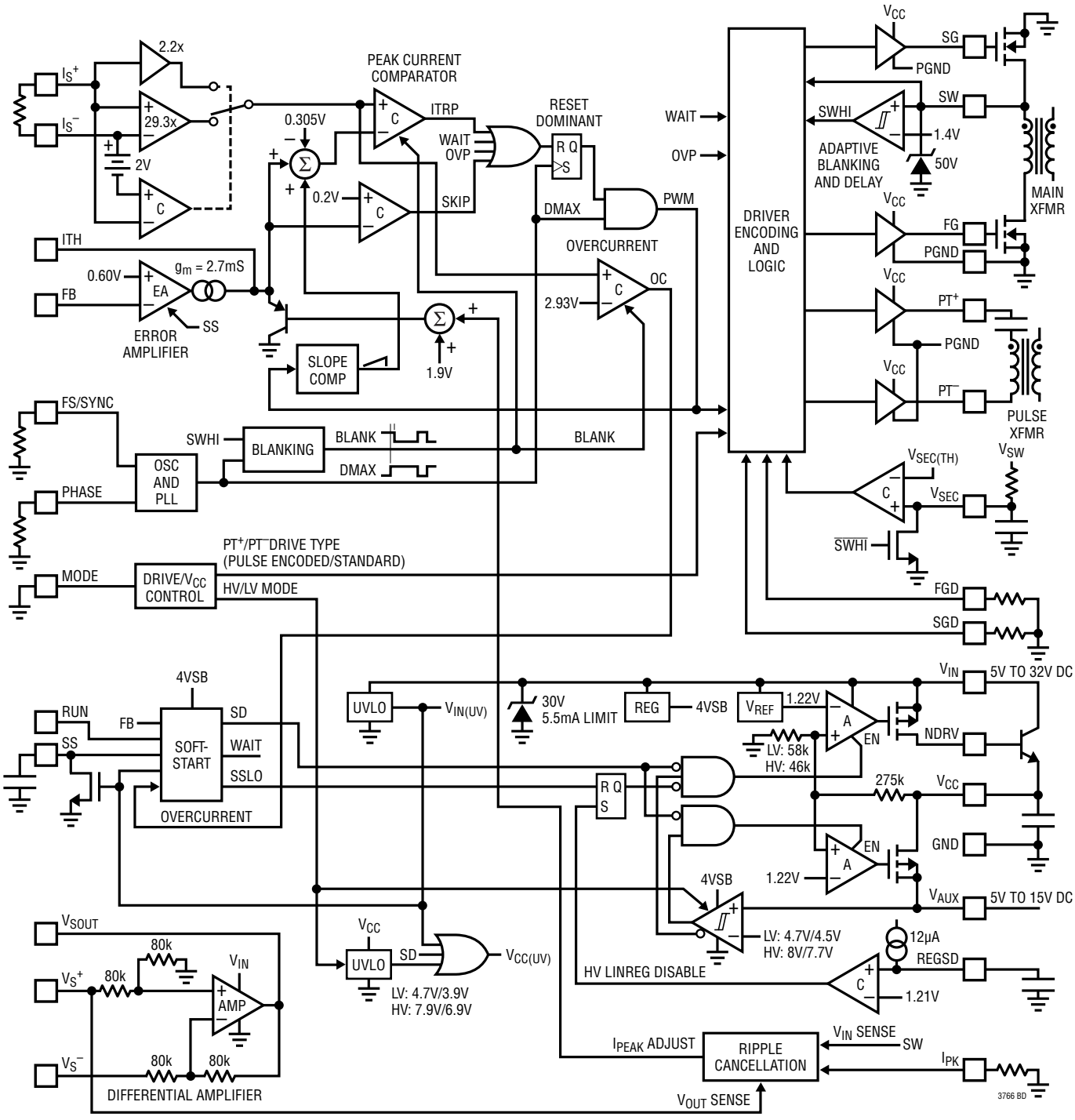
BLOCK DIAGRAM



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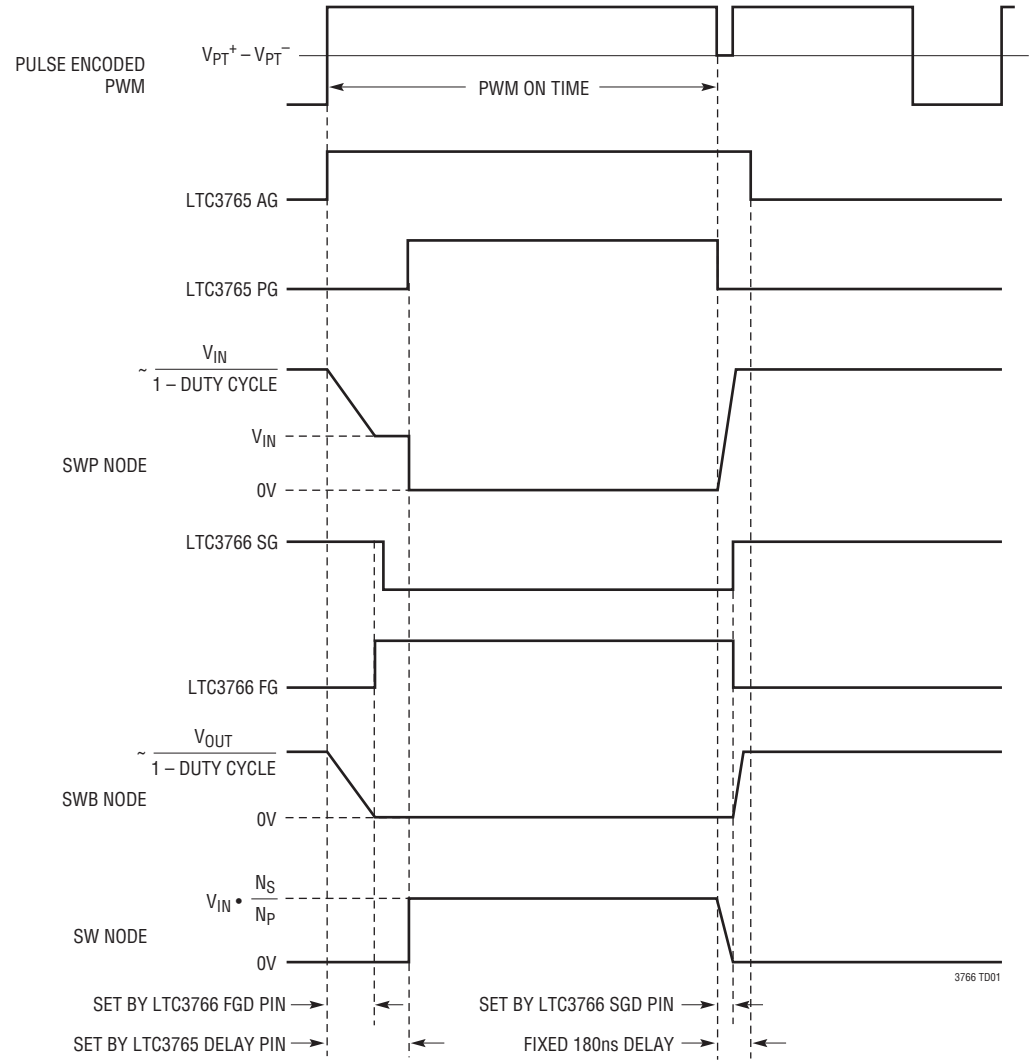
TIMING DIAGRAM



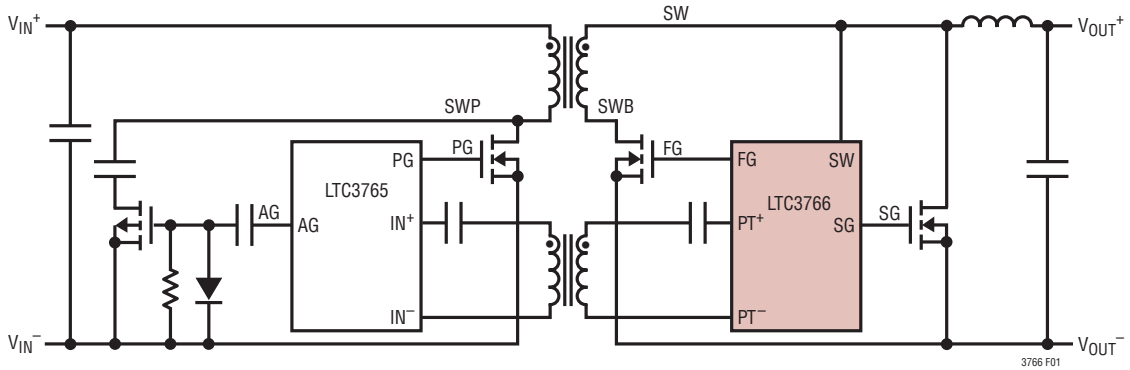


Figure 1. Reference Schematic for Timing Diagram

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OPERATION

The LTC3766 is a secondary-side PWM controller designed for use in a forward converter with active clamp reset and synchronous rectification. When used in conjunction with the LTC3765 active-clamp forward controller and gate driver, it forms a highly efficient and robust isolated power supply with a minimum number of external components. By making use of a secondary-side control architecture, the LTC3766 is able to provide exceptional transient response while directly monitoring the load to ensure that both output voltage and output current are precisely controlled. This architecture provides superior performance and greater simplicity, and is particularly well suited to high power battery charger applications.

Self-Starting Start-Up

In most applications, the LTC3766 will be used with the LTC3765 to create a self-starting forward converter with secondary-side control. Since there is initially no bias voltage available on the secondary side, the LTC3765 must manage the start-up in an open-loop fashion on the primary side. When power is first applied on the primary side, the LTC3765 begins an open-loop soft-start using its own internal oscillator. Power is supplied to the secondary by switching the main primary-side MOSFET with a gradually increasing duty cycle from 0% to 70%, as controlled by the rate of rise of the voltage on the SSFLT pin. On the secondary side, bias voltage can be generated directly from the main transformer using a peak charge circuit, or other technique as appropriate. When the LTC3766 has adequate voltage to satisfy its start-up requirements, it provides duty cycle information through the pulse transformer as shown in Figure 2. The LTC3765 detects this signal and transfers control of the gate drivers to the LTC3766, which continues the soft-start of the output voltage. Typically, this hand-off from primary to secondary occurs when the output voltage is less than one half of its final level. The LTC3765 then turns off the linear regulator and, through an on-chip rectifier, extracts bias power for the primary-side MOSFETs from this signal.

Linear Regulators

In general, the bias voltage generated on the secondary side is higher than the level desired for operation of the forward and synchronous MOSFETs. Consequently, the LTC3766 contains a high voltage linear regulator controller as well as a 15V V_{AUX} bypass regulator with an internal PMOS, either of which can be used to regulate the voltage on the V_{CC} pin. The linear regulator controller is used by tying the NDRV pin to the base or gate of an external N-type pass device. The LTC3766 V_{IN} pin provides bias to the linear regulator controller as well as to internal standby and monitoring circuitry. If adequate voltage is detected on the V_{AUX} pin, then the V_{AUX} bypass regulator will be activated and the high voltage linear regulator controller will be shut down to reduce power loss. Alternatively, if only the V_{AUX} regulator is needed, then the NDRV pin can be tied off to V_{CC}, while V_{IN} is tied to V_{AUX}. This flexible arrangement of two linear regulators allows for the convenient and efficient generation of V_{CC} bias voltage for a wide array of applications.

Using the MODE pin, the output voltage of both linear regulators can be set to either 7V or 8.5V, depending on the level needed to drive the gates of the forward and synchronous MOSFETs. Note that the undervoltage lockout (UVLO) set points as well as V_{AUX} switchover levels are adjusted along with the V_{CC} regulation levels. This ensures that the MOSFETs are only switched when there is adequate gate drive voltage.

Run Control and Soft-Start

The main on/off control for the LTC3766 is the RUN pin. This pin features precision thresholds with both internal and externally adjustable hysteresis. This pin can be used to monitor the secondary-side bias voltage or main output voltage, thereby controlling the point at which hand-off from primary to secondary side occurs. Alternatively, it can be driven directly with a control signal. In nonisolated applications when the LTC3766 is used standalone, this pin can be used as an undervoltage lockout by monitoring the main power supply input voltage. See Nonisolated Applications in the Applications Information section for details.

The LTC3766 will begin a soft-start sequence when the RUN pin is high, adequate voltage is present on both the V_{IN} and V_{CC} pins, and switching is detected on the SW pin. Note that the LTC3766 must see switching on the SW pin prior to initiating a soft-start sequence to ensure that the LTC3765 is ready for control hand-off. The soft-start sequence begins by first measuring the voltage on the FB pin and then rapidly pre-setting the soft-start capacitor voltage to a level that corresponds to the output voltage,

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V_{OUT}. This is done to provide a smooth ramp on the output voltage as control is transferred from primary to secondary, as well as to avoid any unnecessary start-up delay. Once the soft-start capacitor has been pre-set to the appropriate level, the LTC3766 then sends a brief sequence of pulses through the pulse transformer to establish a communication lock between the LTC3766 and the LTC3765. At this point, the LTC3766 assumes control of the primary-side MOSFETs, and the soft-start capacitor begins charging with a constant current of 5µA, continuing the soft-start of the main output voltage. Note that the soft-start voltage is used to limit the effective level of the reference into the error amplifier. This technique maintains closed-loop control of the output voltage during the secondary-side soft-start interval.

Gate Drive Encoding

Since the LTC3766 controller normally resides on the secondary side of an isolation barrier, communication to the primary-side gate driver must be done through a small pulse transformer. A common scheme for communicating gate drive (PWM) information makes use of short pulses and relies on receiver latches to "remember" whether power MOSFETs should be either on or off. However, this system is prone to get into the wrong state, and has difficulty distinguishing a loss of signal from a legitimate zero duty cycle signal. To alleviate these concerns, the LTC3766 uses a proprietary gate drive encoding scheme that reliably maintains constant contact across the isolation barrier without introducing any delay.

The LTC3766 encodes PWM information onto the PT^+ and PT^- outputs, which are in turn connected to a small pulse transformer through a DC-blocking capacitor. These outputs are driven in a complementary fashion, with a constant 79% duty cycle. This results in a stable volt-second balance, so that the signal amplitude transferred across the pulse transformer is constant. As shown in Figure 2, the beginning of the interval when (V_{PT}^+-V_{PT}^-) is positive approximately coincides with the turn-on of the main primary-side MOSFET. Likewise, the beginning of the interval when (V_{PT}^+-V_{PT}^-) is negative coincides with the maximum duty cycle (forced turn-off of main primary-side MOSFET). At the appropriate time during the positive interval, the end of the "on" time (PWM going low) is signaled by briefly applying a zero-volt differential across the pulse transformer. In the event that a zero duty-cycle signal needs to be sent, this is accomplished naturally by placing the zero-voltage differential at the beginning of the positive interval. In this manner, any duty cycle from 0% to the maximum of 79% can be sent across the pulse transformer without delay. Figure 2 illustrates the operation of this encoding scheme.

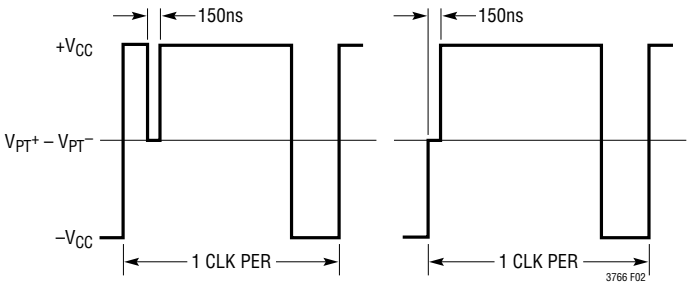

Figure 2: Gate Drive Encoding Scheme (MODE = GND or MODE = V_{CC})

On the primary side, the LTC3765 receives the signal from the pulse transformer through a DC restoring capacitor. After communication lock has been established between the two parts, the LTC3765 extracts clock and duty cycle information from the signal and uses it to control its gate driver outputs. Note that, except for a tiny pulse, this scheme is constantly applying a differential voltage across the pulse transformer. Therefore, the LTC3765 can almost instantly detect a loss of signal and shut off the power MOSFETs.

Forward Converter and Main Loop Operation

Once communication lock has been established between the LTC3766 and the LTC3765, the LTC3766 will have control over the switching of the primary-side MOSFETs. During normal operation, the main primary-side MOSFET (connected to PG on the LTC3765) is turned on somewhat after the forward MOSFET on the secondary side. This applies the input voltage across the transformer, causing the SW node on the secondary side to rise. Since the SW node voltage is greater than the output voltage, the inductor current ramps upward. When the current in the inductor has ramped up to the peak value as commanded by the voltage on the ITH pin, the current sense comparator trips, turning off the primary-side MOSFET. After a short delay,

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OPERATION

the forward MOSFET is turned off and the synchronous MOSFET is turned back on, causing the inductor current to ramp back downwards. At the next rising edge of the LTC3766 internal clock, the cycle repeats as the synchronous MOSFET is turned off and the forward and main primary-side MOSFETs are again turned on. The LTC3766 error amplifier senses the main output voltage, and adjusts the ITH voltage to obtain the peak inductor current needed to keep the output voltage at the desired regulation level.

In some applications, there can be considerable resistive voltage drops between the main output voltage and the load. To address this, the LTC3766 contains a precision differential amplifier, which can be used to remotely sense a load voltage as high as 15V.

Current Sensing, Slope Compensation and Blanking

The LTC3766 supports current sensing either with a current sense resistor or with an isolated current transformer. When using a current sense resistor, the I_S^+ and I_S^- pins operate differentially, and the maximum peak current threshold is approximately 75mV. Normally, the current sense resistor is placed in the source of the forward MOSFET to minimize power loss. If a current transformer is used to sense the primary-side switch current, then the I_S^- input should be tied to V_{CC} and the I_S^+ pin to the output of the current transformer. This causes the gain of the internal current sense amplifier to be reduced, so that the maximum peak current threshold is increased to approximately 1V.

As with any PWM controller that uses constant-frequency peak current control, slope compensation is needed to provide current-loop stability and improve noise margin. The LTC3766 has fixed internal slope compensation. The amount of slope has been chosen to be adequate for a wide range of applications. Normally, the use of slope compensation would have a negative impact on the accuracy of the current limit, but the LTC3766 uses a proprietary circuit to nullify the effect of slope compensation on the current limit performance.

Since the LTC3766 current loop is sensing switch current, leading edge blanking is needed to avoid a current comparator false trip due to the MOSFET turn-on current spike. The LTC3766 uses the voltage on the SW pin (tied to the drain of the synchronous MOSFET) to implement an adaptive leading-edge blanking of approximately 180ns. The blanking of the current comparator begins only after the voltage on SW has risen above 1.4V. This adaptive blanking is essential because of the potentially long delay from the time that PT+ rises to the time that the SW node rises, and current begins ramping up in the output inductor. This blanking also minimizes the need for external filtering.

Gate Driver Delay Adjustment

As in all forward converters, the main transformer core must be properly reset so as to maintain a balanced volt-second product and prevent saturation. This job is handled on the primary side by the LTC3765, which features an active clamp gate driver. The active clamp MOSFET works together with a capacitor to generate an optimal reset voltage for the main transformer. This optimal reset voltage minimizes voltage stress on the main primary-side MOSFET and maximizes the utilization of the power transformer core by reducing the magnetic flux density excursion.

In general, the active clamp MOSFET is switched in a complimentary fashion to the main primary-side MOSFET. Since the active clamp MOSFET is a PMOS, the active clamp gate driver (AG) and the main primary-side gate driver (PG) voltages are therefore “in-phase,” with a programmable overlap time set by the LTC3765 DELAY pin.

The delay time between the active clamp PMOS turn-off and the primary switch NMOS turn-on is critical for optimizing efficiency. When the active clamp is on, the drain of the primary NMOS, or primary switch node (SWP), is driven to a voltage of approximately $V_{IN}/(1–D)$ by the main transformer. When the active clamp turns off, the current in the magnetizing inductance of the transformer ramps this voltage linearly down to V_{IN}. Power loss is minimized by turning on the primary switch when the SWP voltage is at a minimum. A resistor from the LTC3765 DELAY pin to ground sets a fixed time for the PG turn-on delay.

The delay time between the primary switch turn-off and the active clamp turn-on is substantially less critical. When the primary switch turns off, the main transformer leakage inductance is biased with the peak current of the inductor reflected through the transformer. This current drives the voltage across the active clamp PMOS quickly to 0V. Turning on the PMOS after this transition results in

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minimal switching power loss. The LTC3765 active clamp turn on delay is internally fixed to 180ns, which normally achieves zero voltage switching on the active clamp PMOS.

On the secondary side, the turn-on delay of the forward gate (FG) and synchronous gate (SG) MOSFETs are adjusted by the FGD and SGD pins respectively. These delays are set using resistors to GND so as to minimize the dead time (when the load current is being carried by MOSFET body diodes) while avoiding shoot-through with the primary-side MOSFETs. A shoot-through condition exists if either the PG and SG gates, or the AG and FG gates are high at the same time. Note that the SG MOSFET turn-on delay has a minimum limit that is established by the falling edge of the SW node. The SG pin will normally not go high until SW has fallen below 0.5V. After a 180ns timeout, however, the SG pin will go high regardless of the SW voltage. Refer to Delay Resistor Selection in the Applications Information section for more detailed information. In standalone mode (100k or 50k resistor on MODE), the dead time between PG and SG is set adaptively to prevent shoot-through.

Frequency Setting and Synchronization

The LTC3766 uses a single pin to set the operating frequency or to synchronize the internal oscillator to a reference clock using and on-chip phase-locked loop (PLL). The FS/SYNC pin sources a 20µA current, and it may be tied to V_{CC} for fixed 275kHz operation or have a single resistor to GND to set the switching frequency to $f_{SW} = 4R_{FS}$. If a clock signal (>2V) is detected at the FS pin, the LTC3766 will automatically synchronize to the falling edge of this signal using an internal PLL.

Current Limit and Inductor Ripple Cancellation

Since the LTC3766 utilizes peak current control, the peak inductor current is limited when the load current demand increases above the current limit set point. The peak current limit is established by an internal clamp on the maximum level of the ITH voltage. The average current, however, will be less than the peak current by an amount equal to one-half of the inductor ripple current. During current limit, this ripple current will change significantly with variations in V_{IN}, V_{OUT} and switching frequency. Without inductor ripple cancellation, this variation in ripple current would also result in an average output current that changes significantly, even though the peak current is held at a constant value.

In order to keep the average current approximately constant during current limit, the LTC3766 cancels the effect of the ripple current by adjusting the value of the peak current limit (or ITH clamp level) in proportion to the amount of inductor ripple current. This is achieved by generating an internal ramp that mimics the inductor current ramp, and then adding the amplitude of this internal ramp to the ITH clamp voltage on a cycle-by cycle basis. During the on time, the slope of the inductor current is given by:

$$\frac{dI_L}{dt} = \frac{V_{SW} - V_S^+}{L}$$

The LTC3766 establishes a voltage on the I_{PK} pin of $(V_{SW} - V_S^+)/15$, which is one-fifteenth of the voltage across the output inductor during the on-time when SW is high. By choosing a resistor R_{IPK} that is proportional to the value of the output inductor ($R_{IPK} = KL$), the current flowing in R_{IPK} becomes proportional to the slope of the inductor current:

$$I_{RIPK} = \frac{V_{SW} - V_S^+}{15R_{IPK}} = \frac{V_{SW} - V_S^+}{15KL}$$

During the time when SW is high, the LTC3766 uses the R_{IPK} current to create an internal ramp by charging an on-chip capacitor C_{RIP}. The slope of this internal ramp voltage is given by:

$$\frac{dV_{RAMP}}{dt} = \frac{I_{RIPK}}{C_{RIP}} = \frac{V_{SW} - V_S^+}{15KLC_{RIP}}$$

The amplitude of this internal ramp is then added to the ITH clamp level dynamically. By choosing the appropriate value of R_{IPK}, therefore, the average current during current limit will be essentially independent of changes in ripple current.

As is the case with all DC/DC converters that maintain constant frequency operation, a cycle by cycle current limit is only effective at duty cycles where the on time is greater than the minimum controllable on-time. Under short-circuit conditions, for example, the LTC3766 limits

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the current using a separate overcurrent comparator. When this overcurrent comparator is tripped, the LTC3766 generates a fault followed by a soft-start retry. This hiccup mode overcurrent protection is highly effective at minimizing power losses under short-circuit conditions.

Direct Flux Limit

In active clamp forward converters, it is essential to establish an accurate limit to the transformer flux density in order to avoid core saturation during load transients or when starting up into a pre-biased output. Although the active clamp technique provides a suitable reset voltage during steady-state operation, the sudden increase in duty cycle caused in response to a load step can cause the transformer flux to accumulate or "walk," potentially leading to saturation. This occurs because the reset voltage on the active clamp capacitor cannot keep up with the rapidly changing duty cycle. This effect is most pronounced at low input voltage, where the voltage loop demands a greater increase in duty cycle due to the lower voltage available to ramp up the current in the output inductor.

Traditionally, transformer core saturation has been avoided either by limiting the maximum duty cycle of the converter or by slowing down the loop to limit the rate at which the duty cycle changes. Limiting the maximum duty cycle does help the converter avoid saturation for a load step at low input voltage, since the duty cycle maximum is clamped; however, transformer saturation can also easily occur at higher input voltage where the maximum duty cycle clamp is ineffective. Limiting the rate of duty cycle change such that the active clamp capacitor can sufficiently track the duty cycle change also helps to prevent saturation in many situations, but results in a very poor transient response. Neither of these traditional techniques is guaranteed to prevent the transformer from saturating in all situations. For example, saturation can easily occur using these traditional techniques when starting up into a pre-biased output, where the duty cycle can quickly change from 0% to 75%. Moreover, neither of these traditional techniques is able to prevent saturation in the negative direction, which can result from sudden decreases in duty cycle.

The LTC3765 and LTC3766 implement a new unique system for monitoring and directly limiting the flux accumulation in the transformer core. During a reset cycle, when the active clamp PMOS is on, the magnetizing current is directly measured and limited through a sense resistor in series with the PMOS source. This prevents saturation in the negative direction. When the PMOS turns off and the main NMOS switch turns on, the LTC3765 generates an accurate internal estimate of the magnetizing current based on the sensed input voltage on the LTC3765 RUN pin and transformer core parameters customized to the particular core by a resistor from the LTC3765 R_{CORE} pin to ground. The magnetizing current is then limited during the on-time by this accurate internal approximation. Unlike previous methods, the Direct Flux Limit directly measures and monitors flux accumulation and guarantees that the transformer will not saturate in either direction, even when starting into a pre-biased output. This technique also provides the best possible transient response, as it will temporarily allow very high duty cycles, only limiting the duty cycle when absolutely necessary. Moreover, this technique prevents overcurrent damage to the active clamp PMOS, which is a potentially significant weakness in many active clamp forward converter designs.

Additional Protection Features

The LTC3766 contains a wide array of protection features, which protect the DC/DC converter in the event that abnormal conditions persist. In general, protections features are either classified as a fault or a limit. When a fault is detected, all switching stops and the LTC3766 initiates a soft-start retry. Faults of this nature include overcurrent, overtemperature, differential amplifier miswire and communication-lock fault.

An overcurrent fault occurs if the peak current exceeds approximately 133% of its normal value during current limit. Note that when inductor ripple cancellation is used, the value of the peak current during current limit will vary with inductor current ripple. The overtemperature fault is set at 165°C, with 20°C of hysteresis. This is helpful for limiting the temperature of the DC/DC converter in the event of some external device failure or other abnormal condition. The differential amplifier wiring fault is generated if the inputs on the differential amplifier are reversed, or if there is not enough voltage on the V_{IN} pin to support the voltage needed on V_{SOUT}. This is important to avoid an overvoltage condition on the output.

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Finally, since it is essential that the LTC3766 be in constant communication with the LTC3765, a loss of communication lock will also generate a fault. A lock condition is detected by monitoring the SW node voltage, and ensuring that it is both rising and falling as it should in response to the PWM signal being sent to the primary side. If the SW node voltage is not rising and falling in an appropriate manner, than a lock fault is generated. In particular, if the SW node does not rise within approximately 800ns of PT^+ rising, then a fault is immediately generated. Likewise, if the SW node does not fall within approximately 180ns of PT^+ falling, then a fault will also be generated, but only if this condition persists and the LTC3766 is operating at maximum duty cycle.

In addition to the four protection features that generate faults, there are also four protection features that establish a clamp or limit, without generating a fault. First, the LTC3766 contains a precision volt-second clamp. This feature is not needed when the LTC3766 is used in conjunction with the LTC3765, which incorporates the Direct Flux Limit feature. If the LTC3766 is used standalone, however, the volt-second limit can be used by placing a resistor from the SW node to the V_{SEC} pin and a capacitor from V_{SEC} to GND. When the SW node is low, the capacitor is discharged by an on-chip NMOS. When the SW node is high, the capacitor on V_{SEC} is charged. If the capacitor voltage exceeds an internally generated threshold, then the main primary switch will be turned off, thereby limiting the volt-second product applied to the main transformer. To compensate for the exponential nature of the RC charging circuit, the LTC3766 adjusts the threshold of the volt-second comparator according to:

$$V_{SEC(TH)} = 0.6 - \frac{0.16}{V_{SW(HI)}}$$

where $V_{SW(HI)}$ is the voltage on the SW pin during the on-time of the primary switch. This keeps the volt-second limit essentially constant for SW node voltages in the range of 2V to 40V.

Second, in the event that the main output voltage exceeds its regulation target by more than 17%, the LTC3766 will detect an overvoltage condition. If this happens, the LTC3766 will immediately turn off the main primary MOSFET and turn on the synchronous MOSFET. This has the effect of pulling down the output voltage to protect the load from potential damage. Overvoltage protection is not latched, and normal operation is restored when the output voltage has been reduced to within 15% of its regulation level.

Third, the LTC3766 contains an adjustable synchronous MOSFET reverse overcurrent. This is accomplished by monitoring the SW voltage when the synchronous MOSFET is on (SG pin is high). If the voltage on SW exceeds a pre-determined threshold, then the synchronous MOSFET will be turned off, protecting it from potentially damaging current levels. This SW threshold for reverse overcurrent detection can be reduced by placing a resistor in series with the SW pin, which sources a current when the SG pin is high. Note that the SG reverse overcurrent threshold and the SW pin source current are adjusted based on the state of the MODE pin. This is done to accommodate the use of either high voltage or low voltage MOSFETs, which normally have significantly different on resistances. In an overvoltage condition, the SG reverse overcurrent will override the overvoltage protection and force SG low, essentially regulating the reverse SG MOSFET current at a high level while the overvoltage condition persists. However, the SG reverse overcurrent is only active after the LTC3766 has achieved communication lock.

Finally, the REGSD pin can be used to limit the amount of time that the high voltage linear regulator controller is active. This is particularly useful when the LTC3766 is used standalone in a nonisolated forward converter. In this application, the pass device of the linear regulator controller may be dissipating considerable power. When the linear regulator controller is active, the REGSD pin sources a 13µA current. If a capacitor from REGSD to GND charges to a voltage greater than 1.21V, then linear regulator controller is disabled.

Gate Driver Mode Control

In addition to being used in conjunction with the LTC3765, the LTC3766 can also be used standalone in a nonisolated forward converter application. In this case, the MODE pin can be used to disable gate drive encoding by tying MODE to GND through either a 100k (for V_{CC} = 7V operation) or 50k (for V_{CC} = 8.5V operation) resistor. This causes a normal PWM signal to appear on PT^+ and a reference clock to appear on PT^-.

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APPLICATIONS INFORMATION

Secondary-Side Bias and Start-Up

In most applications, the LTC3766 will receive its bias voltage from a supply that is generated on the secondary side. The manner in which the secondary bias is generated depends upon the output voltage as well as the variation in the input voltage of the DC/DC converter. In all applications, however, the secondary bias must always come up before the output reaches the regulation level. This is essential to avoid an overvoltage condition on the output, since the initial start-up is performed from the primary side in an open-loop fashion. See Generating the Secondary-Side Bias for more information.

Note that the LTC3766 will not begin a soft-start sequence and initiate switching until the RUN pin is high, adequate voltage is present on both the V_{IN} and V_{CC} pins, and switching is detected on the SW pin. The LTC3766 looks for switching on the SW pin to ensure that the LTC3765 is active and ready for control hand-off. For switching to be detected, the SW node waveform must have at least eight consecutive pulses in the range of 50kHz to 700kHz. The SW node waveform must also have a peak that is greater than 1.4V and a valley that is less than 0.5V. In standalone mode, the LTC3766 begins the soft-start sequence without waiting for a switching waveform to be detected on the SW pin.

Linear Regulator Operation

The LTC3766 contains two linear regulators that are used to regulate the available bias voltage down to a level suitable for driving MOSFETs. If the bias supply voltage is greater than 15V, then the high voltage linear regulator controller may be used. This makes use of an external N-type pass device. Place a capacitor of 0.22µF or greater on V_{IN} and 1µF or greater on V_{CC}. If the bias supply connected to the V_{IN} pin has a relatively high output impedance, it may be necessary to use a larger capacitor on V_{IN} to prevent the V_{IN} pin voltage from dropping when the V_{CC} capacitor is being charged. The V_{CC} charge rate during linear regulator start-up is set by the LTC3766 to approximately 0.5V/µs, which will create at charging current of $(0.5 \bullet 10^6)\ C_{VCC}$. Care should be taken to ensure that this charging current does not exceed the SOA of the N-type pass device, particularly when operating at higher V_{IN} voltages. The V_{CC} regulation level can be set to either 7V or 8.5V as desired using the MODE pin. See the section on V_{CC} and Drive Mode Selection for details.

The LTC3766 also contains a 15V internal bypass LDO. If the voltage on the V_{AUX} pin exceeds the V_{AUX} switchover threshold, then the high voltage linear regulator is disabled, and an internal PMOS-pass LDO uses the V_{AUX} voltage to supply power to V_{CC}. This allows the high voltage linear regulator to be used for initial start-up and the higher efficiency bypass LDO to be used during normal operation. Figure 3 illustrates such a configuration that uses both linear regulators.

If the voltage on the V_{AUX} pin is below the switchover threshold, then the V_{AUX} pin is internally loaded with a resistance of approximately 920Ω. This internal load is removed after the V_{AUX} regulator is enabled, and is used to ensure that the V_{AUX} supply is reasonably stiff before the bypass regulator is activated.

In some cases, it is desirable to use the high voltage linear regulator only briefly during start-up, so as to limit the temperature rise in the external pass device. To accomplish this, place a capacitor on the REGSD pin to ground (see Figure 3) such that:

$$C_{RSD} = \frac{t_{HVREG}(13\mu A)}{1.21V}$$

where t_{HVREG} is the time that the high voltage regulator will operate. When the high voltage regulator is operating, a 13µA current is sourced from the REGSD pin, and when it is shut down (e.g., the bypass regulator is active), a 3µA current is sinked into the REGSD pin. If the REGSD voltage exceeds 1.21V, the high voltage regulator

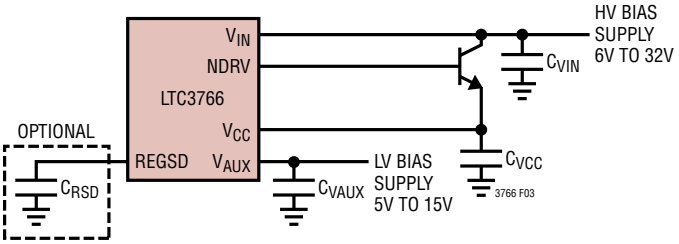

Figure 3. Typical Linear Regulator Connections

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is disabled. Choose a time t_{HVREG} that is greater than the normal start-up time. After start-up, if the voltage on the V_{AUX} pin drops, the high-voltage linear regulator will be re-energized, but only for a limited time.

When used with a bias supply that is between 5V and 10V, the V_{CC} pin can be directly connected to the bias supply as shown in Figure 4a. Note that the V_{IN} and NDRV pins must also be connected to the bias supply for proper operation of internal circuitry. When a bias supply between 6V and 15V is available, the V_{AUX} bypass linear regulator can be used standalone as shown in Figure 4b. In this case, proper start-up is assured by connecting the NDRV pin to V_{CC}. Since there is no external pass device on NDRV, however, the effective UVLO levels will be dictated by the V_{AUX} switchover thresholds instead of the V_{CC} UVLO thresholds. Rather than relying on the V_{AUX} thresholds, the start-up and shutdown levels are normally set by using the RUN pin to monitor the bias supply voltage as shown in Figure 4b. See the RUN Pin Operation section for details.

For applications where the available bias supply is greater than 30V, the LTC3766 also contains a current-limited 30V clamp on the V_{IN} pin. This clamp can sink up to 3.5mA

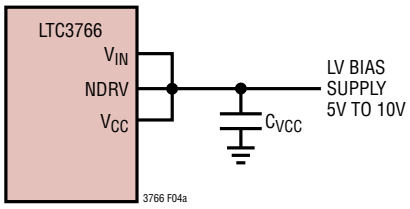

Figure 4a. No Linear Regulator Used

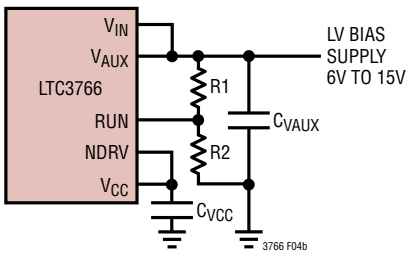

Figure 4b. V_{AUX} Regulator Used Standalone

to allow the V_{IN} pin to be used as a shunt regulator. This is especially useful in nonisolated applications where the LTC3766 is used standalone. See the Nonisolated Applications section for more information.

RUN Pin Operation

Normal operation is enabled when the voltage on RUN rises above its 1.22V threshold. As shown in Figure 5, the RUN pin can be used with an external resistor divider to enable the LTC3766 operation based on a sensed voltage V_X. In self-starting applications, V_X is normally either the converter output voltage (V_{OUT}) or a bias voltage. In

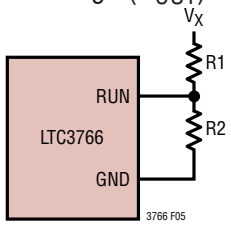

Figure 5. Using the RUN Pin to Determine Start-Up

nonisolated applications, V_X is normally the converter input voltage (V_{IN}). See Nonisolated Applications for more information on the use of the RUN pin in nonisolated applications.

A 3µA current is pulled into the RUN pin when it is below its threshold that, when combined with the value chosen for R1, increases the hysteresis beyond the internal amount of 4%. When used in this manner, the values for R1 and R2 can be calculated from the desired rising and falling V_X thresholds by the following equations:

$$R1 = \frac{V_{X(RISING)} - 1.043 \bullet V_{X(FALLING)}}{3\mu A}$$

$$R2 = \frac{1.17 \bullet R1}{V_{X(FALLING)} - 1.17}$$

In self-starting applications where the LTC3765 performs an open-loop soft-start, the voltage V_X can be tied to V_{OUT} of the converter ($V_X = V_{OUT}$) to inhibit the LTC3766 start-up until the output voltage is above a given level. This

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sets the exact output voltage at which soft-start control is handed off from primary to secondary. This hand-off output voltage should be set high enough so as to avoid pulse-skipping operation when the LTC3766 initially takes control. If excessive pulse skipping occurs in applications that use a peak charge circuit to generate bias voltage, this can cause the bias supply to fall, preventing proper start-up. To preclude this possibility, use the RUN pin to inhibit the LTC3766 start-up until the output voltage is at least:

$$V_{OUT(ON)} > 300ns \frac{N_S f_{SW} V_{IN(MAX)}}{N_P}$$

Note that in self-starting applications, direct RUN/STOP control should be handled only on the primary side using the LTC3765. If the LTC3765 gets disabled, the LTC3766 will sense that the primary side is no longer switching and automatically shut down. To avoid a possible output overvoltage, do not manually disable the LTC3766 unless the LTC3765 is also manually disabled.

If the RUN pin function is not needed, it can be tied directly to the V_{IN} pin.

Setting the Switching Frequency and Synchronization

The switching frequency of the LTC3766 is set using the FS/SYNC pin. This pin sources a 20µA current, and a resistor to ground on this pin sets the switching frequency to a value equal to:

$$f_{SW} = 4R_{FS}$$

Alternatively, the FS/SYNC pin can be tied to V_{CC}, which sets the switching frequency to a fixed value of 275kHz. In general, a higher switching frequency will result in a smaller size for inductors and transformers, but at the cost of reduced efficiency. Although the LTC3766 can operate from 75kHz to 500kHz, the best balance between efficiency and size for a forward converter is found when operating between 150kHz and 350kHz.

If a clock signal (>2V) is detected at the FS pin, the LTC3766 will automatically synchronize to the falling edge of this signal. Table 1 summarizes the operation of the FS/SYNC pin.

Table 1

FS/SYNC PIN	SWITCHING FREQUENCY
V_{CC}	275kHz
R_{FS} to GND	$f_{SW} = 4R_{FS}$
Reference Clock	$f_{SW} = f_{REF}$ (100kHz to 500kHz)

In PolyPhase applications, synchronization can be achieved by tying the PT⁻ pin of the master to the FS/SYNC pin of each slave. The relative phase delay of each slave is set using the PHASE pin. Any one of five preset values can be selected as shown in Table 2. Note that the phase delay is relative to the falling edge of the incoming reference clock on the FS/SYNC pin, since the falling edge of PT⁻ corresponds to the beginning of the PWM cycle.

Table 2

PHASE PIN	PHASE DELAY	APPLICATION
GND	180°	2-Phase and 4-Phase
25k to GND	240°	3-Phase
50k to GND	120°	3-Phase
100k to GND	90°	4-Phase
100k to V_{CC}	270°	4-Phase

In general, the external synchronizing clock should be present before the LTC3766 is enabled, so that the switching frequency has stabilized before the gate drivers begin switching. In some applications, however, it may be necessary to synchronize the LTC3766 after it has begun switching. In this case, the circuit in Figure 6 can be used.

Using the circuit Figure 6, the LTC3766 will run at 275kHz until the 3.3V – 5V amplitude synchronization signal V_{SYNC} begins toggling. This circuit creates a 100ns low-pulse at the FS/SYNC pin, which ensures a smooth transition into synchronization. As shown in Figure 6, the V_{CC} pin can

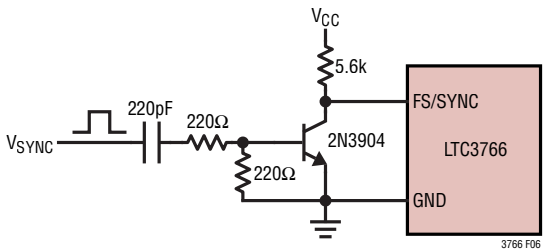

Figure 6. Synchronization After LTC3766 Start-Up

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normally be used to provide the pull-up voltage, which must be between 5V and 12V. In addition, the rise time of the voltage on the FS/SYNC pin must be less than 200ns. Consequently, parasitic capacitance on the FS/SYNC pin must be minimized.

Once the LTC3766 has been synchronized, do not remove the external synchronizing clock unless the LTC3766 is also shut down. Removal of the external clock after synchronization will result in operation at low frequencies for a period of time, which can lead to very high currents in external power components.

Setting the Output Voltage

The LTC3766 output voltage is set by an external feedback resistor divider placed across the output as shown in Figure 7. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

Be careful to keep these divider resistors very close to the FB pin to minimize the trace length and noise pick-up on the sensitive FB signal. Using a low resistance (<2k) for the output voltage divider also minimizes noise on the FB pin. If the remote sense amplifier is used, then the divider should be placed between the V_{SOUT} pin and GND. See the Remote Sensing section for details.

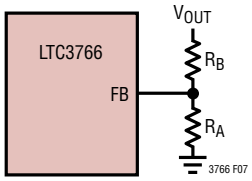

Figure 7. Setting the Output Voltage

Selecting the Main Transformer

The job of the transformer in a forward converter is to step the voltage either up or down while providing isolation between the primary and secondary grounds. Ideally, this transformer would not store any energy (it would have infinite magnetizing inductance). Note that this objective is very different from that of the transformer used in a flyback converter. The transformer used in a flyback converter is really a coupled inductor, the purpose of which is to store energy during the primary-side on time and then deliver it to the secondary during the off-time. In a forward converter, by contrast, the power is transferred during the primary-side on-time, and the off-time is used to recover the small amount of energy that was inadvertently stored in the core of the transformer.

For nearly all applications, an off-the-shelf transformer can be selected. Transformers using planar winding technology are widely available and are a good choice for minimizing leakage inductance as well as component height. There are two basic items to consider in selecting an appropriate family of off-the-shelf transformers: 1) the isolation requirements and 2) the power level requirements. If the application circuit has specific isolation requirements, choose a family of transformers whose isolation level satisfies that requirement. In addition to an isolation voltage rating, the application may require a transformer with certification from a particular agency, or it may require a specific type of isolation (e.g., basic or functional). In terms of power level, choose a family of transformers whose rated power level exceeds that of the required amount of output power. Be careful to allow for room to "grow," as the power requirements of many electronic systems tend to increase throughout development.

Once a family of transformers has been selected, the next step is to choose a suitable transformer from within that family. This mainly consists of choosing the correct number of primary and secondary turns (N_P and N_S). The value of N_S can be calculated from:

$$N_S = \frac{10^8 V_{OUT}}{f_{SW} A_C B_M}$$

where A_C is the cross-sectional area of the core in cm^2 (as normally given in the transformer data sheet) and B_M is the maximum AC flux density desired. For the Pulse PA08xx series power transformers used in the Typical Applications

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section, $A_C = 0.59cm^2$. For the Pulse PA09xx series power transformers, $A_C = 0.81cm^2$. For the Champs-Tech G45 and PQ26 power transformers, $A_C = 0.55cm^2$ and $A_C = 1.21cm^2$ respectively. Most high frequency transformers use a ferrite core material. Consequently, selecting a maximum AC flux density of 2000 gauss is normally a good starting point, provided that the switching frequency is between 150kHz and 350kHz. This value of B_M leaves headroom during transients and avoids excessive core losses. Note that the choice of B_M together with switching frequency will determine the amount of core loss for a given transformer. Consult the transformer data sheet to evaluate the resulting core loss and temperature rise. In some cases, it may be necessary to increase N_S somewhat in order to reduce B_M and the associated temperature rise. In all cases, be sure to stay well below the saturation flux density of the transformer core.

Once the value of has N_S been selected, the required transformer turns ratio can be calculated from

$$\frac{N_P}{N_S} = \frac{D_{MAX} V_{IN(MIN)}}{V_{OUT}}$$

where $V_{IN(MIN)}$ is the minimum input voltage and D_{MAX} is the maximum duty cycle. Although the LTC3766 has a maximum duty cycle of 79% (D_{MAX} = 0.79), normally a lower value of D_{MAX} is chosen in the above equation so that there is duty cycle headroom to accommodate load transients when operating at minimum input voltage. A value for D_{MAX} of 0.65 to 0.70 is appropriate for most applications.

Having selected a particular transformer, calculate the copper losses associated with the transformer winding. These losses are highest when operating at maximum duty cycle and full load. However, it is better to evaluate copper losses at the nominal operating point of 50% duty cycle, where the losses are approximately:

$$P_{CU} = \frac{(I_{MAX})^2}{2}\left(R_{SEC} + \left(\frac{N_S}{N_P}\right)^2 R_{PRI}\right)$$

where R_{PRI} and R_{SEC} are the primary and secondary winding resistances respectively, and I_{MAX} is the maximum output current. An optimal transformer design has a reasonable balance between copper and core losses. If they are significantly different, then adjust the number of secondary turns (and recalculate the needed turns ratio) to achieve such a balance.

Inductor Value Calculation

The selection of an output inductor is essentially the same as for a buck converter. For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} L}\left(1 - \frac{V_{OUT}}{V_{IN}} \bullet \frac{N_P}{N_S}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. Note that a lower inductance can improve transient response and help to reduce the flux swing seen by the main transformer. A reasonable starting point for setting the ripple current is $\Delta I_L = 0.4(I_{OUT(MAX)})$ for nominal V_{IN}. The maximum ΔI_L occurs at the maximum input voltage.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of the more expensive ferrite cores. Actual core loss is essentially independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

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Active Clamp Capacitor

The active clamp capacitor, C_{CL}, stores the average reset voltage of the transformer over many cycles. The voltage on the clamp capacitor is generated by the transformer core reset current, and will intrinsically adjust to the optimal reset voltage regardless of other parameters. The voltage across the capacitor at full load is approximately given by:

$$V_{CL} = \frac{V_{IN}^2}{V_{IN} - 1.15\left(V_{OUT} \bullet \frac{N_P}{N_S}\right)}$$

N_P/N_S is the main transformer turns ratio. The factor of 1.15 accounts for typical losses and delays. When PG and AG on the LTC3765 are low, the bottom side of the clamp capacitor is grounded, placing the reset voltage, V_{CL}, on the SWP node. When PG and AG are high, the top side of the capacitor is grounded, and the voltage on the bottom side of the capacitor is $-V_{CL}$. Therefore the voltage seen on the capacitor is also the voltage seen at the drains of the PG and AG MOSFETs.

As shown in Figure 8, the V_{CL} voltage has a minimum when the converter is operating at 50%. For a given range on V_{IN}, therefore, the maximum clamp voltage ($V_{CL(MAX)}$) will occur either at the minimum or maximum V_{IN}, depending on which input voltage causes the converter to operate furthest from 50% duty cycle. The maximum V_{CL} voltage can be determined by substituting the maximum and minimum values of V_{IN} into this equation and selecting the larger of the two. In order to leave room for overshoot, choose a capacitor whose voltage rating is greater than this maximum V_{CL} voltage by 50% or more. Typically, a good quality (X7R) ceramic capacitor is a good choice for C_{CL}. Also, be sure to account for the voltage coefficient of the capacitor. Many ceramic capacitors will lose as much as 50% of their value at their rated voltage.

The value of the clamp capacitor should be high enough to minimize the capacitor ripple voltage, thereby reducing the voltage stress seen by the MOSFETs. However, a larger clamp capacitor will ultimately result a slower transient response to avoid transformer saturation during load transients. While Direct Flux Limit will automatically limit the PWM on-time only as needed to prevent saturation, a larger clamp capacitor will require a longer time to charge or discharge in response to a load transient. Consequently, the value of the clamp capacitor represents a compromise between transient response and MOSFET voltage stress. A reasonable value for the clamp capacitor can be calculated using the following:

$$C_{CL} = \frac{1}{2L_M} \bullet \left(\frac{4}{2\pi f_{SW}}\right)^2$$

An additional design constraint on C_{CL} occurs because of the resonance between the magnetizing inductance L_M of the main transformer and the clamp capacitor C_{CL}. If the Q of this resonance is too high, it will result in increased voltage stress on the primary-side MOSFET during load

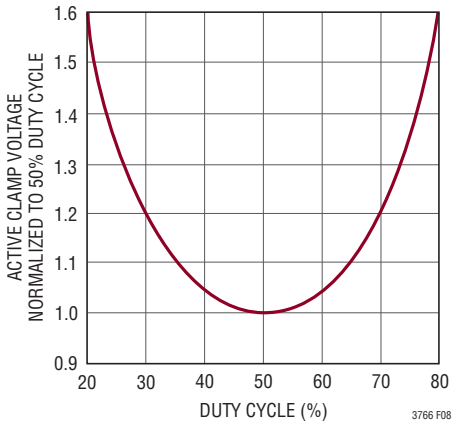

Figure 8. V_{CL} Voltage vs Duty Cycle

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transients. Also, a high Q resonance between L_M and C_{CL} complicates the compensation of the voltage loop, and can cause oscillations under certain conditions. **To avoid the problems associated with this resonance, always use an RC snubber in parallel with the clamp capacitor as shown in Figure 9.** The values for this RC snubber can then be calculated using:

$$R_{CS} = \frac{1}{1-\left(\frac{V_O}{V_{IN(MIN)}} \bullet \frac{N_P}{N_S}\right)} \sqrt{\frac{L_M}{C_{CL}}}$$

and

$$C_{CS} = 6C_{CL}$$

Figure 9 shows a typical arrangement of the active clamp capacitor with an RC snubber. Be careful to account for the effect of voltage coefficient for both C_{CS} and C_{CL} to ensure that the above relationship between C_{CS} and C_{CL} is maintained.

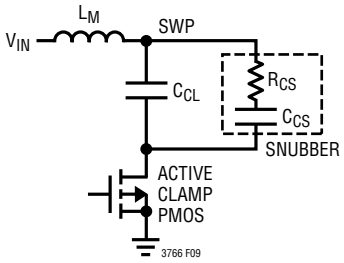

Figure 9. Active Clamp Capacitor and Snubber

Direct Flux Limit

In active clamp forward converters, it is essential to establish an accurate limit to the transformer flux density in order to avoid core saturation during load transients or when starting up into a pre-biased output. The LTC3765 and LTC3766 implement a new unique system for monitoring and directly limiting the flux accumulation in the transformer core. Unlike previous methods, the Direct Flux Limit directly measures and monitors flux accumulation and guarantees that the transformer will not saturate in either direction, even when starting into a pre-biased output. This technique also provides the best possible transient response, as it will temporarily allow very high duty cycles, only limiting the duty cycle when absolutely necessary. Moreover, this technique prevents overcurrent damage to the active clamp PMOS, which is a potentially significant weakness in many active clamp forward converter designs.

Since the Direct Flux Limit functionality is implemented in the LTC3765 on the primary side, there is nothing to adjust on the secondary side. See the LTC3765 data sheet for details on using this feature. Note that if the LTC3765 terminates the PG MOSFET on-time prematurely to limit flux accumulation, the LTC3766 will sense a premature falling on the SW node. In response, the LTC3766 will automatically terminate the FG on-time, thereby allowing the transformer core to reset. A premature falling on the SW node will also occur whenever the LTC3765 has shut down for any reason. Consequently, if the LTC3766 detects 19 consecutive premature SW node falling edges on the SW pin, it will generate a lock fault and shut down.

Primary-Side Power MOSFET Selection

On the primary side, the peak-to-peak drive levels for both the N-channel main switch and the P-channel active clamp switch are determined by the voltage on the V_{CC} pin of the LTC3765. This voltage is normally provided through the pulse transformer, and is typically set in the range of 8.5V to 12V. Note that even in applications where a logic-level MOSFET may be used on the primary side, the V_{CC} voltage on the LTC3765 must still be in this range for proper operation.

Selection of the N-channel MOSFET involves careful consideration of the requirements for breakdown voltage (BV_{DSS}) and maximum drain current, while balancing the losses associated with the on-resistance and parasitic capacitances. In an active clamp topology, the maximum drain voltage seen by this MOSFET is approximately:

$$V_{DS(PG)} = 1.2 \bullet V_{CL(MAX)}$$

where $V_{CL(MAX)}$ is the maximum active clamp voltage given above in the Active Clamp Capacitor section. The factor

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of 1.2 has been added to allow margin for ringing and ripple on the clamp capacitor. It is important to select the lowest possible voltage rating for this MOSFET in order to maximize efficiency. Note that the RC snubber on the active clamp capacitor (see Figure 10) reduces the peak voltage stress on the primary-side MOSFET without adding to operating losses. Also, the leakage inductance of the main transformer at full load can cause considerable ripple on the active clamp capacitor, pushing up the peak voltage stress seen by the primary-side MOSFET. This ripple can be reduced by using a larger active clamp capacitor and a proportionally larger RC snubber capacitor. See Active Clamp Capacitor section for more information.

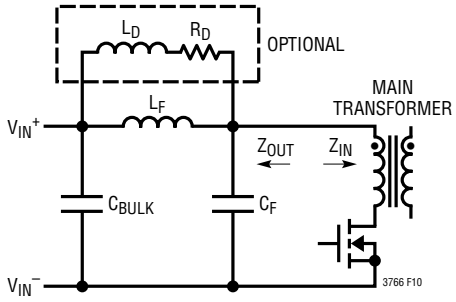

Figure 10. Input Filter with Optional Damping Network

Once the required BV_{DSS} of the N-channel MOSFET is known, choose a MOSFET with the lowest available on-resistance ($R_{DS,ON}$) that has been optimized for switching applications (low Q_G). In most applications, the MOSFET will be used at a drain current that is a fraction of the maximum rated current, so this rating is not normally a consideration. The total losses associated with the N-channel MOSFET at maximum output current can be estimated using:

$$P_{PG} = \left(\frac{N_S}{N_P}\right)\frac{V_{OUT}(I_{MAX})^2}{V_{IN}}(1+\delta)R_{DS(ON)} + \left(\frac{N_S}{N_P}\right)\frac{V_{CL}I_{MAX}R_{DR}Q_{GD}f_{SW}}{2V_{MILLER}} + Q_{GTOT}V_{CC}f_{SW}$$

where δ is the temperature dependence of the on-resistance and V_{CL} is the active clamp voltage (see Active Clamp Capacitor section). R_{DR} (approximately 1.7Ω for the LTC3765) is the gate drive output resistance at the MOSFET's miller plateau voltage, V_{MILLER}. The values of Q_{DG}, Q_{GTOT} and V_{MILLER} can be taken from the V_{GS} versus Q_G curve that is typically provided in a MOSFET data sheet. Q_{GD} is the change in gate charge (Q_G) during the region where the V_{GS} voltage is approximately constant and equal to miller voltage, V_{MILLER}. The total gate charge (Q_{GTOT}) is the gate charge when $V_{GS} = V_{CC}$. The three parts in the above equation represent conduction losses, transition losses and gate drive losses respectively. Highest efficiency is obtained by selecting a MOSFET that achieves a balance between conduction losses and the sum of transition and gate drive losses. Note that the above equation for P_{PG} is an approximation that includes assumptions. First, it is assumed that the turn-on transition losses are relatively small because of the leakage inductance in the main transformer. Also, it is assumed that the energy stored in this leakage inductance at primary-switch turn-off is completely recovered by the active clamp capacitor. For most applications, these assumptions are valid and the above equation is a good approximation.

The active clamp P-channel MOSFET has the same BV_{DSS} requirement as that of the N-channel MOSFET. Since the P-channel MOSFET only handles the magnetizing current, it is normally much smaller (typically a SOT package). To accommodate abnormal transients, use a P-channel MOSFET that has a pulsed drain current rating of 2A or higher. Also, note that when the N-channel MOSFET turns off, the leakage inductance will momentarily force the reflected load current into the body diode of the P-channel MOSFET. Consequently, the body diode should be rated to handle a pulsed forward current of:

$$I_{D(MAX)} = \left(\frac{N_S}{N_P}\right)I_{MAX}$$

In some cases, it may be more practical to add a separate diode in parallel with the body diode of the P-channel MOSFET.

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The primary-side P-channel MOSFET may be driven by a simple level-shift circuit that shifts down the drive voltage on the LTC3765 AG pin. Alternatively, the level-shift circuit can be omitted if the source of the P-channel MOSFET is returned to the V_{CC} pin of the LTC3765. Refer to the LTC3765 data sheet for details.

In nonisolated applications where the LTC3766 is used standalone, it is necessary to use a resonant reset technique instead of the active clamp reset. As a result, there are special considerations in selecting the primary-side MOSFET. See the Nonisolated Applications section for additional information.

Secondary-Side Power MOSFET Selection

On the secondary side, the peak-to-peak drive level for the N-channel MOSFETs is determined by the V_{CC} pin on the LTC3766. Assuming that one or both of the linear regulators in the LTC3766 are used, the V_{CC} regulation voltage can be set to either 7V or 8.5V as needed for driving the gates of the MOSFETs.

The first step in selecting the secondary-side MOSFETs is to determine the needed breakdown voltage. The maximum voltage seen by the synchronous MOSFET is approximately:

$$V_{DS(SG)} = 1.2 \bullet \left(\frac{N_S}{N_P}\right) V_{IN(MAX)}$$

where the factor of 1.2 has been added to allow for ringing and overshoot. This assumes that a snubber has been used on the secondary side of the main transformer (see the RC Snubbers section). If no snubber is used, the ringing and peak overshoot will be considerably higher. The maximum voltage seen by the forward MOSFET is approximately:

$$V_{DS(FG)} = \frac{1.2 \bullet V_{OUT}}{1 - \frac{V_{OUT}}{V_{IN(MIN)}}\left(\frac{N_P}{N_S}\right)}$$

where the factor of 1.2 has again been added to allow for ringing and overshoot.

Having determined the BV_{DSS} requirement for the forward and synchronous MOSFETs, the next step is to choose the on-resistance. Since both secondary-side MOSFETs are zero-voltage switched, choose MOSFETs that have a low $R_{DS(ON)}$ and have been optimized for use as synchronous rectifiers, including a body diode with a fast reverse recovery if possible. In most applications, the nominal input voltage will correspond to approximately 50% duty cycle, so the forward and synchronous MOSFETs will be selected to have the same $R_{DS(ON)}$. The power loss associated with the forward MOSFET can be approximated by:

$$P_{FG} = \left(\frac{N_P}{N_S}\right)\frac{V_{OUT}(I_{MAX})^2}{V_{IN}}(1+\delta)R_{DS(ON)} + Q_{GTOT}V_{BIAS}f_{SW}$$

where δ is the temperature dependence of the on-resistance and V_{BIAS} is the input to the LTC3766 linear regulator (if used). The value for Q_{GTOT} can be taken from the V_{GS} versus Q_G curve given in the MOSFET data sheet. Q_{GTOT} is the value of Q_G when $V_{GS} = V_{CC}$, where V_{CC} is the voltage on the V_{CC} pin of the LTC3766. For the synchronous MOSFET, the power loss is approximately:

$$P_{SG} = \left(1 - \frac{N_P}{N_S}\frac{V_{OUT}}{V_{IN}}\right)(I_{MAX})^2(1+\delta)R_{DS(ON)} + Q_{GTOT}V_{BIAS}f_{SW}$$

The power losses for the synchronous and forward MOSFET are generally dominated by conduction losses. For both of the above power loss equations, it is assumed that the dead time (when the MOSFET body diode is conducting) has been minimized. See Setting the Gate Drive Delays section for details on minimizing the dead time.

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V_{CC} and Drive Mode Selection

In order to accommodate various operating gate voltages that may be required by the secondary-side MOSFETs, the MODE pin can be used to set the LTC3766 for either LV mode or HV mode operation. In LV mode, the V_{CC} regulation point for both linear regulators is set to 7V, while the V_{CC} UVLO and V_{AUX} switchover rising thresholds are adjusted to 4.7V. In HV mode, the V_{CC} regulation point is set to 8.5V, while the V_{CC} UVLO and the V_{AUX} switchover rising thresholds are set to 7.9V and 8V respectively. Use LV mode for MOSFETs that are rated for 4V to 5V operation, and use HV mode for those rated with 7V to 10V operation. The V_{CC} regulation levels, as well as the UVLO and switchover voltages have been optimized to ensure that both types of MOSFETs are operated safely and efficiently. In general, MOSFETs with a higher V_{DS} rating also have a higher operating gate voltage rating. As a result, applications with output voltages of approximately 12V and higher will generally use MOSFETs that are rated for 7V to 10V gate operation.

In addition to changing the V_{CC} regulation, UVLO and V_{AUX} switchover levels, the selection of HV mode or LV mode also changes the behavior of the SG reverse overcurrent. In LV mode, the reverse overcurrent threshold on the SW pin is 73mV and the adjust current is 103µA. In HV mode, these levels are changed to 148mV and 42µA to account for the fact that high voltage MOSFETs have larger on-resistance than low voltage MOSFETs. For details, see the Setting the SG Reverse Overcurrent.

In applications where the LTC3766 is used in conjunction with the LTC3765, the signals on the PT^+ and PT^- pins contain encoded PWM information with amplitude equal to the V_{CC} voltage. This encoded gate drive signal is received by the LTC3765 and decoded into PWM and clock information that drives the primary-side MOSFETs. However, the LTC3766 can also be used standalone in nonisolated forward converter applications. In such applications, the MODE pin can be used to disable the PWM encoding on the PT^+ and PT^- pins. As a result, the LTC3766 will generate a normal PWM gate drive signal on the PT^+ pin and a reference clock on the PT^- pin. Also, in standalone mode the FGD pin is ignored and the dead time between SG falling and PT^+ rising is set adaptively.

The MODE pin has four possible states. Tying MODE to GND or V_{CC} will provide encoded gate drive signals with either LV mode or HV mode operation respectively. Tying MODE to GND through either a 100k or a 50k resistor will provided standard PWM gate drive signals with either LV mode or HV mode operation respectively. Table 3 Summarizes the use of the MODE pin for setting the operating voltage and gate drive encoding modes, and Table 4 summarizes the effect of low voltage and high voltage gate drive operating modes.

Table 3

MODE PIN	DRIVE LEVEL	PT^+/PT^- MODE	INTENDED APPLICATIONS
GND	LV	Encoded PWM	Low V_{OUT} Isolated Apps with LTC3765
V_{CC}	HV	Encoded PWM	High V_{OUT} Isolated Apps with LTC3765
100k to GND	LV	Standard PWM	Low V_{OUT}, Nonisolated Apps, Standalone
50k to GND	HV	Standard PWM	High V_{OUT}, Nonisolated Apps, Standalone

Table 4

DRIVE LEVEL	V_{CC}	V_{CC} UVLO THRESHOLD (RISE/FALL)	V_{AUX} SWITCHOVER THRESHOLD (RISE/FALL)	SG OVERCURRENT	
				V_{TH}	I_{SW}
LV	7.0V	4.7V/3.9V	4.7V/4.5V	73mV	103µA
HV	8.5V	7.9V/6.9V	8.0V/7.7V	148mV	42µA

Input Capacitor/Filter Selection

In applications with a low impedance source, or where there the input voltage is relatively low, a simple capacitive input filter is generally suitable. This capacitor needs to have a very low ESR and must be rated to handle a worst-case RMS input current of:

$$I_{C(RMS)} = \left(\frac{N_S}{N_P}\right)\frac{I_{OUT(MAX)}}{2}$$

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Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3766, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

For higher input voltage applications, however, it can be very costly to use bulk capacitance that is rated to handle the required RMS current. Also, if a simple capacitor is used as an input filter, it is hard to know exactly where the AC input current will flow when a power supply is placed into a larger system. To avoid these issues, an LC filter can be used on the power supply input as shown in Figure 10. This keeps the large AC currents contained in relatively small and inexpensive capacitors whose RMS current rating is known to be adequate. Choosing an LC filter such that:

$$\frac{1}{2\pi\sqrt{L_F C_F}} < \frac{f_{SW}}{5}$$

will attenuate the AC content of the RMS input current by a factor of approximately 5×. This greatly alleviates the RMS current requirements of the bulk input capacitor. The filter inductor should have a saturation current of at least:

$$I_{SAT(LF)} \geq 1.3 \bullet \frac{V_{OUT} I_{OUT(MAX)}}{V_{IN(MIN)}}$$

In order to keep the ripple voltage at the filter output to a reasonable level, choose a value of L_F and C_F that also satisfies:

$$\sqrt{\frac{L_F}{C_F}} < 2.9 \bullet \left[\left(\frac{N_S}{N_P} \right) \frac{V_{RIPPLE}}{I_{OUT(MAX)}} + \frac{R_{ESR}}{2} \right]$$

where V_{RIPPLE} is the desired ripple voltage at the output of the input filter and R_{ESR} is the ESR of capacitor C_F. A reasonable target for V_{RIPPLE} 3% of nominal V_{IN}.

When using an LC input filter, the output impedance of the LC filter must never be greater in magnitude than the input impedance looking into the power stage of the DC/DC converter. This is necessary to avoid loop instabilities. In most applications, this condition is naturally satisfied because the ESR of the bulk input capacitance, C_{BULK}, is high enough to lower the Q of the LC input filter, thereby reducing the peaking in its output impedance to a safe level. Also, using a larger value for C_F reduces the Q, although this can be expensive in high V_{IN} applications. In some situations, a series damping network must be added as shown in Figure 10.

In order to provide critical damping, choose LD and RD according to:

$$L_D = \frac{L_F}{5} \text{ and } R_D = 0.8\sqrt{\frac{L_F}{C_F}}$$

The damping inductor L_D does not carry the DC input current. However, to ensure adequate attenuation during large transients, choose an inductor whose saturation current is at least:

$$I_{SAT(LD)} \geq 0.6 \left(\frac{V_{OUT} I_{OUT(MAX)}}{V_{IN(MIN)}} \right)$$

Output Capacitor Selection

The selection of C_{OUT} is driven by the effective series resistance (ESR) and the resulting output voltage ripple. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 f_{SW} C_{OUT}} \right)$$

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where f_{SW} is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Current Sensing and Average Current Limit

The LTC3766 supports current sensing either with a current sense resistor or with an isolated current transformer. A current transformer is generally more efficient and has the advantage of sensing current on the primary side in isolated applications. This can be important because it provides an additional safeguard against saturating the main transformer during load transients. In addition, a current transformer can generate a much larger current sense signal than a sense resistor, resulting in a vastly superior signal to noise ratio. This eases board layout concerns for noise pickup and reduces jitter as well. Also, the accuracy of LTC3766 current limit is significantly better in current transformer mode than in current sense mode.

Compared to a current transformer, a current sense resistor is less expensive and somewhat simpler to apply than a current transformer. **When current sensing on the secondary side of an active clamp forward converter, Direct Flux Limit is required to prevent transformer saturation and possible damage of the primary-side MOSFET.** This is because the current loop does not see the magnetizing current, and will not provide its own safeguard against saturation. Note that in nonisolated applications, however, the current sense resistor is placed in series with the primary-side switch, so the current loop will be monitoring magnetizing current.

When using a current sense resistor, the I_S^+ and I_S^- pins operate differentially and the maximum peak current threshold is approximately 75mV. Normally, the current sense resistor is placed in the source of the forward MOSFET, as shown in Figure 11. Depending on PCB layout and the shielding of the traces going to the I_S^+ and I_S^- pins, it is sometimes necessary to add a small amount of filtering as shown in Figure 11. Typically, values of R_{FL} = 100Ω and C_{FL} = 200pF to 1nF will provide adequate filtering of noise pickup without substantially affecting the current loop response.

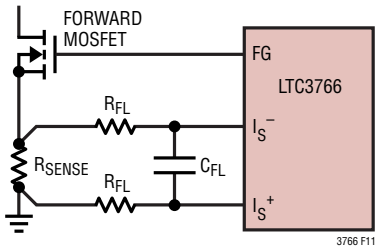

Figure 11. Using a Current Sense Resistor

This filter is also helpful in correcting for the effect of the ESL (parasitic inductance) of the sense resistor, which can be important for R_{SENSE} values less than 2mΩ. The effect of the ESL is cancelled if the RC filter is chosen so that:

$$R_{FL}C_{FL} = \frac{ESL}{R_{SENSE}}$$

Since the LTC3766 implements an average current limit architecture, choose the value of R_{SENSE} based upon the desired average current limit:

$$R_{SENSE} = \frac{55mV}{I_{LIM(AVG)}}$$

Alternatively, if a current transformer is used to sense the primary-side switch current, then the I_S^- pin should be tied to V_{CC} and the I_S^+ pin to the output of the current transformer. This causes the gain of the internal current sense amplifier to be reduced, so that the maximum peak current voltage is increased to approximately 1V. The current transformer connections are shown in Figure 12.

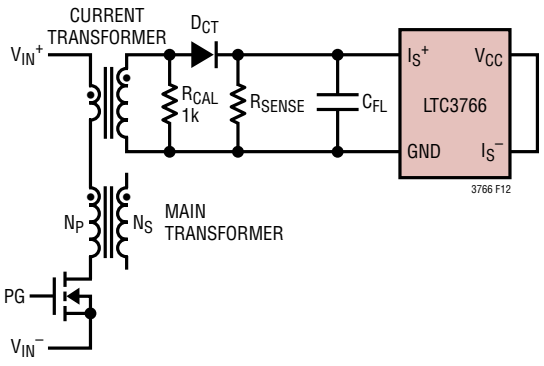

Figure 12. Using a Current Sense Transformer

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Typically, the current transformer is placed in series with the power supply feed to the main transformer. This reduces common mode noise, and is generally convenient for the PCB layout. Use a small filter capacitor, C_{FL}, between 1nF and 3.3nF, or a time constant for $R_{SENSE} \bullet C_{FL}$ of less than 75ns, to eliminate high frequency noise. The diode D_{CT} is needed to allow the core of the current transformer to properly reset.

When using a current transformer, set the value of R_{SENSE} using:

$$R_{SENSE} = \frac{0.73V}{K_{CT} I_{LIM(AVG)}} \bullet \frac{N_P}{N_S}$$

where N_P/N_S is the turns ratio of the main transformer, K_{CT} is the current gain of the transformer, and $I_{LIM(AVG)}$ is the average current limit desired. For most applications, a current transformer turns ratio of 1:100 is suitable (K_{CT} = 0.01).

The resistor R_{CAL} is added to compensate for the effects of the magnetizing current in the main and current sense transformers, both of which cause the voltage on R_{SENSE} to be somewhat higher than expected (2% to 8%). Typically, R_{CAL} is in the range of 1.5k to 5k. For the highest possible accuracy, the value of R_{CAL} should be adjusted to calibrate the current sensing at full load and nominal input voltage by carefully measuring the R_{SENSE} voltage and comparing it to the output inductor current. Figure 13 shows an example of a well-calibrated current sense transformer, where the R_{SENSE} voltage has been scaled by a factor of:

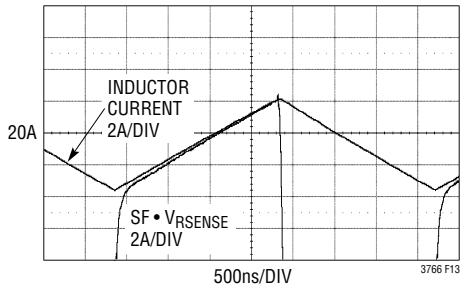

Figure 13. Properly Calibrated Current Transformer

$$SF = \frac{N_P}{R_{SENSE} K_{CT} N_S}$$

Because of the magnetizing current, the slope of the scaled R_{SENSE} voltage will not exactly match that of the inductor current. Choose R_{CAL} so that the scaled R_{SENSE} voltage and the inductor current are identical at the peak.

In order to maintain a constant average current while in current limit, the LTC3766 automatically adjusts the value of the peak current limit to cancel the effect of the inductor ripple current. This is accomplished by creating an internal ramp that mimics the inductor current ripple. The amplitude of this ramp is determined by the resistor on the I_{PK} pin, which must be set to be proportional to the output inductor. The LTC3766 establishes a voltage on the I_{PK} pin of $(V_{SW} – V_S^+)/15$, which is one-fifteenth of the voltage across the output inductor during the on-time when SW is high. Therefore, it is imperative that the SW and V_S^+ pins be connected as shown in Figure 14 or Figure 15 so that the LTC3766 can properly sense the inductor voltage. If the differential amplifier is not needed, tie V_S^- and V_S^+ together to V_{OUT} as shown in Figure 14b.

For high V_{OUT} applications where the SW node plateau voltage is greater than 40V, it is necessary to add a resistor divider on both the SW and V_S^+ pins, as shown in Figure 15. This divider will limit the voltage at the SW pin and also impact the SG reverse overcurrent trip threshold. See Setting the SG Reverse Overcurrent for details on selecting the resistor divider on the SW pin.

Note that the ratios of the resistor dividers on the SW and V_S^+ pins must be the same for ripple cancellation to operate properly. This requires that:

$$K_R = \frac{R2}{R1+R2} = \frac{69k \bullet R4}{69k \bullet R4 + R3(69k + R4)}$$

where the 69k accounts for the internal resistance on the V_S^+ and V_S^- pins.

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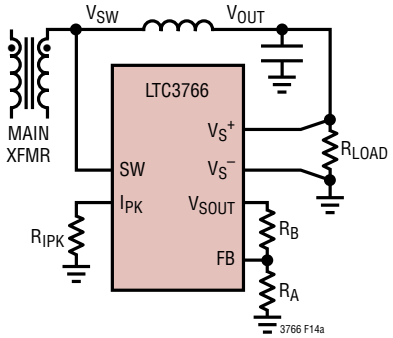

Figure 14a. Setting the Average Current Limit (R_{IPK})

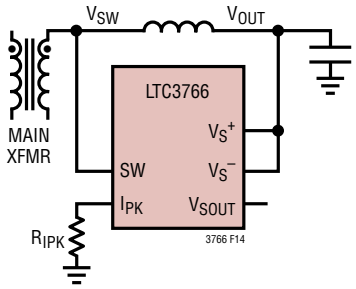

Figure 14b. Setting R_{IPK} with No Differential Amplifier

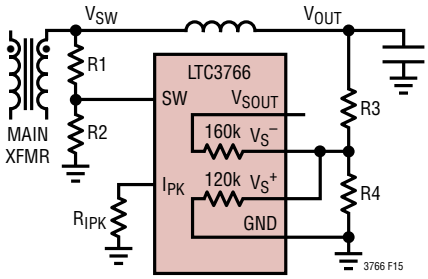

Figure 15. Setting R_{IPK} for High V_{OUT} Applications

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For resistor sense mode, place a resistor on the I_{PK} pin that is chosen using:

$$R_{IPK} = \frac{K_R L_{IPK}}{(17.6nF)R_{SENSE}}$$

where L_{IPK} is the inductance of the output inductor at I = $I_{LIM(AVG)}$. For low V_{OUT} applications where no SW node divider is needed, K_R = 1. For current transformer mode, use:

$$R_{IPK} = \frac{K_R L_{IPK}}{(1.32nF)K_{CT}R_{SENSE}} \bullet \frac{N_P}{N_S}$$

When the LTC3766 is in current limit and the output voltage is very low, the control of the output current will be limited by the minimum on-time of the converter. Once this minimum on-time has been reached, further decreases in output voltage during current limit will result in an inductor current that continues to rise, until the overcurrent limit is reached. This will cause the LTC3766 to shut down and attempt a restart, resulting in a hiccup mode of operation.

Typical average current limit performance is illustrated in Figure 16. Note that the average current delivered to the load is held substantially constant as the output voltage is decreased down to a low level, at which point the converter will enter hiccup mode. Depending upon the particular application, hiccup mode is entered either due to the loss of secondary-side bias voltage (UVLO) or due to an overcurrent fault.

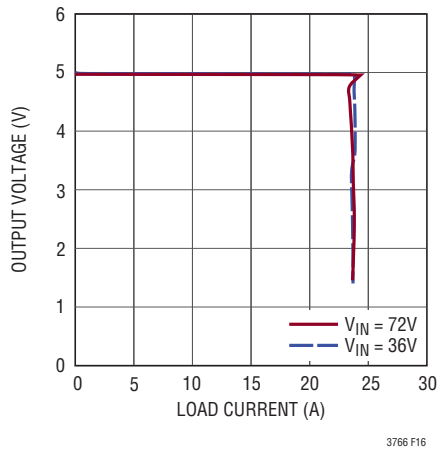

Figure 16. Typical Current Limit Performance

Estimating the Average Current Limit Accuracy

The accuracy of the average current limit depends on the LTC3766 specifications together with a number of application circuit parameters as well as parasitics. Consequently, it is very difficult to precisely calculate the average current limit accuracy. This accuracy can be estimated, however, by carefully considering the three primary sources of error:

1. The accuracy of the current sense resistor and/or current sense transformer. For resistor sensing, the accuracy of the current sense resistor is normally 1%. For sense resistors less than 2mΩ, however, the parasitic inductance can cause a significant error in the sensed current. This error can be eliminated by adding an RC filter as shown in Figure 11.

   When using a current transformer, the accuracy of the sense resistor on the current transformer secondary and the turns ratio of the transformers (both K_{CT} and N_P/N_S) are generally 1% or better. Depending on where the current sense transformer is placed, however, there can be an additional 1% to 4% error due to the magnetizing current of both the main and current sense transformers. Generally, this error is in the form of a relatively constant offset, and it can be adjusted out for a particular design for nominal input voltage and maximum load current. The resulting tolerance due to the variation in magnetizing current effects is generally less than 2%, resulting in an overall accuracy of approximately 3% for current transformer sensing.

2. The accuracy of the average current sense threshold $V_{IS(AVG)}$. The accuracy of the LTC3766 current sense threshold is given in the Electrical Characteristics table and depends on the current sense mode chosen. Current transformer mode provides an accuracy of 10% and is more accurate than the resistor sense mode accuracy of 15%.

3. The accuracy of the compensation for inductor ripple current. The accuracy of the inductor ripple compensation depends both on the internal adjustment of V_{ITH} as well as the tolerance of the output inductor itself. For most application circuits, the ripple compensation accuracy will be 25% or better for current transformer mode, and 35% or better for resistor sense mode. Note

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that the inductor current ripple is typically 30% to 60% of the average current limit, and only one-half of this peak-to-peak ripple is being compensated. As a result, the effect of the ripple compensation accuracy on the average current limit is attenuated by a factor of:

$$F_R = \frac{R}{R+2}$$

where R is the ratio of the peak-to-peak inductor ripple current to the average current limit. For 30% to 60% ripple, for example, the value of F_R varies from 0.13 to 0.23.

Considering each of the above factors, the worst-case tolerance of the average current limit can be estimated as:

ΔI_{AVG} = 3% + 10% + 0.23 (25%) = 18.5%

for current transformer mode and:

ΔI_{AVG} = 1% + 15% + 0.23 (35%) = 24%

for resistor sense mode. Since the three sources of error are statistically independent, the current limit tolerance for current transformer and resistance sense modes can be calculated using the RSS method as approximately 12% and 17% respectively.

Setting the Gate Drive Delays

The forward switch gate driver (FG) and the synchronous switch gate driver (SG) operate with make-before-break timing on the FG rising edge, and with simultaneous timing on the SG rising edge. The delays for these transitions relative to the switching of the primary-side MOSFETs are critical for optimizing efficiency, and can be configured independently using the SGD and FGD pins.

The SG rising delay should be adjusted to minimize the switch node (SW) body diode conduction. At full load, the power loss in the body diode is significant, and the SG rising delay can have a substantial impact on efficiency. By minimizing the dead time between PG falling and SG rising (while avoiding shoot-through), this power loss is also minimized. Similarly, the dead time between SG falling (set by the FG rising delay) and PG rising should also be minimized.

In addition to being set to minimize the dead time between SG falling and PG rising, the FG rising delay should also be adjusted to ensure that the drain of the forward switch (SWB) is close to 0V when the switch is turned on, which minimizes switching loss. When the LTC3765 active clamp switch turns off, the drain voltage of the primary switch (SWP) decreases linearly from $V_{IN}/(1 – D)$ to V_{IN}, where D is the duty cycle. On the secondary side of the transformer, SWB ramps from $V_{OUT}/(1 – D)$ to 0V. Switching power loss is minimized when FG and PG MOSFETs are switched with minimal drain-to-source voltage across them. The FG and PG rising delays should be adjusted to ensure that the SWB and SWP nodes are at their minimums when the switches are turned on.

Keep in mind the following set of relationships when setting the delays (refer to the Timing Diagram and Figure 1):

1. The forward gate (FG) always turns on with make-before-break timing relative to the synchronous gate (SG). This ensures that negative inductor current does not create excessive voltage on the synchronous switch drain.
2. Shoot-through is caused when the synchronous gate (SG) and the LTC3765 primary gate (PG) are simultaneously high, or when the forward gate (FG) is high and the LTC3765 active gate (AG) is low. The leakage inductance of the main transformer will prevent significant power loss due to shoot-through for a few tens of nanoseconds; however, if the PG and SG or FG and AG gates are on simultaneously for a longer period of time, the shoot-through will cause power loss, excessive heat, and potentially rapid part displacement.
3. The primary side turn-off of either AG or PG should occur before FG and SG switch, and the primary-side turn-on should occur after FG and SG switch. For example, on a particular cycle, AG goes high first (turning the PMOS off), then FG goes high, then SG goes low, then PG goes high. On the PG turn-off edge, PG goes low first, then FG goes low and SG goes high, then AG goes low (turning the PMOS on).

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Delay Resistor Selection: PG Turn-Off Transition

In general, the PG turn-off delays are relatively simpler to set and less critical than the PG turn-on delays. At the end of the PWM on-time, the LTC3766 will assert a falling edge on the PT+ pin, which in turn causes the LTC3765 to immediately turn off the PG MOSFET. Once the PG voltage falls below 1.5V, the LTC3765 waits for a fixed 180ns delay and then turns on the AG MOSFET. Consequently, the only delay adjustment to be made for this transition is on the secondary side using the SGD pin of the LTC3766. This pin is used to set the delay from PT+ falling to FG falling/SG rising, which must occur after PG turn-off and before AG turn-on.

The first consideration in setting the SGD delay is to reduce the dead time between PG and SG, during which the body diode of the synchronous MOSFET is carrying the load current. After PG turn-off, the SW node on the secondary side will rapidly fall until being clamped by the body diode of the SG MOSFET. The objective is to turn on the SG MOSFET as the SW node crosses through 0V. The LTC3766 makes this easy to achieve by directly sensing the SW node and inhibiting SG turn-on until SW has fallen through 0.5V. In other words, minimum dead time between PG and SG can be achieved by setting the SGD delay to any value less than or equal to the delay time from PT+ falling to SW falling through 0V. In general, this delay time is in the range of 50ns to 100ns. The resistor from SGD to ground that gives a particular delay t_{SGD} can be computed using:

$$R_{SGD} = (t_{SGD} - 12ns) \bullet \frac{1k\Omega}{4.3ns}$$

A 10k resistor from SGD to ground sets the FG falling/SG rising delay to approximately 50ns, which is generally a good starting point. **To prevent damaging cross conduction between the FG and AG MOSFETs, do not set the SGD delay to be longer than the 180ns fixed turn-on delay of the AG MOSFET.** Always start low when setting the SGD delay. This is safe because of the adaptive limit that inhibits premature SG turn-on. Note also that the adaptive limit on the SG turn-on delay has a 180ns timeout. This means that 180ns after PT+ falls (indicating the end of the PWM on-time), the SG pin will go high regardless of the voltage on the SW pin.

Another important consideration in setting the SGD delay is the prevention of SWP collapse due to excessive FG turn-off delay. After PG turn-off, the SWP node is quickly driven high by the transformer leakage to a level of approximately $V_{IN}/(1 – D)$. Ideally, it should remain at this voltage as FG turns off, SG turns on, and then AG turns on. However, if the delay to FG turn-off is too long, the SWP voltage will momentarily fall towards V_{IN}, and it will not rise again until being forced high by AG turn-on. This collapse of the SWP node is illustrated in Figure 17, and is more prominent at lighter loads.

It can significantly degrade efficiency as the SWP node is discharged and recharged every cycle, but it is easily avoided by further shortening the SGD delay. Although the LTC3766 inhibits the SG turn-on until SW < 0.5V, this is not true of the delay to FG turn-off. The delay from PT+ falling to FG turn-off can be decreased beyond the adaptive limit of SG turn-on, so that the FG and SG edges can be separated with a small dead time between them. This is

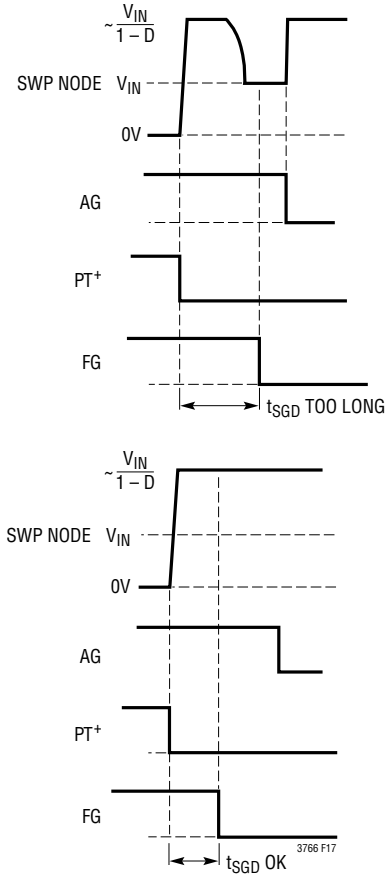

Figure 17. Avoiding SWP Collapse from Long Delay

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important to allow the FG turn-off to be separately optimized based upon circuit parasitics. In most applications, a peak in full load efficiency is normally found with the SGD delay set so that there is no SWP collapse and there is a small dead time between FG turn-off and SG turn-on.

In applications where efficiency is less critical, this delay can be set adaptively by tying SGD to GND. In this case, FG falling and SG rising will both be inhibited until SW < 0.5V. For fixed delay mode, always use a resistor of 8k or greater on the SGD pin to avoid activating the adaptive delay mode.

Delay Resistor Selection: PG Turn-On Transition

The delays associated with the PG turn-on transition are set by the DELAY pin on the LTC3765 and the FGD pin on the LTC3766. At the beginning of the PWM on-time, the LTC3766 will assert the PT^+ pin high, and will then turn FG on and SG off after a delay set by the resistor on the FGD pin. On the primary side, the LTC3765 will immediately turn off the AG MOSFET in response to PT^+ rising, and it will then turn on the PG MOSFET after a delay determined by the resistor on the LTC3765 DELAY pin. The FGD delay resistor on the secondary side must be selected in careful coordination with the delay on the primary side; therefore, the following procedure outlines how to choose components for both the LTC3765 and LTC3766.

The first objective in setting the PG turn-on delays is to minimize switching loss by turning on the PG and FG MOSFETs at minimum drain voltage. After the AG MOSFET has turned off, the PG and FG drain voltages (SWP and SWB) will naturally ramp down to approximately V_{IN} and 0V respectively. These voltages take 100ns to 500ns or longer to fall, depending on the main transformer magnetizing inductance and the parasitic capacitance on the MOSFET drains. Choosing the delay settings correctly can significantly impact the power loss due to switching the MOSFETs.

For a particular design, the most effective procedure is to set the PG and FG delays based on the resulting waveform on SWP and SWB. In order to evaluate these waveforms, the delays should initially be selected so that they are long, while keeping in mind that the FG delay must be less than the PG delay to prevent potentially damaging PG/SG cross-conduction. As a first pass, use a 75k resistor from FGD to ground for a 415ns delay and 60k resistor from DELAY to ground for a 622ns delay. The SWP and SWB waveforms should appear as shown in Figure 18.

The ramp rate on SWB and SWP is to a first order independent of duty cycle; however, the starting point of the ramp is a function of the duty cycle. Therefore, the longest delay time will be at high duty cycle when V_{IN} is at a minimum. For the lowest switching losses over the range of input voltage, the delays should be chosen based on the waveforms when V_{IN} is at its minimum operating voltage.

The resistor value from the FGD pin to ground should be selected first. This should be chosen to give a delay equal to the time from PT^+ rising until SWB ramps down to approximately 0V. The FGD resistor value can be determined from the following equation:

$$R_{FGD} = \left(t_{FGD} - 18ns\right) \bullet \frac{1k\Omega}{5.1ns}$$

Note that if the FG turns on before the SWP and SWB voltages have naturally fallen to their minimums, they will be instantly pulled to their minimum by the FG MOSFET turning on. This can give the appearance that FG is turning on after SWB has ramped to 0V, although it is actually premature. Turning on FG prematurely will slightly degrade efficiency due to increased switching loss; however, if the fall time of SWP and SWB exceed a maximum FGD delay of 600ns, it is acceptable to have premature FG turn-on

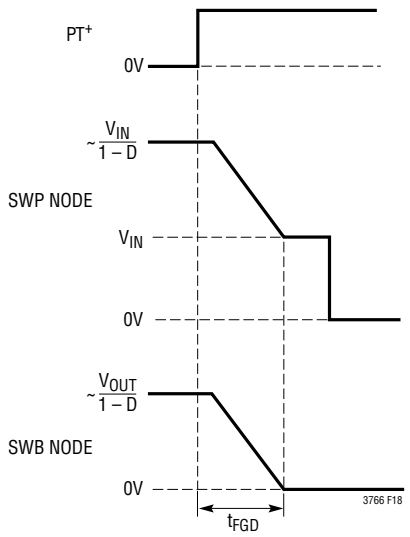

Figure 18. SWP and SWB Waveforms

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at low input voltage. Generally, the delay will be adequate at higher V_{IN} to allow a complete ramp down.

In rare cases, the LTC3765 and LTC3766 will be in delay phase-out mode when operating at minimum V_{IN} voltage. This will be apparent because the measured delay will be smaller than the programmed delay on either or both chips. This feature allows the LTC3765 and LTC3766 to operate at duty cycles up to a maximum of 79% by reducing the programmed delays when they would otherwise limit the maximum duty cycle. If this mode is evident, increase V_{IN} until delay phase-out is no longer active, and then set the FGD delay as described above.

Having set the FGD delay to optimize for low voltage switching, the PG delay is next chosen to minimize the dead time between SG turn-off and PG turn-on. The delay for the primary gate can be determined by taking the delay set tolerance and rise/fall times into account. The FG delay setting on the LTC3766 and the PG delay setting on the LTC3765 are both accurate to within 15% for a range of resistance values. Given this accuracy, a reasonable choice for the LTC3765 delay time is to set the PG delay time to $1.22 \bullet t_{FGD}$.

Be aware that the fall time of SG and the rise time of PG cannot be neglected. For example, if SG is driving a MOSFET with high input capacitance, and PG is driving a MOSFET with low input capacitance, then SG will fall slowly and PG will rise quickly. This increases the potential for shoot-through. Moreover, since SG will not turn off until FG turns on (make before break), the rise time of FG is also a factor. A final consideration is that the LTC3765 experiences a delay in PT^+ rising due to the pulse transformer. All of these considerations can be accounted for in the delay resistor selection by the following equation, in which $t_{D(PT)}$ is the delay time from PT^+ rising to IN^+ rising on the LTC3765, $t_{R(FG)}$ is the rise time of FG to 2V, $t_{F(SG)}$ is the fall time of SG to 1V and $t_{R(PG)}$ is the rise time of PG to 1V. The delay time can then be chosen such that:

$$t_{PGD} = 1.22 \bullet t_{FGD} + t_{R(FG)} + t_{F(SG)} - t_{R(PG)} - t_{D(PT)}$$

The resistor from the LTC3765 DELAY pin to ground can be selected to give this delay by using the following equation:

$$R_{DELAY} = \left(t_{PGD} - 45ns\right) \bullet \frac{1k\Omega}{9.5ns}$$

In practice, the LTC3765 PG turn-on delay should be optimized by monitoring the PG and SG waveforms. A conservative approach is to set the PG delay to create a dead time between SG falling and PG rising that accounts for the delay set tolerances (typically 22% of the total delay). A more aggressive approach takes into account the fact that transformer leakage inductance will delay the effect of PG turn on (i.e., SW node rising) by 75ns to 150ns or more at full load. Also, transformer leakage inductance mitigates the effect of a small amount of shoot-through by slowing the rise time of the transformer current. Higher full-load efficiency can be achieved by setting the PG turn-on closer to SG turn-off. In addition, a shorter dead time at PG turn-on can reduce the overshoot and ringing on the switch node, thereby reducing the size of the required RC snubber and its associated power loss.

While a shorter dead time at PG turn on can improve full-load performance, care must be taken to ensure that the worst case shoot-through at no load is well within safe limits.

Maximum Duty Cycle and Delay Phase-Out

While the PG turn-on delay time is important for reducing turn-on switching losses, no power is transferred from the input supply to the output load during this delay time. In most forward converter systems, the maximum available duty cycle is artificially limited by this delay, which then forces a trade-off between the optimal delay time and the maximum available duty cycle. The LTC3765 and LTC3766 implement a unique delay phase-out feature in which the PG and FG turn-on delays are gradually reduced as the demanded duty cycle approaches the maximum value of 79%. This feature allows a forward converter to be designed with an optimal delay at nominal input voltage, but still approach the maximum duty cycle at low input voltage, thereby making better utilization of the power transformer.

If continuous operation at maximum duty cycle is required, special attention must be paid to the fall time of the SW pin in order to avoid a Communication Lock Fault. In particular, the voltage on the SW pin should fall below 0.5V within 150ns of PT^+ falling. If the SW pin repeatedly falls more than 180ns after PT^+ falls while operating at maximum duty cycle, then the LTC3766 will interpret this condition as a loss primary-side power and generate a fault.

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Generating Secondary-Side Bias

There are five items to consider when determining the best way to generate bias for the LTC3766 in an isolated application:

1. The required operating current. This includes the gate drive current for both primary and secondary MOSFETs as well as the operating supply currents of both the LTC3765 and the LTC3766.
2. The operating voltage needed for the MOSFET gates. Depending on whether logic-level or standard threshold MOSFETs are used, the V_{CC} operating voltage and undervoltage lockout (UVLO) levels can be set accordingly using the MODE pin. The bias supply must provide adequate voltage to keep the LTC3766 V_{CC} pin above its UVLO level and keep the overall supply operating at peak efficiency.
3. Current limit operation at low output voltage. The minimum required V_{OUT} during current limit relative to the normal operating V_{OUT} has a major impact on the design of the bias supply. The bias supply must provide adequate voltage over this range of V_{OUT} voltages.
4. The variation in input voltage. At minimum input voltage, the bias supply must still provide enough voltage for proper operation. At maximum voltage, the bias supply must not generate a voltage that exceeds maximum ratings or dissipates excessive power.
5. The potential need for a rapid hand-off from primary to secondary control. In PolyPhase applications, it is important to quickly transfer control to the secondary side during start-up so that current sharing and proper phasing can be established before the full load current is seen at the output. By contrast, some applications may not need to have control handed off to the secondary until just prior to the output reaching its regulation value. **In all applications, however, the secondary bias must always come up and control must be transferred before the output reaches the regulation level.**

The current that must be supplied by the secondary bias supply can be estimated using

$$I_{VCC} \approx (Q_{GPRI} f_{SW} + 3mA) N_{PT} + Q_{GSEC} f_{SW} + 18mA$$

where Q_{GPRI} is the total gate charge of all primary-side MOSFETs, Q_{GSEC} is the total gate charge of all secondary-side MOSFETs, and N_{PT} is the turns ratio of the pulse transformer. Note that the primary-side current is scaled by the turns ratio of the pulse transformer. The 18mA constant in the above equation includes typical gate drive switching current as well as losses associated with the pulse transformer.

Using V_{OUT} Directly for Secondary-Side Bias

The simplest method of generating secondary-side bias is to directly use the output voltage of the converter. This is only practical when V_{OUT} is in the range of 5V to 15V. When V_{OUT} is in the range of 5V to 10V, it can be directly connected to V_{CC} as shown in Figure 4a. When V_{OUT} is in the range of 6V to 15V, it can be used as a bias input to the V_{AUX} regulator as shown in Figure 4b. For output voltages higher than 15V, this method is generally not practical due to high power dissipation. This simple method also does not provide constant current limit operation at lower output voltage. It also does not provide a quick hand-off to the secondary and is not recommended for PolyPhase applications.

Using a Peak Charge Circuit for Secondary-Side Bias

A common way to generate a bias voltage on the secondary side is by using a peak charge circuit connected to the transformer secondary, as shown in Figure 19. This circuit is useful for generating an unregulated bias voltage that can be directly tied to the V_{IN} pin of the chip and used as an input to the high voltage linear regulator.

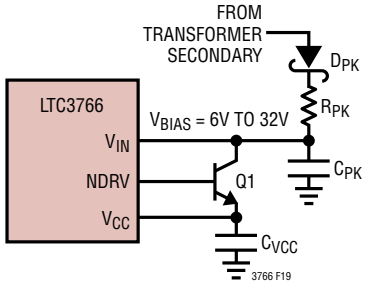

Figure 19. Peak Charge Circuit for Secondary Bias

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The peak charge circuit is capable of providing bias even at low output voltages, so it is a good choice when constant current limit operation is needed over a wide V_{OUT} range. Since it provides a bias voltage even when the converter is operating at tiny duty cycles, the peak charge is also a good choice for PolyPhase applications where a quick hand-off to secondary is important. However, since the output of a peak charge circuit directly follows changes in the converter input voltage, it is should only be used in applications where the input voltage varies by 2:1 or less. Note that for bias voltages on the V_{IN} pin of 28V or greater, the internal 30V clamp will draw between 3.5mA and 7mA. This will result in 100mW to 200mW of additional power dissipation in the LTC3766. To limit the initial charging current out of the peak charge circuit, use a series resistor R_{PK} in the range of 1Ω to 4Ω. A Schottky diode D_{PK} with a peak surge current rating of 5A or higher should also be used, and the pass transistor Q1 should have a minimum beta of at least 200. Capacitor C_{PK} should be a ceramic capacitor with a value of at least 2.2µF or greater.

During open-loop start-up, it is imperative that the peak charge bias come up and control is transferred to the secondary before an output overvoltage can occur. Since a peak charge circuit is not directly coupled to the output voltage of the converter, care must be taken to ensure that the primary-side soft-start is not too fast relative to the rise time of the peak charge bias on the secondary side. The time required for the peak charge bias voltage to rise to a level that allows control to be handed off to the secondary can be approximated using:

$$t_{BIAS} \approx 10^3 \bullet \sqrt{R_{EQ} C_{PK} C_{SSP}} + 150\mu s$$

where R_{EQ} is the sum of R_{PK} and the series resistance of diode D_{PK}, and C_{SSP} is the LTC3765 soft-start capacitor.

During open-loop soft-start, the time required for the converter output voltage to reach a given level V_{HO} can be approximated using

$$t_{OUT} \approx 10^4 \bullet \left(\frac{C_{SSP}^2 (V_{HO})^2 L C_{OUT} f_{SW}}{\left(V_{IN(MIN)} \bullet \frac{N_S}{N_P} \right)^2} \right)^{1/3}$$

The above equation assumes that there is no load current, which is the worst-case condition for output voltage rise. When calculating t_{OUT}, use a value for V_{HO} that corresponds to the target output voltage for control hand-off, typically one-half the normal regulation level or less. If t_{OUT} is less than t_{BIAS}, then the LTC3765 soft-start capacitor value should be increased. Note that these equations are approximations and the actual times will vary somewhat with circuit parameters.

Peak Charge Bias Configurations

When the peak voltage on the SW node is in the range of 7V to 32V, the peak charge can be taken directly from the SW node as shown in Figure 20. In practice, this condition only holds when the output voltage of the converter is approximately 5V.

In most applications, it is necessary to add an additional auxiliary winding on the secondary for use in generating an adequate bias voltage. For low V_{OUT} applications (V_{OUT} < 5V), this winding can be configured as shown in Figure 21 to provide a higher voltage for bias generation.

This configuration is advantageous because it achieves a higher voltage on the transformer secondary with a minimum number of additional turns. The number of turns on the auxiliary winding for this configuration should be approximately:

$$N_{AUX} \approx N_S \left(\frac{V_{B(MIN)} D_{MAX}}{V_{OUT}} - 1 \right)$$

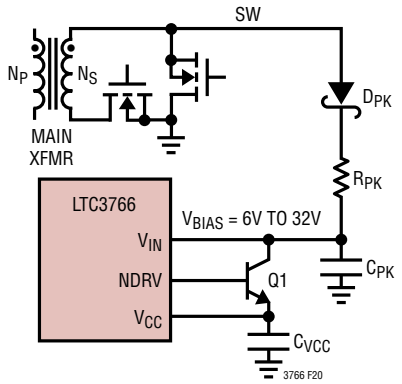

Figure 20. Peak Charge Directly from SW for V_{OUT} ≈ 5V

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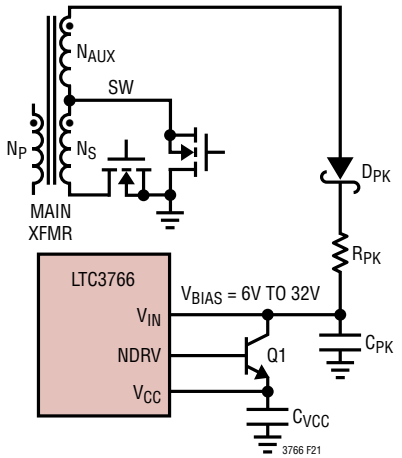

Figure 21. Peak Charge for Low V_{OUT} Applications

where D_{MAX} is the maximum operating duty cycle (typically 0.65 to 0.70) and $V_{B(MIN)}$ is either 7V for low voltage or 10V for high voltage drive mode operation. These values for $V_{B(MIN)}$ are approximately 2V higher than the UVLO levels on the LTC3766 to allow for drops in the peak charge circuit. As an example, for V_{OUT} = 1.5V, D_{MAX} = 0.65V and N_S = 1 turn, use N_{AUX} = 2 turns, assuming low voltage drive mode.

For high V_{OUT} applications (V_{OUT} > 6V), this winding can be configured as shown in Figure 22 to provide a reduced voltage for generating bias. In this case, choose an auxiliary winding with turns

$$N_{AUX} \approx N_S \left(\frac{V_{B(MIN)} D_{MAX}}{V_{OUT}} \right)$$

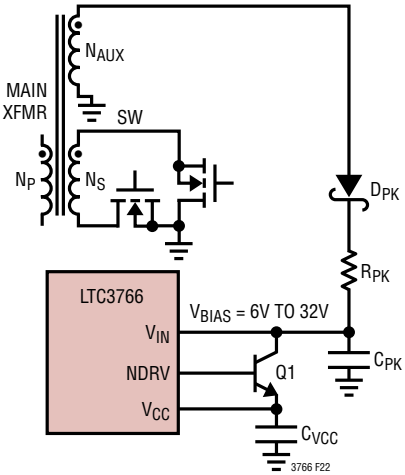

Figure 22. Peak Charge for High V_{OUT} Applications

At maximum V_{IN}, there may be considerable power dissipation in the linear regulator pass device Q1. This power can be calculated using

$$P_{Q1} = (V_{BIAS} - V_{CC})I_{VCC}$$

In applications where the peak charge and high voltage linear regulator must operate continuously, transistor Q1 must be capable of dissipating this power without excessive temperature rise. In such applications, use a transistor with a suitable package (SOT89) and connect the thermal tab of the transistor to an adequately large island of copper on the PCB.

High Efficiency Secondary-Side Bias Techniques

A high-efficiency alternative to using a peak-charge circuit to generate secondary-side bias is to connect a buck output to the transformer secondary. This buck output is normally combined with a peak charge circuit as shown in Figures 23 and 24. The bias voltage from this buck output can be fed directly into the V_{AUX} pin. This arrangement combines the quick start-up and flexibility of a peak charge circuit with the higher operating efficiency of a buck bias supply.

For Figure 23, the output voltage of the buck bias supply is given by:

$$V_{BUCK} = V_{OUT} \left(1 + \frac{N_{AUX}}{N_S} \right) - 0.5$$

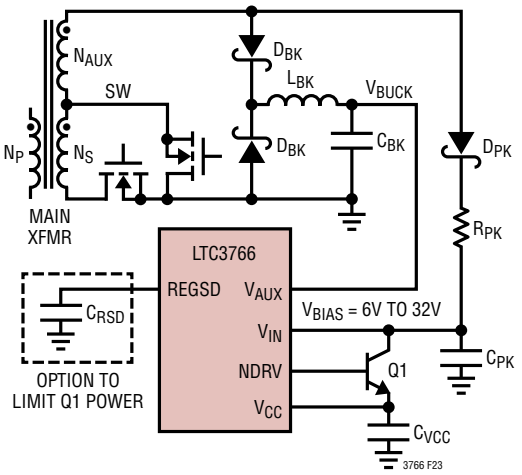

Figure 23. Buck Bias Supply for Low V_{OUT} Applications

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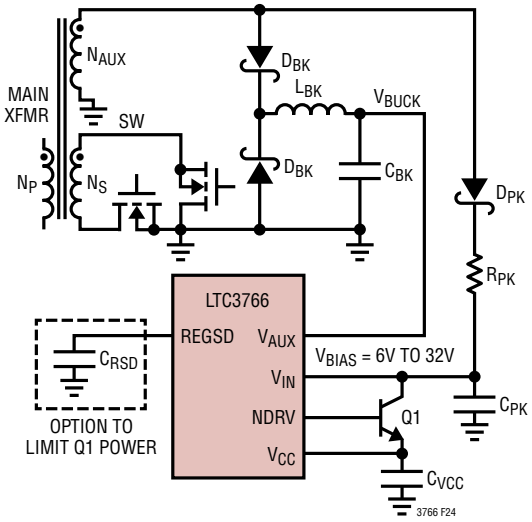

Figure 24. Buck Bias Supply for High V_{OUT} Applications

For Figure 24 the output is given by:

$$V_{BUCK} = V_{OUT}\frac{N_{AUX}}{N_S} - 0.5$$

For a buck bias supply, inductor L_{BK} must be rated to carry the required V_{CC} bias current and should have an inductance value that will provide continuous current operation at one-fourth of the required bias current load or less. Choose and inductor L_{BK} to according to:

$$L_{BK} > \frac{V_{CC}}{I_{CC} f_{SW}}$$

A value of 1mH for L_{BK} is adequate for most applications.

The output voltage of the buck bias supply (V_{BUCK}) should be set to optimize efficiency during normal operation. This will typically require a somewhat higher number of auxiliary turns than is ideal for a peak charge output. As a result, the buck supply and the peak charge circuit are sometimes driven from separate auxiliary windings. Also, note that the output voltage of the peak charge circuit will increase somewhat when the V_{AUX} bypass regulator is activated and the high voltage linear regulator is disabled. Care must be taken not to exceed the maximum voltage rating on the V_{IN} pin of the LTC3766.

The buck bias winding can also be used standalone without the peak charge supply, as shown in Figure 25. This is sometimes done in applications where the peak charge circuit is impractical, such when the V_{IN} voltage has a wide range.

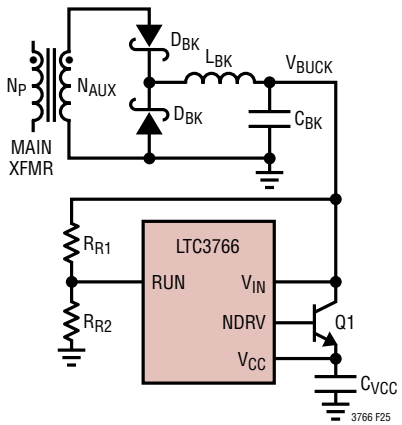

Figure 25. Using the Buck Bias Supply Standalone

When using the buck bias supply standalone, particular care must be taken to ensure that the bias output comes up more quickly than the main output, and that there is adequate bias voltage immediately after control hand-off. This is made more difficult by the presence of some load on the V_{CC} pin during start-up whereas there may be no load on the main output. In general, a clean start-up with a standalone buck bias supply can be achieved by observing the following guidelines: 1) set the turns ratio of the auxiliary winding so that the operating V_{AUX} will be at least 3V above the rising V_{CC} UVLO voltage, 2) use a smaller value for L_{BK}, typically one-half of that calculated in the above equation, but always large enough for continuous current in L_{BK} during normal operation 3) use the high-voltage linear regulator to minimize the load on V_{CC} during start-up, 4) use the RUN pin to monitor the bias voltage and set the start-up voltage to 2V above the rising V_{CC} UVLO voltage with a hysteresis of 1.5V, 5) use a shorter soft-start time, less than 10ms if possible, 6) use a small V_{CC} capacitor (typically C_{VCC} = 0.22µF) and a capacitor C_{BK} given by:

$$C_{BK} = \frac{20\left[\left(Q_{GPRI} f_{SW} + 3mA\right)N_{PT} + 18mA\right]}{f_{SW} V_{HYST}}$$

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where V_{HYST} is the hysteresis set by the RUN pin (1.5V). Note that this value for C_{BK} is as small as possible so that V_{BUCK} rises quickly, but large enough to support the bias current until control is handed off to the secondary and the duty cycle increases. Once control is handed off, both the buck supply and the main converter will be operating in continuous current mode, so their outputs will track.

Another high efficiency option for generating bias is to make use of an inductor overwinding, as shown in Figure 26. This supply is created by adding a second winding on the main output inductor.

During the on-time of the synchronous MOSFET, the V_{OUT} voltage is scaled and coupled through diode D_{OW} to capacitor C_{OW}, so that the resulting bias voltage is:

$$V_{OW} = V_{OUT}\frac{N_{L2}}{N_{L1}} - 0.5$$

This is similar to the buck supply in that it is highly efficient and fairly well regulated. However, it is simpler in that it does not require the use of an additional inductor to generate the bias voltage. Another advantage of this technique is that the bias voltage always tracks V_{OUT}, so there is no concern about the bias voltage potentially lagging the output voltage during start-up. Like the buck bias supply, the inductor overwinding can be used either stand alone (as shown in Figure 26) or together with a peak charge bias supply. Use a Schottky diode D_{OW} with a peak surge current rating of 5A or higher. Capacitor C_{OW} should be a ceramic capacitor with a value of 2.2µF or greater.

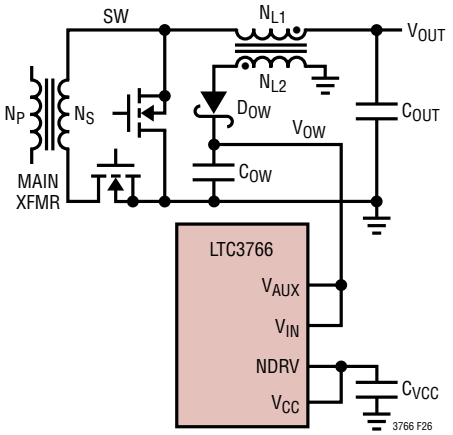

Figure 26. Inductor Overwinding Bias Supply

A useful variant of the inductor over-winding bias supply is shown in Figure 27, where a discrete transformer T_{OW} has been used instead of an additional winding on the main inductor L_F. This is often more convenient because standard parts can readily be used.

In the circuit of Figure 27, a second diode D_{OW2} has been added to prevent DC bias current from being carried in the transformer T_{OW}. This transformer can be either a gate-drive or flyback-style transformer, which are widely available in a range of turns ratios. Note that transformer T_{OW} requires only functional isolation and can be physically very small. This circuit produces a bias voltage given by:

$$V_{OW} = (V_{OUT} - 0.5)\frac{N_{L2}}{N_{L1}} - 0.5$$

During an output overload condition, the voltage generated by a either a buck supply or inductor overwinding supply will drop as the converter output voltage decreases. If this happens and there is no peak charge bias supply,

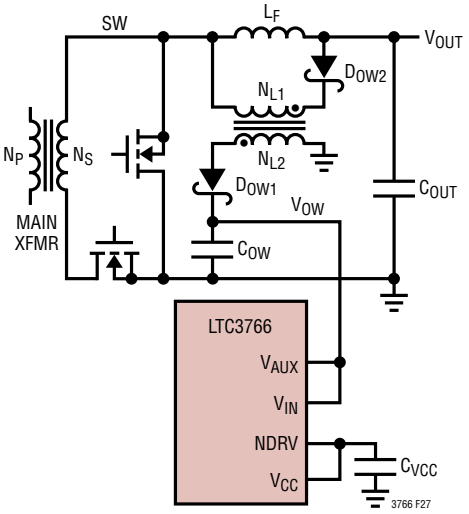

Figure 27. Inductor Overwinding Using Standard Parts

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then the LTC3766 will have a UVLO fault that will cause both the LTC3765 and LTC3766 to shut down and attempt a restart. If a peak charge supply is used together with a buck or inductor overwinding supply, then the LTC3766 will automatically re-energize the high voltage linear regulator when the V_{AUX} pin gets too low. If continuous operation of the peak charge and high voltage regulator is not needed, then the REGSD pin can be used to limit the total time that this regulator is allowed to operate (shown as an option in Figures 23 and 24). This enables a low power pass transistor to be used. See Linear Regulator Operation for more information on using the REGSD feature.

Soft-Start Ramp Time and Control Hand-Off

The soft-start ramp time on the LTC3766 is set by placing a capacitor between the SS pin and GND. This secondary-side soft-start capacitor only controls the output voltage ramp after control hand-off has taken place. Consequently, its effect on the overall output voltage start-up will depend on the primary to secondary hand-off voltage in the particular application. Choose a soft-start capacitor using:

$$C_{SS} = \frac{(5\mu A)\,t_{SS}}{1.83\left(0.6 - V_{FB(HO)}\right)}$$

where t_{SS} is the soft-start time after control hand-off to the secondary and $V_{FB(HO)}$ is the voltage on the FB pin at control hand-off. The total soft-start time will be the sum of t_{SS} and the open-loop soft-start time prior to control hand-off set by the LTC3765. Note that during the open-loop soft-start time, the output voltage ramp will vary significantly with load, since the synchronous MOSFET is not enabled and the converter may operate in discontinuous current mode. If precise control over the soft-start time is desired, use a secondary-side bias scheme that provides control hand-off at the lowest possible output voltage. See above sections on generating secondary-side bias for details. A soft-start capacitor between 8.2nF and 2.2µF is recommended to ensure a proper start-up.

Just prior to control hand-off, the LTC3766 rapidly presets the soft-start capacitor so that the internal soft-start voltage is equal to $V_{FB(HO)}$, ensuring a smooth transition from primary to secondary control. Due to the dielectric absorption of the soft-start capacitor, however, the voltage on the soft-start capacitor may droop somewhat following the initial preset. This can result in a small step down in the output voltage ramp after control hand-off, and an associated negative current transient in the output inductor. To minimize this effect, use a soft-start capacitor with a low dielectric absorption, such as an NPO ceramic capacitor.

Pulse Transformer Selection

The pulse transformer that connects the LTC3766 PT^+/PT^- outputs to the LTC3765 IN^+/IN^- inputs functions as the communication link between the secondary-side controller and the primary-side gate driver, as shown in Figure 28. In addition, LTC3765 contains a bridge rectifier that extracts bias power from the pulse transformer, which it then uses to drive the gates of the primary-side MOSFETs.

The designs have been coordinated so that the transformer turns ratio should be set to:

$$N_{PT} = N_{LTC3765}: N_{LTC3766} = 2:1$$

for low voltage mode operation on the LTC3766 (V_{CC} = 7V), and:

$$N_{PT} = N_{LTC3765}: N_{LTC3766} = 1.25:1$$

for high voltage mode operation on the LTC3766 (V_{CC} = 8.5V). The resulting V_{CC} voltage on the LTC3765 is approximately:

$$V_{CC(3765)} = V_{CC(3766)}N_{PT} - 1.3$$

Using the above turns ratios will provide a primary-side V_{CC} voltage of approximately 12V for the LTC3765 to drive the gates of the primary-side MOSFET. Note that the primary-side V_{CC} voltage provided by the pulse transformer must also be greater than the LTC3765 UVLO threshold for

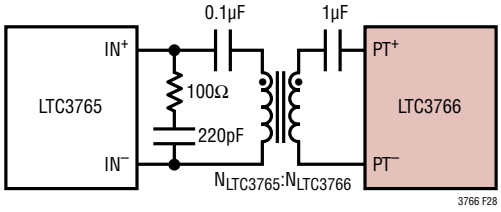

Figure 28. Pulse Transformer Connection

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proper operation. Care must also be taken not to exceed the maximum voltage rating on the LTC3765 V_{CC} pin.

The pulse transformer must also have a minimum volt-second rating as required by the 79% duty cycle signal on PT^+/PT^- and the lowest frequency of operation. The required volt-seconds rating can be calculated from the minimum frequency as:

$$\text{Volt-Sec} = 0.33 \bullet \frac{V_{CC}}{f_{SW(MIN)}}$$

Since the pulse transformer is used for transmitting PWM information as well as bias power, choose a pulse transformer with a leakage inductance of 1µH or less. This reduces ringing and distortion of the PWM information so that a solid communication link is always maintained.

For low voltage (7V) mode on the LTC3766, transformers that meet the above requirements include the PA2008 from Pulse Engineering and the DA2320 from Coilcraft. For high voltage (8.5V) mode on the LTC3766, transformers that meet the above requirements include the PA3290 from Pulse Engineering.

The 1µF and 0.1µF capacitors in series with the pulse transformer of Figure 28 are for blocking and restoring the DC level of the signal. The 220pF/100Ω RC snubber shown at the IN^+/IN^- inputs of the LTC3765 is required to minimize ringing due to the leakage inductance of the pulse transformer. The values shown for each of these four components are appropriate in nearly all LTC3765/LTC3766 applications.

Voltage Loop Compensation

The voltage loop of the LTC3766 is compensated in much the same way as a standard buck converter, by placing a compensation network on the ITH pin. It is important to note, however, that the speed and stability of the voltage loop is heavily dependent upon several factors apart from the design of the ITH compensation. Common PCB layout errors, for example, often appear as stability problems. Examples include the distant placement of the input decoupling capacitor, connecting the ITH compensation to a ground track carrying significant switch current, and routing the FB signal over a long distance such that noise pick occurs. Refer to the PCB Checklist section for additional information. Another factor that affects the voltage loop is the choice of output capacitor. If the value is too low, or the ESR is too high, then it will not be possible to achieve optimum loop performance. A third factor that can impair loop response is the presence of underdamped resonances in the power stage. Examples include an underdamped LC input filter or an active clamp capacitor resonating with the main transformer magnetizing inductance. Refer to the Input Capacitor/Filter Selection and Active Clamp Capacitor sections for details on how to properly damp these LC resonances. Before attempting to optimize the loop response, carefully consider the above factors, because no amount of tweaking to the ITH components can cancel their effect. Also, any theoretical analysis of loop response only considers first order non-ideal component behavior. Consequently, it is important that a final stability check be made with production layout and components.

Stabilizing the voltage loop of the LTC3766 is accomplished by using the error amp to provide a gain from V_{OUT} to ITH that compensates for the control to output gain from ITH to V_{OUT}. The DC component of the ITH to V_{OUT} gain is approximately:

$$A_{DC1} = \frac{1}{29.3R_{SENSE}} \bullet \frac{2Lf_{SW}R_{OUT}}{2Lf_{SW} + R_{OUT}}$$

for resistor sense mode, and:

$$A_{DC1} = \frac{N_P}{2.2K_{CT}N_SR_{SENSE}} \bullet \frac{2Lf_{SW}R_{OUT}}{2Lf_{SW} + R_{OUT}}$$

for current transformer mode. Since the LTC3766 utilizes current mode control, the ITH to V_{OUT} transfer function can be basically characterized by one pole and one zero. The pole is given approximately by:

$$f_P = \frac{1}{2\pi R_{OUT}C} + \frac{1}{\pi f_{SW}LC}$$

and the zero is given by:

$$f_Z = \frac{1}{2\pi R_{ESR}C}$$

where R_{ESR} is the ESR of the output capacitance C. Note

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that the frequency of this zero will vary substantially depending on the type of capacitor chosen.

The LTC3766 uses internal slope compensation to stabilize the current loop. The amount of slope that is effectively seen at the current sense (I_S^+) input is:

$$S_R = Kf_{SW}(26mV)$$

for R_{SENSE} mode and:

$$S_R = Kf_{SW}(0.35V)$$

for current transformer mode, where K = 1 for duty cycles less than 50% and K = 2 for duty cycles greater than 50%. For most applications, this internal slope compensation will be on the order of the down slope of the inductor, which provides adequate current-loop stability without introducing excessive phase shift at the crossover frequency. For phase margin calculations, assume that two poles exist at one-half of the switching frequency. Use of an abnormally high valued inductor will produce additional phase shift due to slope compensation, thereby forcing a lower voltage loop crossover frequency to ensure stability. In order to avoid having either too little or too much slope compensation, make sure that the inductor satisfies the following inequalities:

$$\frac{V_{OUT}R_{SENSE}}{f_{SW}(78mV)} < L < \frac{V_{OUT}R_{SENSE}}{f_{SW}(17mV)}$$

for resistor sense mode and:

$$\frac{V_{OUT}R_{SENSE}K_{CT}N_S}{f_{SW}(1.06V)N_P} < L < \frac{V_{OUT}R_{SENSE}K_{CT}N_S}{f_{SW}(0.23V)N_P}$$

for current transformer mode.

In some cases, the LTC3766 and LTC3765 will be in delay phase-out mode at low input voltages. This cycle-by-cycle reduction of the PG and FG turn-on delays has the effect of reducing the amount of slope compensation by approximately 20% to 40%. Consequently, a higher value of inductance may be required to maintain current-loop stability during operation in delay phase-out mode.

The compensation network is typically configured as shown in Figure 29. The objective of this network is to add DC gain for excellent load regulation while providing good phase margin in the voltage loop at the highest possible crossover frequency. Normally this is achieved by adding a dominant pole at very low frequency and a zero well before the crossover frequency to remove most of the phase associated with the dominant pole. A high frequency pole is also added to reduce noise and provide attenuation of the output voltage ripple. Note that significant gain at the switching frequency in this compensation network can cause instabilities.

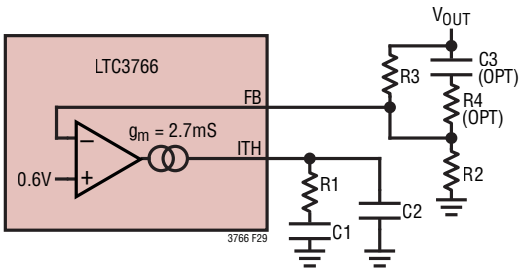

Figure 29. ITH Compensation Network

The network of Figure 29 has a DC gain of:

$$A_{DC2} = \frac{R2}{R2+R3} g_m R_{EA}$$

where R_{EA} = 5MΩ is the output resistance of the error amplifier and g_m = 2.7mS is the transconductance. The low frequency pole and zero are given by:

$$f_{P1} = \frac{1}{2\pi R_{EA} C1} \text{ and } f_{Z1} = \frac{1}{2\pi R1 C1}$$

where C1 >> C2, and the high frequency pole is given by:

$$f_{P2} = \frac{1}{2\pi R1 C2}$$

A good target for the 0dB crossover frequency of the voltage loop is between one-tenth and one-fifth of the switching frequency and a phase margin of 60° or more. Note that the zero produced by the ESR of the output capacitor helps to stabilize the loop by providing positive

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phase shift at frequencies near crossover. This tends to cancel the negative phase shift associated with the high frequency current loop poles. However, if the output capacitor is purely ceramic, the ESR zero may be at too high a frequency to contribute phase lead to the overall loop response. In this case, it can be helpful to add an optional phase lead capacitor C3 as shown in Figure 29, which generates a zero at a frequency of:

$$f_{Z2} = \frac{1}{2\pi R3C3}$$

This zero should be placed near the crossover frequency to provide additional phase boost. If C3 is used, it may also be necessary to add a resistor R4 in series with C3, where R4 << R3. This additional resistor prevents high-frequency switching noise from reaching the V_{FB} pin.

When optimizing the voltage loop, bear in mind that the large signal step response may be limited by factors other than the crossover frequency. At low input voltage, for example, the maximum duty cycle limit of 79% will impair the ability of the loop to respond to a sudden increase in load. Also, in responding to a very large load step (e.g., zero to full load) the loop may demand duty cycles that cause the main transformer to saturate. Hard saturation is prevented if current in sensed on the primary side or if the volt-second clamp is used, but the large signal step response will be limited by the available excess volt-seconds in the main transformer.

Setting the SG Reverse Overcurrent

The LTC3766 has been carefully designed to turn off the SG MOSFET as needed to prevent an overcurrent during start-up, shutdown and normal operation. Nevertheless, the LTC3766 also contains a user-adjustable SG reverse-over current protection circuit as an added protection feature. This feature is also useful in special applications where it may be advantageous to limit the SG reverse current to a particular value. SG reverse overcurrent is implemented by monitoring the voltage on the SW pin when SG is high, and terminating the SG on-time for the duration of the switching cycle if the SW voltage exceeds an internal threshold. If the LTC3766 is operating at zero duty cycle when the SG overcurrent occurs, then the FG MOSFET is forced on prior to SG turn-off to re-route current to the primary and prevent avalanche from occurring. If not adjusted, the internal SG overcurrent threshold has been set high enough so that it should not interfere with the operation of normal applications. **Be careful to make Kelvin connections from SW and GND to the drain and source of the SG MOSFET.**

In addition to a fixed internal threshold on the SW pin, a current is sourced from the SW pin so that a resistor can be added to decrease the overcurrent threshold if desired. Both the SW pin threshold and the adjust current are changed depending on whether the LTC3766 is operating in HV or LV mode, so as to account for the higher on-resistance of high voltage MOSFETs. In applications where the SW node plateau voltage is 40V or less ($V_{IN} \bullet N_S/N_P \leq 40$), a single resistor can be used to set the SG overcurrent threshold (Figure 30). The resulting overcurrent V_{DS} on the SG MOSFET is given by:

$$V_{OC} = V_{REV} - I_{REV}R_{SW}$$

The SG overcurrent trip should normally be targeted at twice the maximum V_{DS} of the SG MOSFET during normal operation. This can be estimated using:

$$V_{OC} = \frac{R_{DS(MAX)}V_{OUT}}{f_{SW}L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \bullet \frac{N_P}{N_S}\right)$$

where $R_{DS(MAX)}$ is the maximum $R_{DS(ON)}$ of the SG MOSFET over temperature. This equation allows for twice the reverse SG current that would normally occur due to the

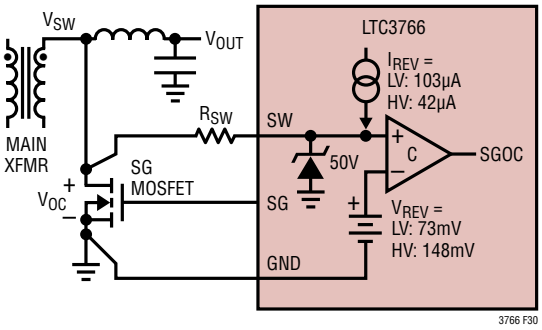

Figure 30. SG Overcurrent for Low V_{OUT} Applications

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inductor current ripple at no load. The % error in the SG overcurrent trip can be estimated using:

$$\Delta V_{OC} = \frac{100}{V_{OC}} \sqrt{\left(\frac{I_{REV} R_{SW}}{6}\right)^2 + \left(\frac{V_{REV}}{14}\right)^2}$$

If the above error is greater than 30%, then the V_{OC} threshold may need to be increased accordingly. To ensure that the inductor doesn't saturate prior to the SG overcurrent trip, the inductor should have a saturation current such that:

$$I_{LSAT} > \frac{V_{OC(MAX)}}{R_{DS(MIN)}}$$

where $V_{OC(MAX)}$ is the maximum overcurrent trip based on the above error and $R_{DS(MIN)}$ is the minimum $R_{DS(ON)}$ of the SG MOSFET over temperature.

While the circuit of Figure 30 can be used whenever the SW node plateau voltage is 40V or less, care must be taken to limit the current into the 50V clamp on the SW pin due to overshoot and ringing. Figure 31 illustrates a typical SW node waveform.

The overshoot and ringing on the SW node is due to the leakage inductance of main transformer, and it is worse at full load and maximum V_{IN}. The peak SW node voltage ($V_{SW(PK)}$) also depends heavily on the gate drive timing as well as the RC snubber that is typically used on the SW node. See Delay Resistor Selection: PG Turn-On Transition and RC Snubber sections for details. Make sure that the peak SW node voltage does not cause more than 0.2A to flow into the SW pin:

$$\frac{V_{SW(PK)} - 50V}{R_{SW}} < 0.2A$$

The above condition is normally satisfied with reasonable values for R_{SW} and the use of an RC snubber to limit $V_{SW(PK)}$.

In applications where the SW node plateau voltage is greater than 40V, it is necessary to add a divider as shown in Figure 32.

For the circuit of Figure 32, the overcurrent V_{DS} on the SG MOSFET is given by:

$$V_{OC} = V_{REV}\left(\frac{R1+R2}{R2}\right) - I_{REV}\left[R1+R3\left(\frac{R1+R2}{R2}\right)\right]$$

In addition to producing the desired V_{OC} threshold, there are three constraints on the selection of resistors R1, R2 and R3 that must be simultaneously met: 1) R1 and R2

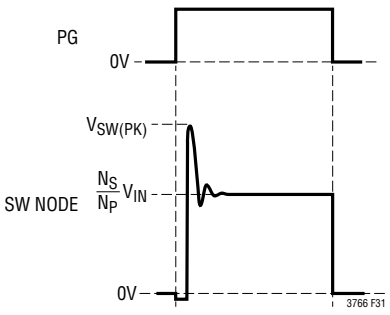

Figure 31. Typical SW Node Waveform

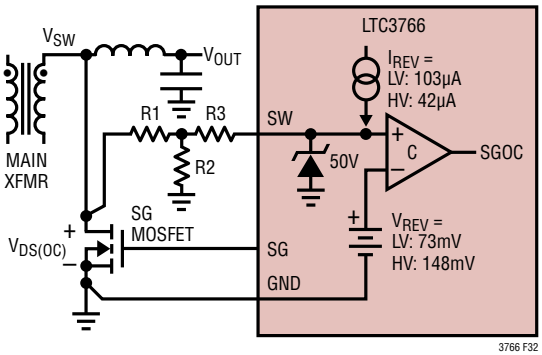

Figure 32. SG Overcurrent for High V_{OUT} Applications

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must divide the maximum V_{SW} plateau voltage down to 40V or less, 2) the impedance at the SW pin must be kept as low as possible to reduce the delay in sensing the V_{SW} voltage, and 3) the power dissipation in R1 and R2 must be kept reasonably low. The last two constraints can be met by choosing a maximum power (P_R) to be dissipated in the sum of R1 and R2. Typically, setting P_R = 0.25W is a reasonable compromise that keeps the time constant low while not greatly impacting converter efficiency.

The selection of R1, R2 and R3 is made using the following procedure:

1. Calculate R1 and R2 based on a maximum power (P_R = 0.25W) and a divider ratio that will produce exactly 40V maximum on the SW pin:

$$R1 = \frac{N_S}{N_P}\left(\frac{V_{OUT}V_{IN(MAX)}}{P_R}\right) - \frac{40V_{OUT}}{P_R}$$

$$R2 = \frac{40 \bullet R1}{\frac{N_S}{N_P}V_{IN} - 40}$$

2. If the value for V_{OC} calculated using R1 and R2 from step 1) is greater than the target V_{OC} value, then choose R3 such that I_{REV} • R3(R1+ R2)/R2 equals the difference between the calculated and target V_{OC} values.

3. If the value for V_{OC} calculated using R1 and R2 from step 1) is less than the target value, then R3 = 0. Recalculate R1 and R2 based on maximum power (P_R = 0.25W) and the desired target V_{OC} value:

$$R1 = \frac{BI_{REV} - AV_{OC} + \sqrt{\left(AV_{OC} + BI_{REV}\right)^2 - 4ABV_{REV}I_{REV}}}{2AI_{REV}}$$

$$R2 = \frac{B - AR1}{A}$$

where A = $P_R(N_P/N_S)$ and B = $V_{OUT}V_{IN(MAX)}$.

For the circuit of Figure 32, the % error in the SG overcurrent trip can be estimated using:

$$\Delta V_{OC} = \frac{100}{V_{OC}}\sqrt{\left(\frac{I_{REV}(R1+K \bullet R3)}{6}\right)^2 + \left[K\frac{V_{REV}}{14}\right]^2}$$

where K = (R1 + R2)/R2.

When using resistors to set the SG overcurrent threshold or to limit the SW pin voltage, be careful to maintain a fast rise and fall time at the SW pin to avoid a Communication Lock Fault on the LTC3766. Note that the SW pin must fall below 0.5V within 150ns of PT^+ falling. In some cases, a small capacitor (5pF – 15pF) may be needed between V_{SW} and the SW pin in Figure 30 or Figure 32 to achieve a fast fall time.

RC Snubbers

Most applications will make use of an RC snubber to reduce the overshoot and ringing on the SW and SWB pins, as shown in Figure 33. The snubber capacitor is chosen to limit the peak voltage overshoot on SW or SWB by absorbing the energy in the leakage inductance of the main transformer. The snubber resistor is then chosen to provide optimum damping so as to minimize ringing. A larger snubber capacitor reduces the overshoot, but at the expense of increased power dissipation in the snubber resistor. In general, the snubber on the SWB node has far less energy to absorb and can therefore be smaller than that on the SW node. In some cases, the snubber on SWB can be eliminated entirely.

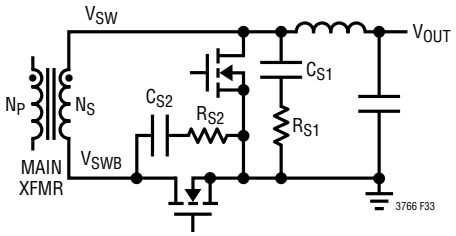

Figure 33. Using RC Snubbers

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The precise values needed for the RC snubbers will depend upon the specifics of each application, and should be optimized in the lab. Typical values for C_{S1} and C_{S2} range from 1nF to 4.7nF, and R_{S1} and R_{S2} are typically 1Ω to 50Ω. Always use a high quality ceramic (X7R) capacitor and resistors with a high power rating (1/4W to 1/2W) for and an RC snubber.

Remote Sensing

The LTC3766 contains a precision differential amplifier for use in remote sensing applications. As shown in Figure 14a, this is useful in eliminating the voltage drops associated with bussing the power supply output voltage to a remote load. Be aware that the differential amplifier is powered from the V_{IN} pin of the LTC3766, and requires 1.5V of overhead on V_{IN} above the output voltage (V_{SOUT}). If the voltage on the V_{IN} pin is not adequate to support the V_{SOUT} voltage, the LTC3766 will generate a fault. This is necessary to avoid a potential overvoltage on the main output of the converter. In addition, the LTC3766 will generate a fault if the polarity of the V_S^+ and V_S^- pins are reversed by approximately 0.3V or more.

In rare applications, it may be useful to raise the common mode voltage of the V_S^+ and V_S^- inputs. When doing so, always ensure that $V_S^+ < 2(V_{IN} – 2V)$ to prevent saturating the input stage of the differential amplifier. If the input stage is saturated, the LTC3766 forces the V_{SOUT} pin to 0V. In applications where the differential amplifier is not needed, connect the inputs as shown in either Figure 14b or Figure 15.

Self-Starting PolyPhase Applications

Figure 34 shows the PolyPhase connections for the LTC3765 and LTC3766. On the primary side, the design of one phase of the LTC3765 can be optimized and then replicated up to four times by simply tying the SSFLT pins together. The common SSFLT pins are held low until all

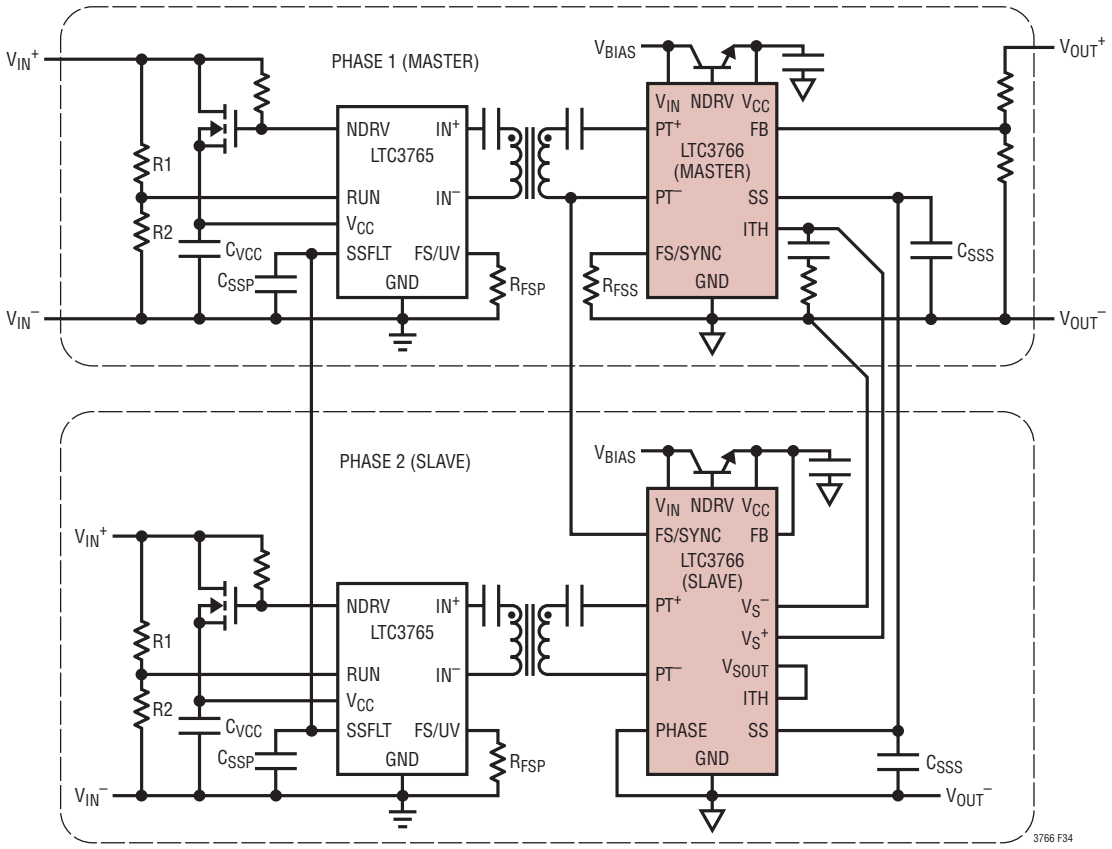

Figure 34. PolyPhase Connections

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phases have adequate voltage on their V_{CC} supplies and RUN pins. This prevents any of the phases from switching until every phase has satisfied the requirements for start-up. When start-up conditions have been met, the SSFLT pin is released and quickly charged until all phases have switched once. The SSFLT pin currents then decrease to their nominal values. This ensures that all phases begin their asynchronous, open-loop start-up at nearly the same time.

On the secondary side, the SS pins from all phases are interconnected as well. This prevents any one phase from starting until all phases have adequate bias voltage and have detected switching on their respective SW pins. Once this condition is met, the master will advance the soft-start voltage to match the V_{OUT} of the converter, and switching begins on the secondary side on all phases. After a brief lock sequence, all phases will transfer control to the secondary. The ITH pins are interconnected between the phases so that current is shared evenly between the master (which controls the ITH pin to regulate V_{OUT}) and the slaves.

The LTC3765 SSFLT connection is also used to communicate faults. If one phase has a primary-side fault (undervoltage, overcurrent, overtemperature, or communication loss), it immediately stops switching and rapidly pulls SSFLT to 6V. The other phases will detect that SSFLT is above 5V and will also stop switching. On the secondary side, the LTC3766s detect that switching has stopped and also fault, which is communicated to all phases through the common SS connection. The voltage on the primary-side SSFLT node then slowly decreases and a restart begins. Likewise, if a fault originates on the secondary side on a give phase, this fault is communicated to the other LTC3766s so that all phases stop switching. This will cause a communication fault on the primary side followed by a restart attempt.

For the LTC3765 on the primary side, choose components based on a single-phase design. Duplicate the single phase to the desired number of phases, up to the maximum of four, with the following modifications:

1. Connect the SSFLT pins together. Instead of having multiple capacitors from the SSFLT node to ground, the capacitors can be consolidated into one capacitor with a value equal to $N \bullet C_{SSFLT}$, where N is the number of phases.
2. If desired, the phases can share the linear regulator of one phase by shorting their V_{CC} and NDRV pins to the linear regulator output; however, be aware that the linear regulator pass device will be dissipating more power and may require a larger and more thermally conductive package. The design and PCB layout are generally simplified if each phase uses its own linear regulator.

The secondary side follows a similar procedure; however, there is more differentiation between the master phase and the slave phases. For the master, choose components based on the above design equations. Be aware that each phase should have its own linear regulator pass device to distribute the power dissipation. Duplicate the components for each slave, with the following exceptions:

1. Connect all of the SS pins together. Instead of having multiple capacitors from the SS node to ground, the capacitors can be consolidated into one capacitor. Note that only the master charges and discharges the soft-start capacitor.
2. Connect the FB pin of the slaves to V_{CC}. This connection puts the LTC3766 into slave mode. In this mode, the ITH pin becomes a high impedance input and the SS pin is only used for fault communication. An LTC3766 slave will not perform a pre-set of the soft-start capacitor, nor will it charge or discharge it. A slave can only force the SS pin high to indicate a fault, and it also monitors the SS pin to respond to a fault in another phase.

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3. For each slave, the integrated unity-gain differential amplifier is used to sense the voltage on the ITH pin of the master. Connect the V_S^+/V_S^- inputs of each slave between the ITH and signal GND pins of the master. Connect the V_{SOUT} pin on each slave to its own ITH pin.
4. Connect the FS/SYNC pins of each slave to the PT^- pin of the master. The PT^- pin of the master contains the clock signal used to synchronize the slaves and master together.

For each slave, set the relative phase using the PHASE pin. Note that ripple current in the input capacitor is minimized by operating the controllers out of phase. For a 2-phase system, set the slave at 180°. For a 3-phase system, set the slaves at 120° and 240°. For a 4-phase system, set the slaves at 90°, 180°, and 270°. Refer to Setting the Switching Frequency and Synchronization for details on setting the PHASE pin.

Volt-Second Clamp

When used in applications with the LTC3765, Direct Flux Limit will guarantee that no saturation occurs on the main transformer. Consequently, there is no need to use a volt-second clamp in applications that have the Direct Flux Limit feature. In applications where the LTC3766 is used standalone, however, the volt-second clamp can be used as a failsafe to prevent excessive volt-seconds from being applied to the main transformer during the PWM on-time. Figure 35 illustrates the use of the volt-second clamp. As shown in Figure 35, the SW voltage is used to monitor the voltage applied to the main transformer. During the PWM on-time, the C_{VS} capacitor is charged by the SW node through the R_{VS} resistor.

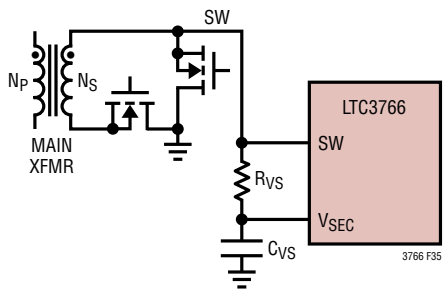

Figure 35. Using the Volt-Second Clamp

The PWM on-time is terminated when a pre-determined threshold is reached. This will limit the applied volt-second product to:

$$(V \bullet S)_{LIM} = 0.605 R_{VS} C_{VS}$$

The above equation is accurate even when the peak voltage on the SW node is relatively low and the charging is nonlinear, such as in low V_{OUT} applications. This is possible because the LTC3766 senses the voltage on the SW pin and adjusts the internal volt-second comparator reference so that constant volt-seconds are maintained regardless of the voltage on SW. Consequently, it is important that the LTC3766 SW pin be connected to the secondary SW node for proper sensing of this voltage to occur.

The volt-second limit should normally be set approximately 10% above the operational volt-second requirement. To accomplish this, calculate R_{VS} using:

$$R_{VS} = 1.10 \frac{V_{OUT}}{0.605 f_{SW} C_{VS}}$$

For capacitor C_{VS}, use a 5% or better NPO-type ceramic capacitor, since accuracy is important. Typically a value of 1nF is suitable. Likewise, use a 1% resistor for R_{VS}.

In high output voltage applications where the SW node must be divided down, use the circuit of Figure 36 to set the volt-second clamp.

In this case, assuming $R_{VS} >> R1||R2$, R_{VS} can be calculated using:

$$R_{VS} = 1.10 \frac{V_{OUT}}{0.605 f_{SW} C_{VS}} \left(\frac{R2}{R1+R2} \right)$$

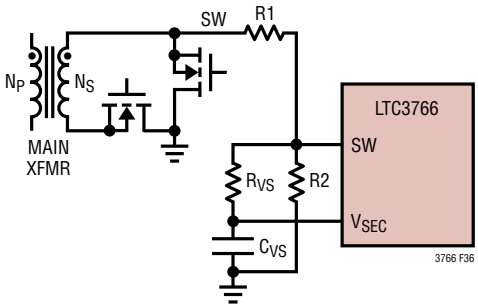

Figure 36. Volt-Second Clamp in High V_{OUT} Application

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APPLICATIONS INFORMATION

Nonisolated Applications

In addition to being used with the LTC3765 in isolated applications, the LTC3766 can also be used standalone to make a nonisolated resonant-reset forward converter as shown in Figure 37. In this application, the primary-side MOSFET is driven directly by the PT^+ pin, and the MODE pin is tied to GND through either a 100k or 50k resistor to select LV or HV operating mode.

The bias for the V_{IN} pin is normally taken directly from the input voltage of the converter. The LTC3766 contains a current-limited internal 30V shunt to simplify applications where V_{IN} > 30V. In such applications, place a current limiting resistor in series with the V_{IN} pin calculated using:

$$R_{VIN} = \frac{V_{IN(MAX)} - 30V}{3.5mA}$$

Note that at low V_{IN}, there will be a maximum drop across R_{VIN} equal to (1.2mA) • (R_{VIN}) that is due to the V_{IN} pin operating current. For proper operation, the voltage on the V_{IN} pin at low input voltage must be greater than the rising V_{CC} UVLO by at least the threshold voltage of Q_P.

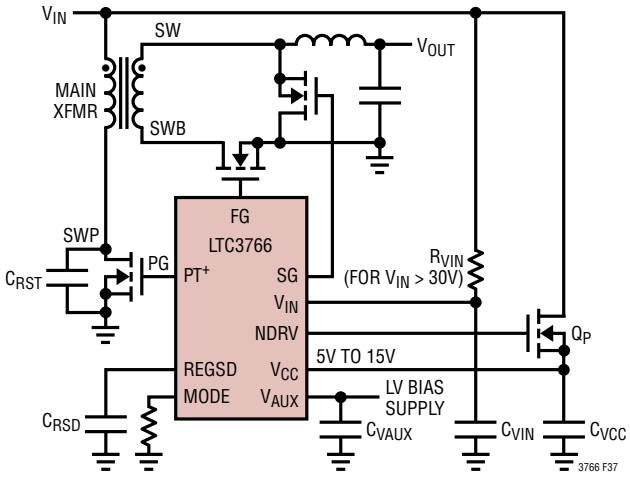

Figure 37. Nonisolated Resonant-Reset Application

Using a MOSFET for Q_P instead of an NPN eliminates the base current that would otherwise add to the V_{IN} operating current. If more margin is needed at low V_{IN} operation, a Darlington transistor is another option for Q_P.

To reduce power dissipation in Q_P, a low voltage bias supply should be fed into the V_{AUX} pin to power the bypass LDO. This bias supply can be generated off of either the primary or secondary of the main transformer using an auxiliary buck or an inductor overwinding supply. During an output overload condition, the low voltage bias supply will collapse, causing the high voltage linear regulator controller to be re-energized. To prevent excessive power dissipation under this condition, place a capacitor on the REGSD pin to limit the operating time of the high voltage linear regulator.

The RUN pin can be used as an undervoltage lockout (UVLO) on the converter input voltage. Direct RUN/STOP control can be achieved by using a small NMOS on the RUN pin as shown in Figure 38.

The resonant reset capacitor, C_{RST}, serves to generate a voltage on the SWP node during the off-time of the primary MOSFET that resets the transformer flux on a cycle-by-cycle basis. This capacitor is normally sized so that the SWP voltage exactly resonates back to V_{IN} at the end of the off time with minimum V_{IN}:

$$C_{RST} \approx \frac{1}{L_M}\left[\frac{1}{\pi f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN(MIN)}}\frac{N_P}{N_S}\right)\right]^2 - C_{PAR}$$

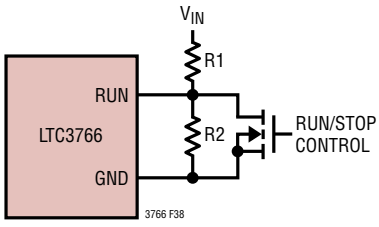

Figure 38. RUN/STOP Control for Standalone Applications

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APPLICATIONS INFORMATION

where L_M is the main transformer magnetizing inductance and C_{PAR} is the total parasitic capacitance on SWP:

$$C_{PAR} = C_{OSS(PG)} + \left(\frac{N_S}{N_P}\right)^2 \left(C_{OSS(FG)} + C_{SNUB}\right)$$

C_{PAR} includes the drain capacitance of both the PG and FG MOSFETs as well as any snubber capacitance on the SWB node. In reality, the presence of leakage inductance makes the SWP node rise much faster than it otherwise would. As a result, the optimum value for C_{RST} can be 40% to 60% higher than that calculated by the above equation. The steady-state peak voltage on the primary and forward MOSFETs is given by:

$$V_{DS(PG)} = V_{IN(MAX)} + \frac{V_{OUT}}{2f_{SW}} \frac{N_P}{N_S} \sqrt{\frac{1}{L_M\left(C_{RST} + C_{PAR}\right)}}$$

$$V_{DS(FG)} = \frac{V_{OUT}}{2f_{SW}} \sqrt{\frac{1}{L_M\left(C_{RST} + C_{PAR}\right)}}$$

If a larger value of C_{RST} is used, the peak voltage stresses can be decreased, possibly allowing the use of a MOSFET with lower BV_{DSS} rating. However, with a larger C_{RST} the SWP voltage at low V_{IN} will not have time to resonate back down to V_{IN}, thereby increasing the turn-on switching losses. In practice, some truncation of the low V_{IN} reset waveform is often tolerated to maximize the overall efficiency of the converter. Note also that the peak MOSFET voltage stress during transients can be considerably higher, so allow at least 30% margin above these calculated voltages. The volt-second clamp can be used to reduce the peak voltage stress due to load transients.

The setting of the gate drive timing for a resonant reset converter is simplified by the adaptive delays featured in the LTC3766. When standalone mode is active (100k or 50k on MODE), the FGD pin is ignored, and the associated dead time between SG turn-off and PG turn-on is controlled adaptively. In this mode, LTC3766 delays the PG turn-on until after the SG pin has fallen below approximately 0.5V. For the PG turn-off transition, the SGD resistor is chosen to minimize the dead time and also prevent collapse of the SWP node (i.e., catch the SWP voltage at its peak if possible). Note that setting the FG turn-off so as to catch the SWP voltage near its peak will improve efficiency and allow for the use of a larger resonant reset capacitor, thereby reducing the peak voltage stresses on the MOSFETs. Adaptive delay limiting on this edge ensures that SG will not go high until SW has fallen, so shoot-through is not a concern.

In nonisolated applications, the inductor current is normally sensed on the input side of the power transformer, typically using a sense resistor. Note that in this situation, the values for the sense resistor (R_{SENSE}) and the I_{PK} resistor (R_{IPK}) should be calculated using the above equations, but then scaled by a factor of NP/NS. For applications where the transformer is configured to step up the voltage, however, it may be more efficient to sense current on the output side of the power transformer. In this case, be careful to avoid transformer saturation by keeping the resonant reset capacitor as small as possible and making use of the volt-second clamp.

Common Mode Noise

Common mode noise arises in isolated converter applications due to the parasitic capacitance between the primary and secondary windings of the main transformer. When rapid voltage changes occur on the primary-side MOSFET drain, this will inject current through the inter-winding capacitance. This causes the ground reference of the secondary to suddenly jump with respect to the primary ground. As a result, current is injected across the inter-winding capacitance of the pulse transformer back to the primary, and a resulting common mode voltage can appear at the IN^+ and IN^- inputs of the LTC3765. While the LTC3765 has been carefully designed to reject this common mode voltage, always use a common mode filter capacitor that is directly connected between the primary and secondary grounds. This capacitor shunts away the common mode noise. Typically, a value of 2.2nF is adequate. Use a high quality ceramic Y capacitor rated for 250VAC operation, or other voltage rating as needed for the isolation and safety requirements of the particular application.

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APPLICATIONS INFORMATION

Thermal Considerations

When designing a forward converter with an output power of 50W or more, particular attention must be paid to the thermal aspects of the design and layout. In general, it is better to use multiple elements in parallel to spread out the power dissipation and reduce temperature rise. Beneath all power MOSFETs, use thermal vias and copper islands on multiple layers to provide cooling. If excessive temperature rise occurs, both the LTC3765 and the LTC3766 contain overtemperature shutdown circuits that will help to prevent thermal damage. Both overtemperature shutdowns are set at approximately 165°C rising with 20°C of hysteresis.

PCB Checklist

The LTC3766 requires proper bypassing on the V_{CC} supply due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing and undershoot/overshoot.

To obtain optimum performance from the LTC3766:

1. Use a low inductance, low impedance ground planes to reduce any ground drop and stray capacitance. Remember that the LTC3766 switches at greater than 2A peak currents and the power MOSFETs can carry 50A or more. Any significant ground drop will degrade signal integrity.
2. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain three separate planes if possible: signal ground (GND pin), power ground (PGND pin) and power stage ground. The power ground plane should be connected with a single via to the source of the SG MOSFET. The signal ground plane should be connected with a single via to the source of the SG MOSFET for accurate V_{DS} sensing. If resistor current sensing is used for I_S^+ and I_S^-, be careful to minimize the inductance of the plane between the sense resistor and the source of the SG MOSFET.
3. Mount a bypass capacitor as close as possible between the V_{CC} pin and the power ground plane.
4. Keep the copper traces between the driver output pins and the MOSFET short and wide.
5. Keep the high current switching path on both the primary and secondary as short as possible, using multiple layers in parallel to further reduce parasitic inductance.
6. If resistor sense mode is used, the I_S^+ and I_S^- pins must be Kelvin connected to the sense resistor. The traces to the sense resistor must run side-by-side and be shielded with signal ground on all sides.
7. Keep the switching nodes (SW, PT^+, PT^-, FG, SG) away from noise sensitive nodes, especially FB, ITH, I_S^+ and I_S^-.
8. The voltage divider on the output should be connected as close as possible to the load at the output terminal of the power supply. The bottom of the voltage divider should be tied to the signal ground plane. Use the differential amplifier to sense the load voltage and eliminate distribution voltage drops.

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TYPICAL APPLICATIONS

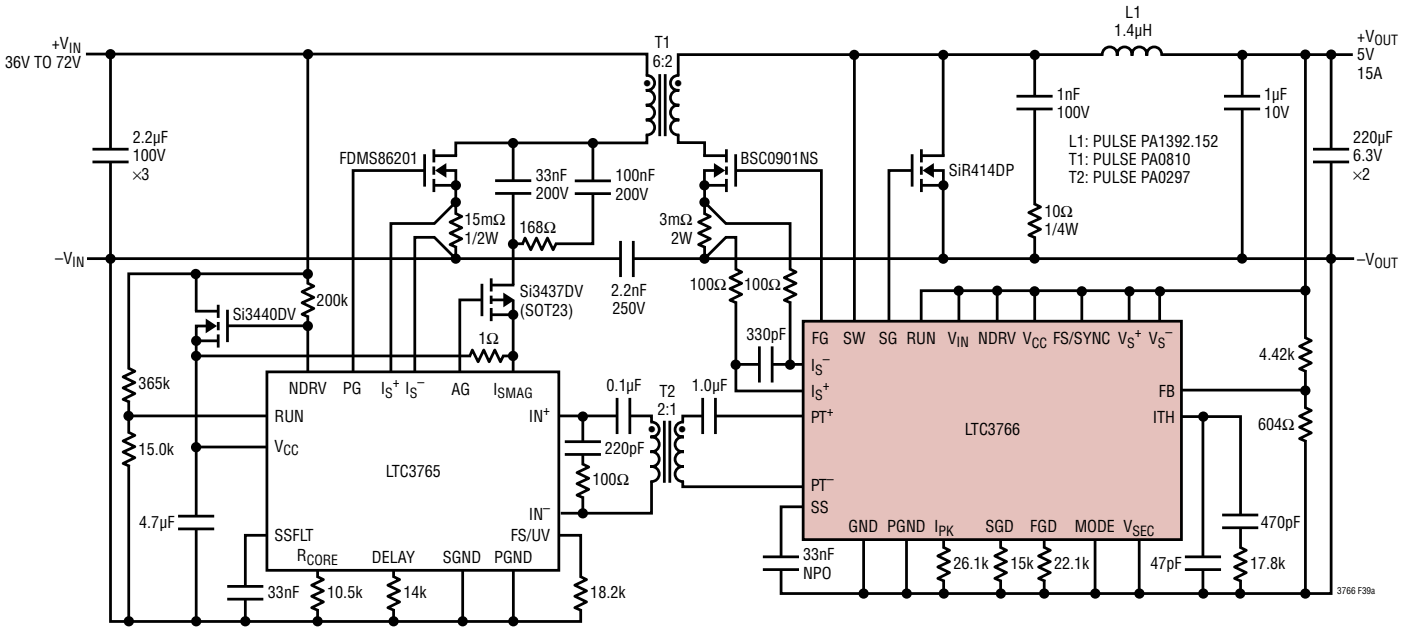
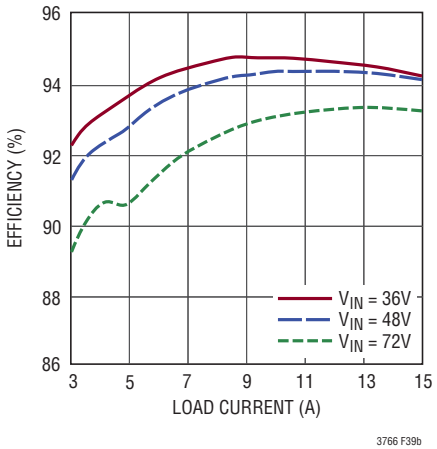
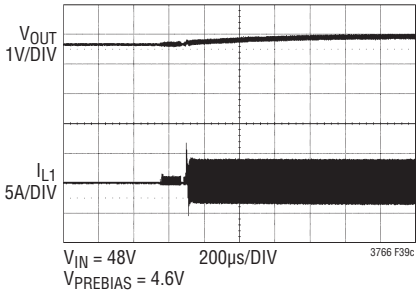


Figure 39. 36V – 72V to 5V/15A Active Clamp Isolated Forward Converter

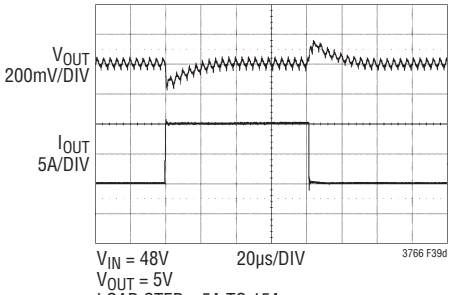
Efficiency vs Load Current



Pre-Biased Start-Up



Load Step



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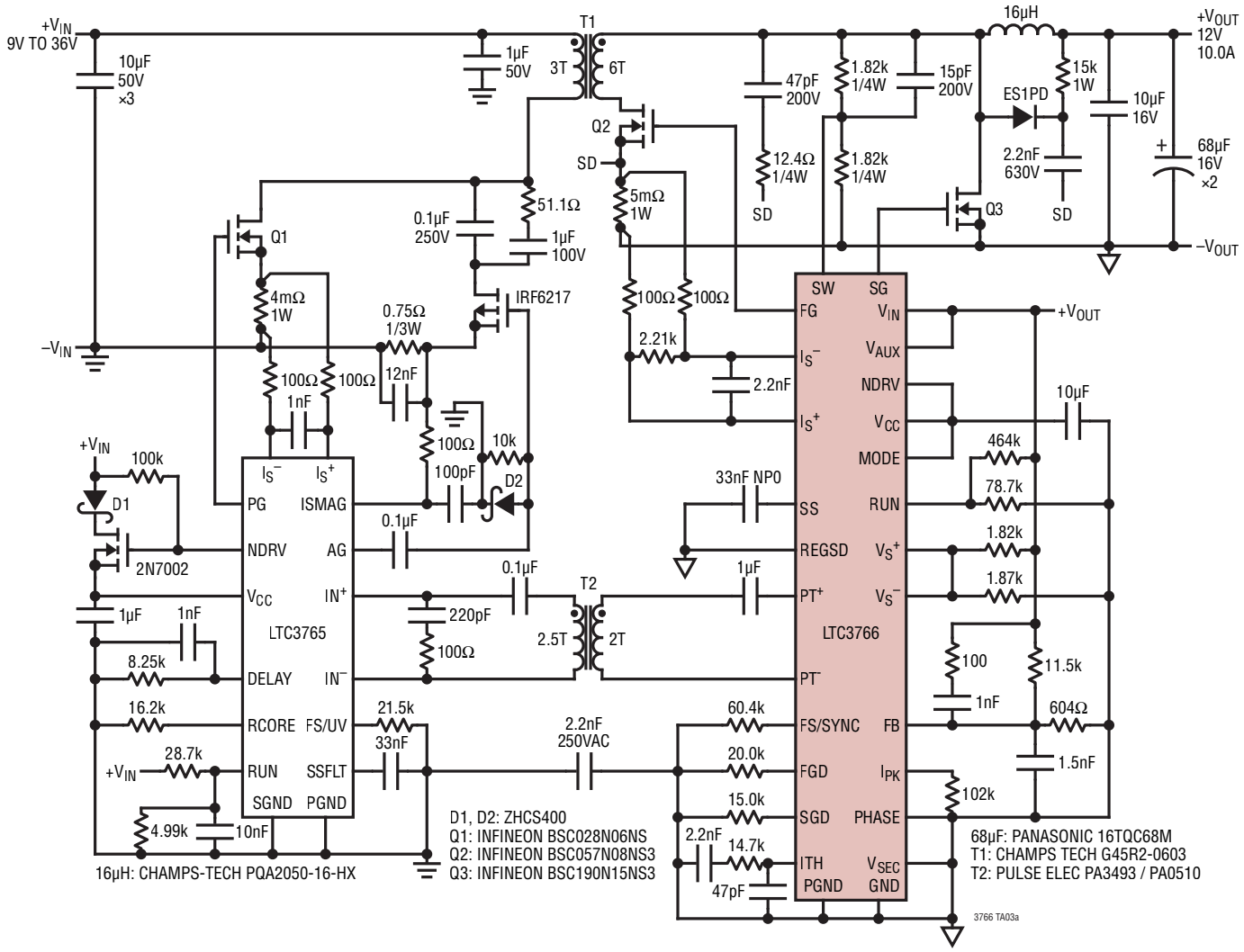
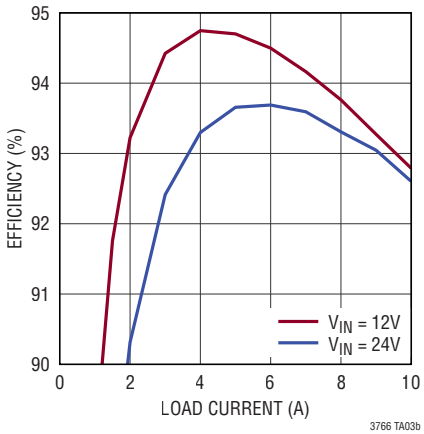
TYPICAL APPLICATIONS

9V – 36V to 12V/10A Active Clamp Forward Converter



Efficiency vs Load Current



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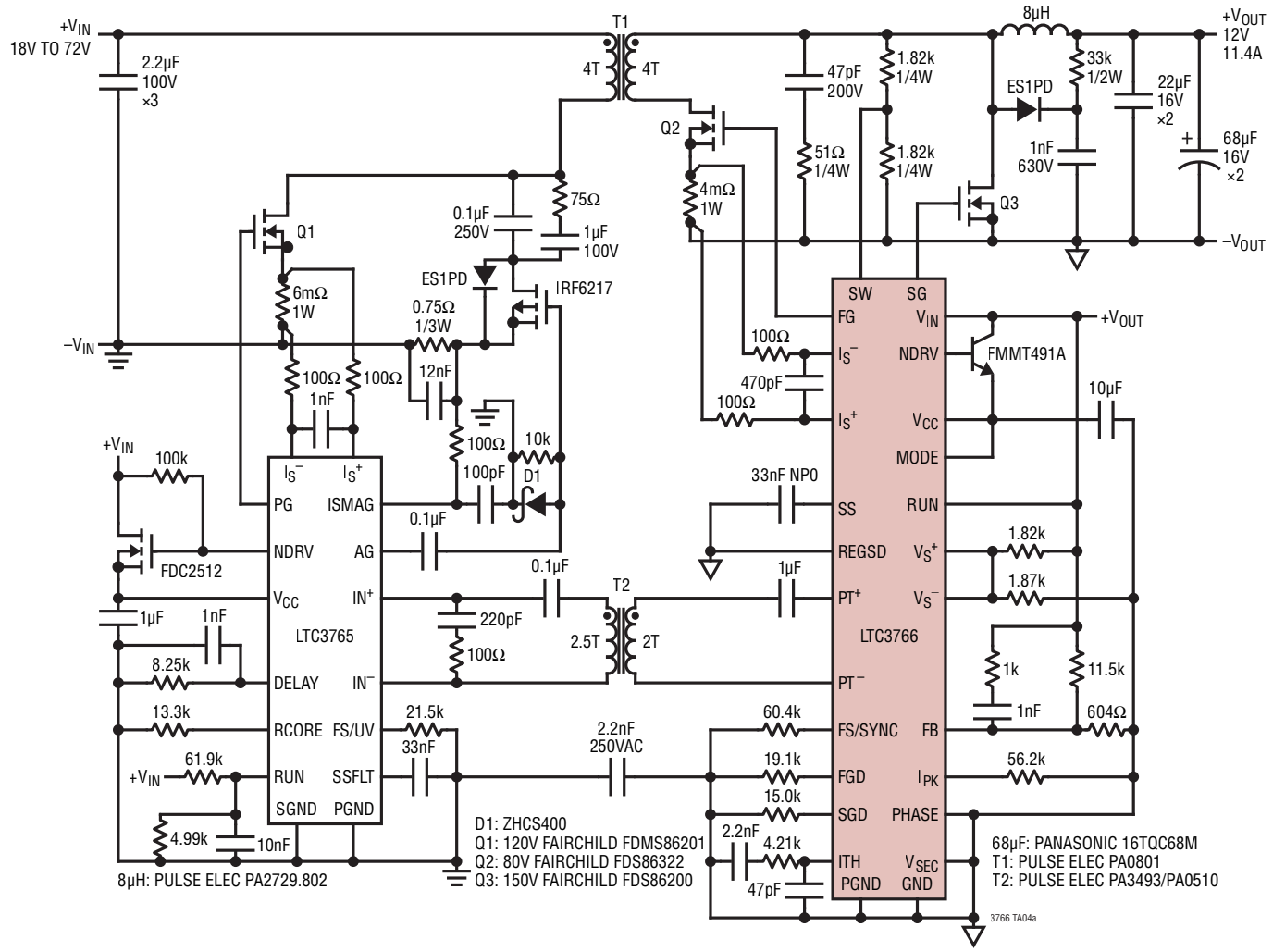
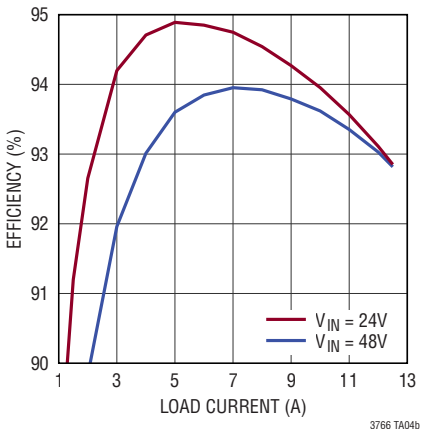
TYPICAL APPLICATIONS

18V – 72V to 12V/11.4A Active Clamp Forward Converter



Efficiency vs Load Current



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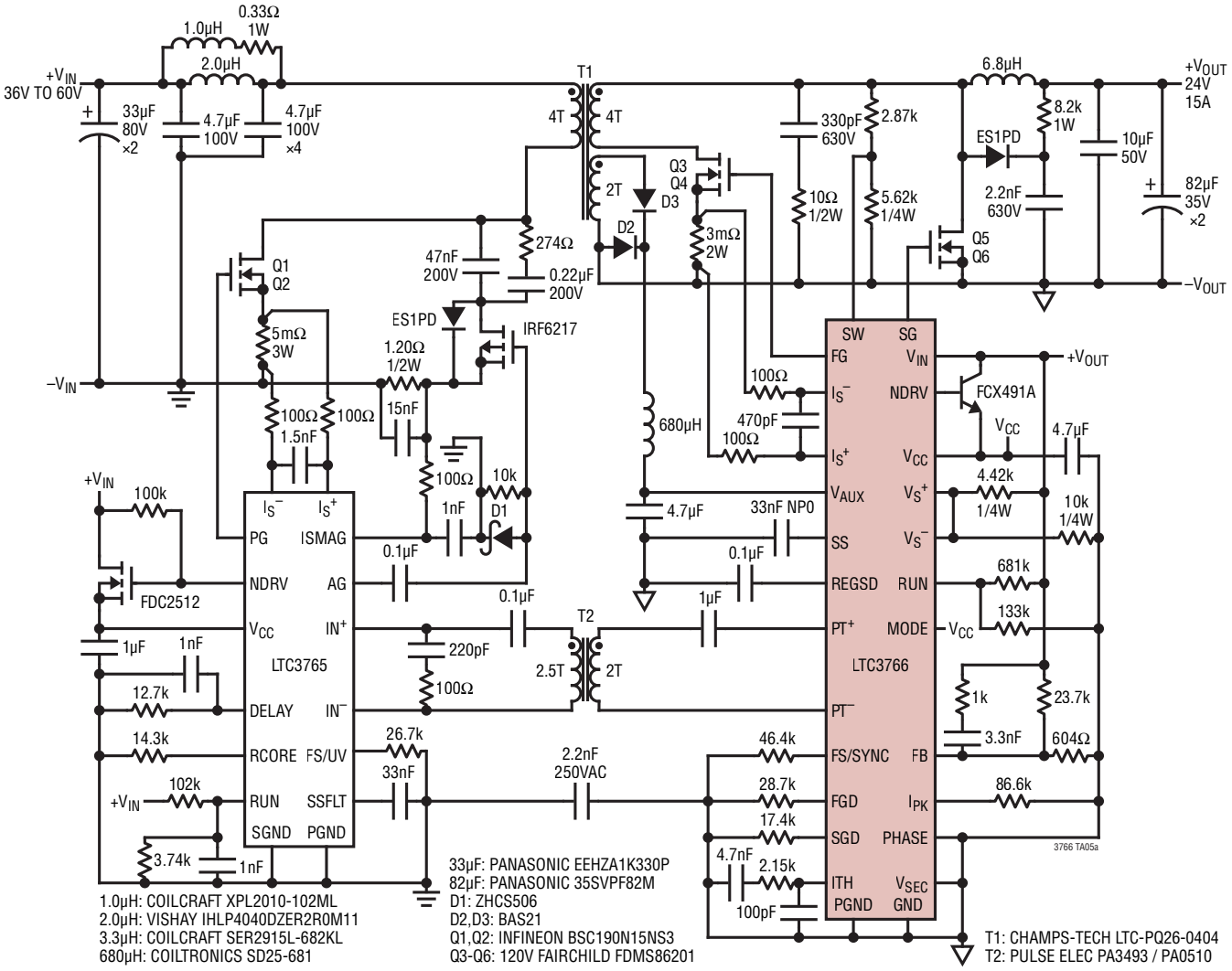
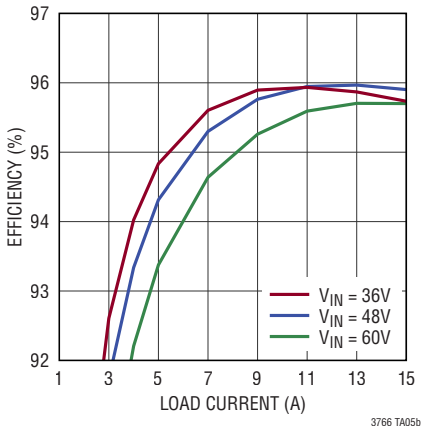
TYPICAL APPLICATIONS

36V-60V to 32V at 10A 320W Isolated P/A Power Supply



Efficiency vs Load Current



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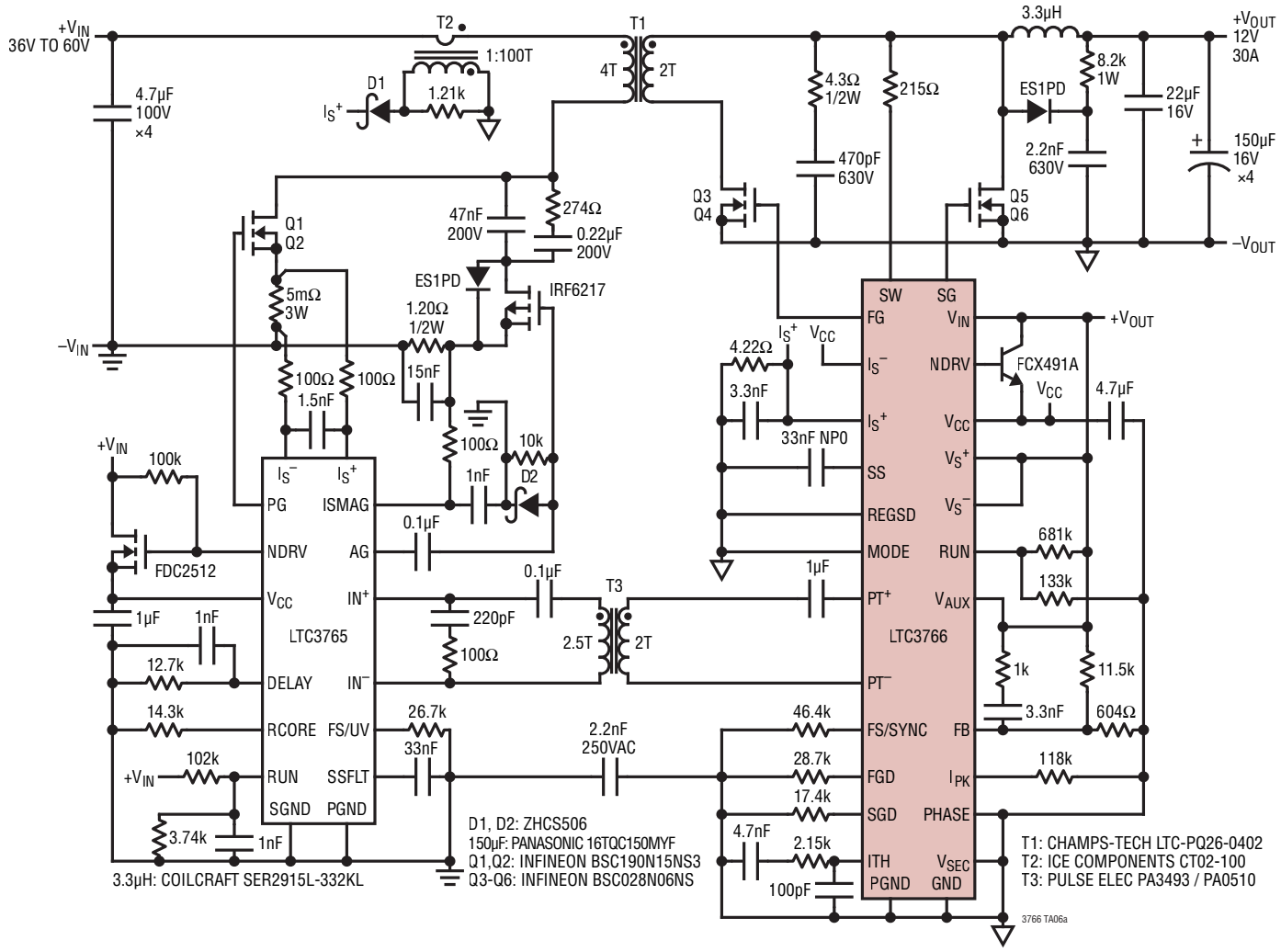
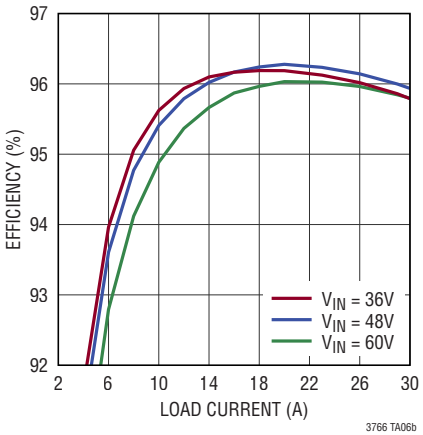
TYPICAL APPLICATIONS

36V – 60V to 14V at 25A 350W Isolated Bus Converter



Efficiency vs Load Current



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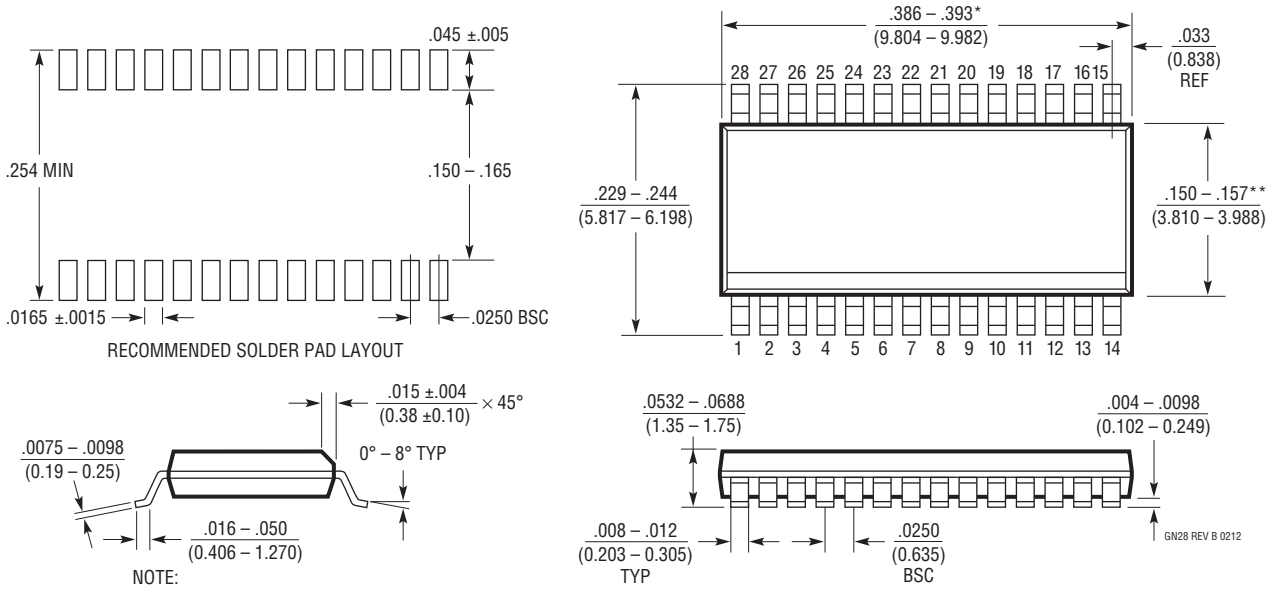
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3766#packaging for the most recent package drawings.

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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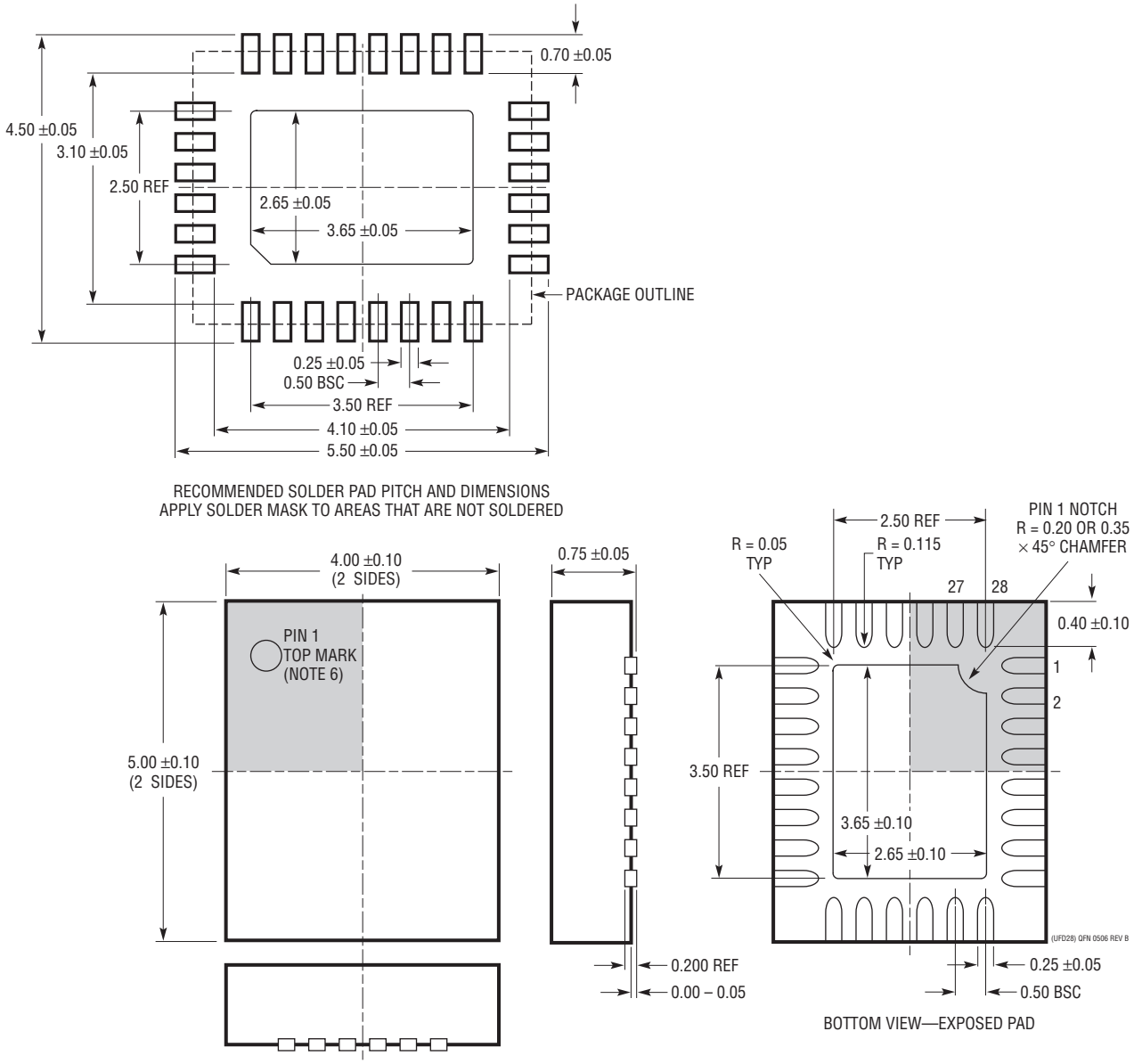
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3766#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/13	Switch polarity between I_S^+ and I_S^- in Figure 11	28
B	6/16	Modified FB, V_{SOUT}, V_S^+ and V_S^- pin descriptions Updated Figure 6 Revised schematics	8 20 55, 56, 57, 58
C	9/16	Clarified Selecting the Main Transformer section	21

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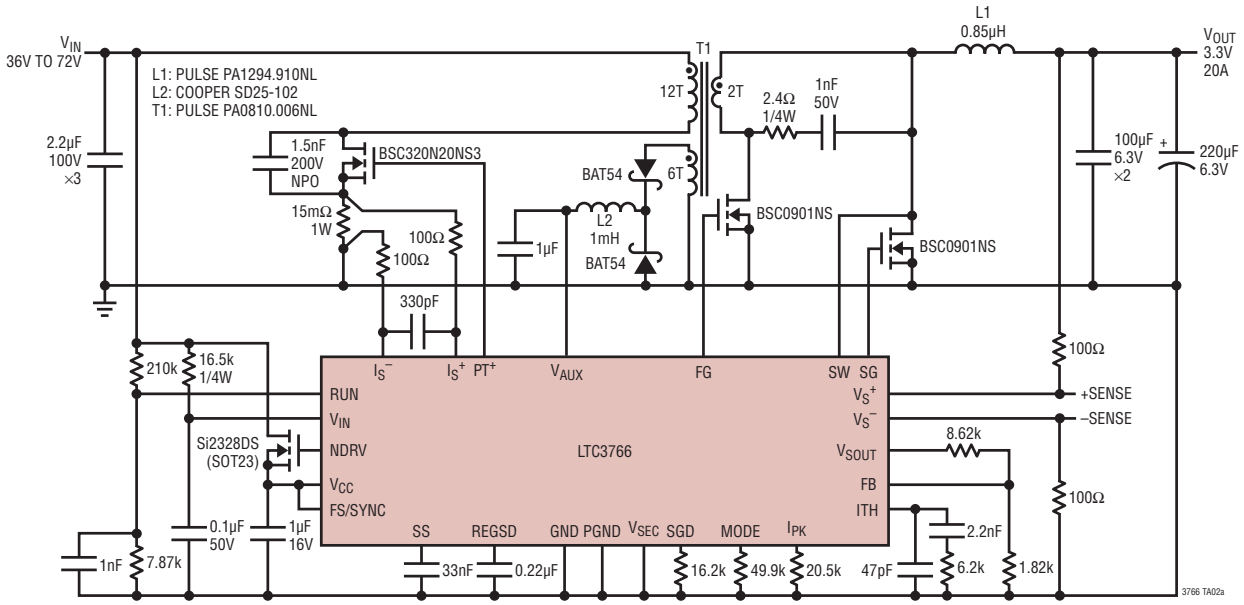
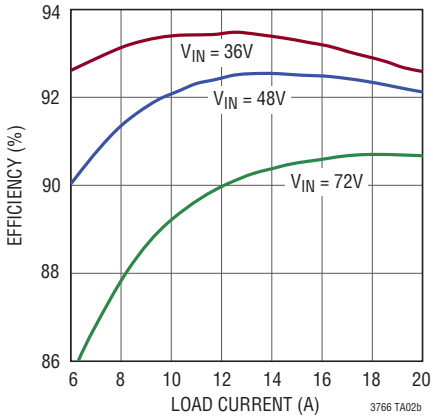
TYPICAL APPLICATION

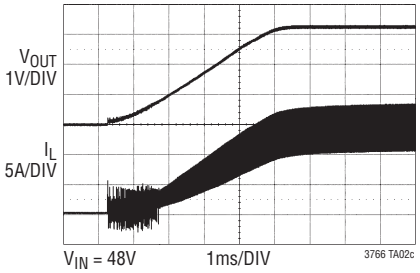
36V-72V to 3.3V/20A Nonisolated Resonant-Reset Forward Converter



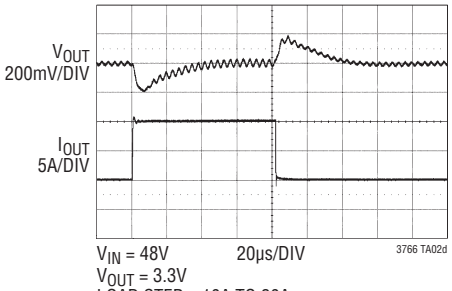
Efficiency vs Load Current



Start-Up



Load Step



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3765	Active Clamp Forward Controller and Gate Driver	Direct Flux Limit, Supports Self-Starting Secondary Forward Control, Works in Conjunction with LTC3766
LT®3752/ LT3752-1	Active Clamp Synchronous Forward Controllers with Internal Housekeeping Controller	Input Voltage Range: LT3752: 6.5V to 100V, LT3752-1: Limited Only by External Components
LT3753	Active Clamp Synchronous Forward Controller	Input Voltage Range: 8.5V to 100V
LT8310	100V Forward Converter Controller	Input Voltage Range: 6V to 100V, TSSOP-20
LTC3721-1/LTC3721-2	Non-Synchronous Push-Pull and Full-Bridge Controllers	Minimizes External Components, On-Chip MOSFET Drivers
LTC3722/LTC3722-2	Synchronous Isolated Full Bridge Controllers	Adaptive or Manual Delay Control for Zero Voltage Switching, Adjustable Synchronous Rectification Timing

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