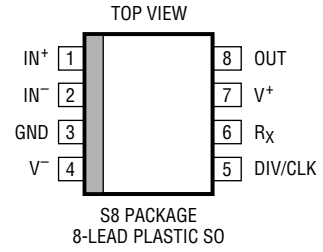
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage 11V
Power Dissipation 500mW
Operating Temperature
LTC1569C ..... 0°C to 70°C
LTC1569I ..... –40°C to 85°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 80°C/W (Note 6)

ORDER PART NUMBER
LTC1569CS8-7 LTC1569IS8-7
S8 PART MARKING
15697 1569I7

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V (V^+ = 3V, V^- = 0V), f_{CUTOFF} = 128kHz, R_{LOAD} = 10k unless otherwise specified.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Filter Gain	V_S = 5V, f_{CLK} = 8.192MHz, f_{CUTOFF} = 256kHz, V_{IN} = 2.5V_{P-P}, R_{EXT} = 5k, Pin 5 Shorted to Pin 4	f_{IN} = 5120Hz = 0.02 • f_{CUTOFF}	●	–0.10	0.00	0.10	dB
		f_{IN} = 51.2kHz = 0.2 • f_{CUTOFF}	●	–0.25	–0.15	–0.05	dB
		f_{IN} = 128kHz = 0.5 • f_{CUTOFF}	●	–0.50	–0.41	–0.25	dB
		f_{IN} = 204.8kHz = 0.8 • f_{CUTOFF}	●	–1.1	–0.65	–0.40	dB
		f_{IN} = 256kHz = f_{CUTOFF}, LTC1569C	●	–5.7	–3.8	–2.3	dB
		f_{IN} = 256kHz = f_{CUTOFF}, LTC1569I	●	–6.2	–3.8	–2.0	dB
		f_{IN} = 384kHz = 1.5 • f_{CUTOFF}	●		–58	–48	dB
		f_{IN} = 512kHz = 2 • f_{CUTOFF}	●		–62	–54	dB
		f_{IN} = 768kHz = 3 • f_{CUTOFF}	●		–67	–64	dB
	V_S = 2.7V, f_{CLK} = 1MHz, f_{CUTOFF} = 31.25kHz, V_{IN} = 1V_{P-P}, Pin 6 Shorted to Pin 4, External Clock	f_{IN} = 625Hz = 0.02 • f_{CUTOFF}	●	–0.08	0.00	0.12	dB
		f_{IN} = 6.25kHz = 0.2 • f_{CUTOFF}	●	–0.25	–0.15	–0.05	dB
		f_{IN} = 15.625kHz = 0.5 • f_{CUTOFF}	●	–0.50	–0.40	–0.30	dB
		f_{IN} = 25kHz = 0.8 • f_{CUTOFF}	●	–0.75	–0.65	–0.50	dB
		f_{IN} = 31.25kHz = f_{CUTOFF}	●	–3.3	–3.15	–3.0	dB
		f_{IN} = 46.875kHz = 1.5 • f_{CUTOFF}	●		–57	–52	dB
		f_{IN} = 62.5kHz = 2 • f_{CUTOFF}	●		–60	–54	dB
		f_{IN} = 93.75kHz = 3 • f_{CUTOFF}	●		–66	–58	dB
Filter Phase	V_S = 2.7V, f_{CLK} = 4MHz, f_{CUTOFF} = 125kHz, Pin 6 Shorted to Pin 4, External Clock	f_{IN} = 2500Hz = 0.02 • f_{CUTOFF}			–11		Deg
		f_{IN} = 25kHz = 0.2 • f_{CUTOFF}	●	–114	–112	–110	Deg
		f_{IN} = 62.5kHz = 0.5 • f_{CUTOFF}	●	78	80	82	Deg
		f_{IN} = 100kHz = 0.8 • f_{CUTOFF}	●	–85	–83	–81	Deg
		f_{IN} = 125kHz = f_{CUTOFF}	●	155	158	161	Deg
		f_{IN} = 187.5kHz = 1.5 • f_{CUTOFF}			–95		Deg
Filter Cutoff Accuracy when Self-Clocked	R_{EXT} = 10.24k from Pin 6 to Pin 7, V_S = 3V, Pin 5 Shorted to Pin 4				125kHz ±1%		
Filter Output DC Swing	V_S = 3V, Pin 3 = 1.11V				2.1		V_{P-P}
			●	1.9			V_{P-P}
	V_S = 5V, Pin 3 = 2V				3.9		V_{P-P}
			●	3.7			V_{P-P}
	V_S = ±5V				8.6		V_{P-P}
		LTC1569C	●	8.4			V_{P-P}
		LTC1569I	●	8.0			V_{P-P}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V (V^+ = 3V, V^- = 0V), f_{CLK} = 4.096MHz, f_{CUTOFF} = 128kHz, R_{LOAD} = 10k unless otherwise specified.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output DC Offset (Note 2)	R_{EXT} = 10k, Pin 5 Shorted to Pin 4	V_S = 3V V_S = 5V V_S = ±5V			±2 ±6 ±15	±5 ±12	mV mV mV
Output DC Offset Drift	R_{EXT} = 10k, Pin 5 Shorted to Pin 4	V_S = 3V V_S = 5V V_S = ±5V			–25 –25 ±25		µV/°C µV/°C µV/°C
Clock Pin Logic Thresholds when Clocked Externally	V_S = 3V	Min Logical "1" Max Logical "0"			2.6 0.5		V V
	V_S = 5V	Min Logical "1" Max Logical "0"			4.0 0.5		V V
	V_S = ±5V	Min Logical "1" Max Logical "0"			4.0 0.5		V V
Power Supply Current (Note 3)	f_{CLK} = 1.028MHz (10k from Pin 6 to Pin 7, Pin 5 Open, ÷ 4), f_{CUTOFF} = 32kHz	V_S = 3V	 ●		6	8 9	mA mA
		V_S = 5V	 ●		7	9 10	mA mA
		V_S = 10V	 ●		9	13 14	mA mA
	f_{CLK} = 4.096MHz (10k from Pin 6 to Pin 7, Pin 5 Shorted to Pin 4, ÷ 1), f_{CUTOFF} = 128kHz	V_S = 3V	 ●		9.5	 14	mA mA
	f_{CLK} = 8.192MHz (5k from Pin 6 to Pin 7, Pin 5 Shorted to Pin 4, ÷ 1), f_{CUTOFF} = 256kHz	V_S = 5V	 ●		20	 30	mA mA
		V_S = 10V	 ●		27	 37	mA mA
Power Supply Voltage where Low Power Mode is Enabled	Pin 5 Shorted to Pin 4, Note 3		●	3.7	4.2	4.6	V
Clock Feedthrough	R_{EXT} = 10k, Pin 5 Open				0.4		mV_{RMS}
Wideband Noise	Noise BW = DC to 2 • f_{CUTOFF}				125		μV_{RMS}
THD	f_{IN} = 10kHz, 1.5V_{P-P}				74		dB
Clock-to-Cutoff Frequency Ratio					32		
Max Clock Frequency (Note 4)	V_S = 3V V_S = 5V V_S = ±5V				5 9.6 13		MHz MHz MHz
Min Clock Frequency (Note 5)	3V to ±5V, T_A < 85°C				3		kHz
Input Frequency Range	Aliased Components <–65dB				0.9 • f_{CLK}		Hz

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: DC offset is measured with respect to Pin 3.

Note 3: There are several operating modes which reduce the supply current. For V_S < 4V, relative to divide-by-1 mode, the current is typically reduced by 50% relative to V_S = 5V. If the internal oscillator is used as the clock source and the divide-by-4 or divide-by-16 mode is enabled, the supply current is typically reduced by 60%,relative to divide-by-1 mode, independent of the value of V_S.

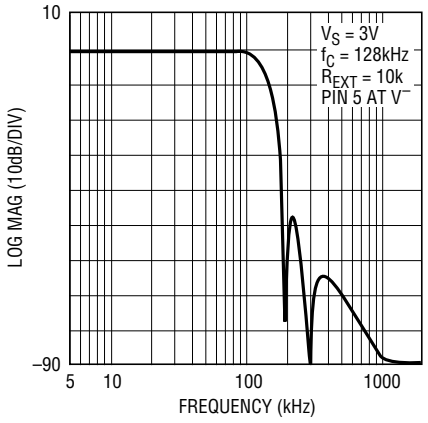
Note 4: The maximum clock frequency is arbitrarily defined as the frequency at which the filter AC response exhibits >1dB of gain peaking.

Note 5: The minimum clock frequency is arbitrarily defined as the frequecy at which the filter DC offset changes by more than 5mV.

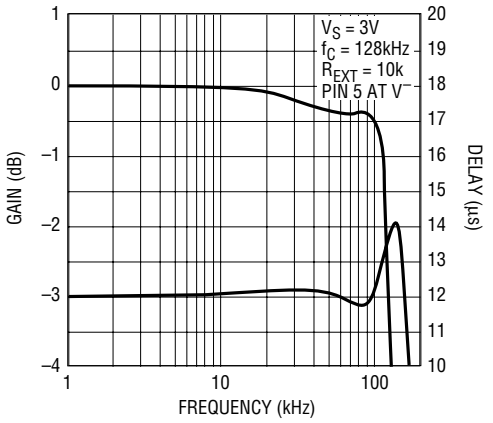
Note 6: Thermal resistance varies depending upon the amount of PC board metal attached to the device. θ_{JA} is specified for a 2500mm^2 test board covered with 2oz copper on both sides.

TYPICAL PERFORMANCE CHARACTERISTICS

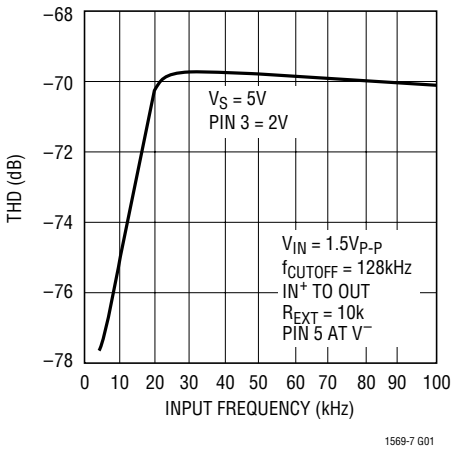
Gain vs Frequency



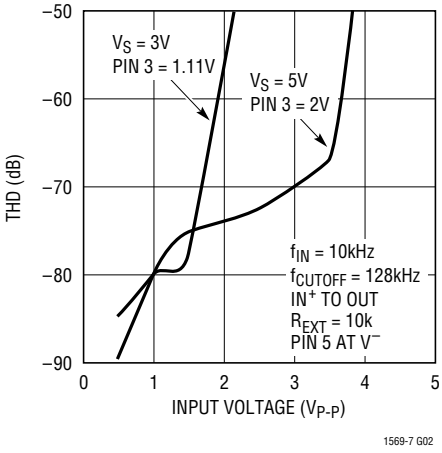
Passband Gain and Group Delay vs Frequency



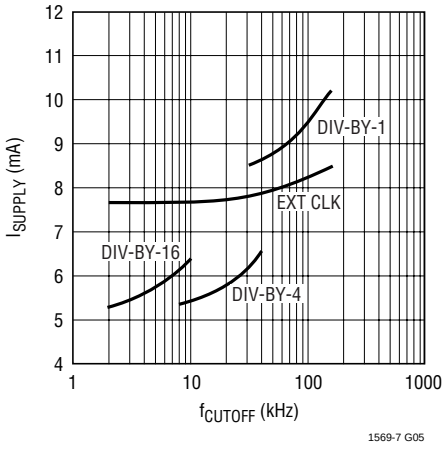
THD vs Input Frequency



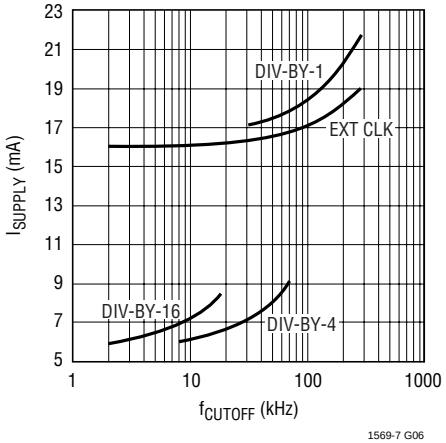
THD vs Input Voltage



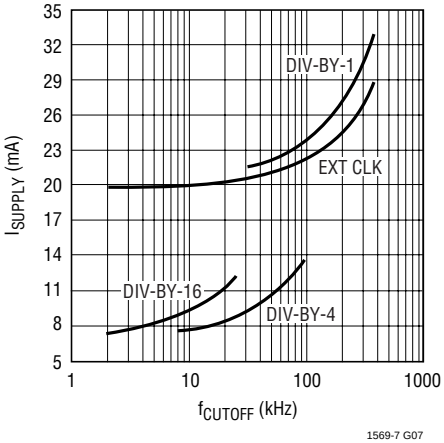
3V Supply Current



5V Supply Current



±5V Supply Current



PIN FUNCTIONS

IN^+/IN^- (Pins 1, 2): Signals can be applied to either or both input pins. The DC gain from IN^+ (Pin 1) to OUT (Pin 8) is 1.0, and the DC gain from Pin 2 to Pin 8 is –1. The input range, input resistance and output range are described in the Applications Information section. Input voltages which exceed the power supply voltages should be avoided. Transients will not cause latchup if the current into/out of the input pins is limited to 20mA.

GND (Pin 3): The GND pin is the reference voltage for the filter and should be externally biased to 2V (1.11V) to maximize the dynamic range of the filter in applications using a single 5V (3V) supply. For single supply operation, the GND pin should be bypassed with a quality 1µF ceramic capacitor to V^- (Pin 4). The impedance of the circuit biasing the GND pin should be less than 2kΩ as the GND pin generates a small amount of AC and DC current. For dual supply operation, connect Pin 3 to a high quality DC ground. A ground plane should be used. A poor ground will increase DC offset, clock feedthrough, noise and distortion.

V^-/V^+ (Pins 4, 7): For 3V, 5V and ±5V applications a quality 1µF ceramic bypass capacitor is required from V^+ (Pin 7) to V^- (Pin 4) to provide the transient energy for the internal clock drivers. The bypass should be as close as possible to the IC. In dual supply applications (Pin 3 is grounded), an additional 0.1µF bypass from V^+ (Pin 7) to GND (Pin 3) and V^- (Pin 4) to GND (Pin 3) is recommended.

The maximum voltage difference between GND (Pin 3) and V^+ (Pin 7) should not exceed 5.5V.

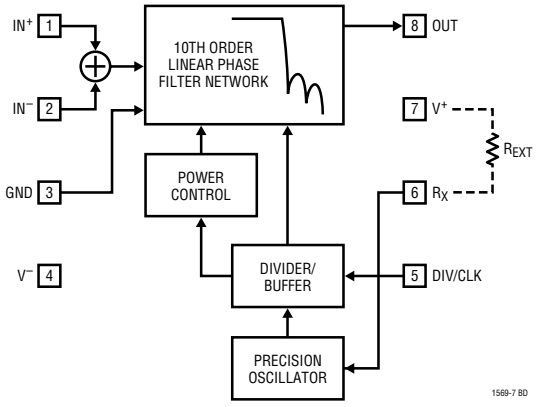
DIV/CLK (Pin 5): DIV/CLK serves two functions. When the internal oscillator is enabled, DIV/CLK can be used to engage an internal divider. The internal divider is set to 1:1 when DIV/CLK is shorted to V^- (Pin 4). The internal divider is set to 4:1 when DIV/CLK is allowed to float (a 100pF bypass to V^- is recommended). The internal divider is set to 16:1 when DIV/CLK is shorted to V^+ (Pin 7). In the divide-by-4 and divide-by-16 modes the power supply current is reduced by typically 60%.

When the internal oscillator is disabled (R_X shorted to V^-) DIV/CLK becomes an input pin for applying an external clock signal. For proper filter operation, the clock waveform should be a squarewave with a duty cycle as close as possible to 50% and CMOS voltages levels (see Electrical Characteristics section for voltage levels). DIV/CLK pin voltages which exceed the power supply voltages should be avoided. Transients will not cause latchup if the fault current into/out of the DIV/CLK pin is limited to 40mA.

R_X (Pin 6): Connecting an external resistor between the R_X pin and V^+ (Pin 7) enables the internal oscillator. The value of the resistor determines the frequency of oscillation. The maximum recommended resistor value is 40k and the minimum is 3.8k/8k (single 5V/3V supply). The internal oscillator is disabled by shorting the R_X pin to V^- (Pin 4). (Please refer to the Applications Information section.)

OUT (Pin 8): Filter Output. This pin can drive 10kΩ and/or 40pF loads. For larger capacitive loads, an external 100Ω series resistor is recommended. The output pin can exceed the power supply voltages by up to ±2V without latchup.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Self-Clocking Operation

The LTC1569-7 features a unique internal oscillator which sets the filter cutoff frequency using a single external resistor. The design is optimized for V_S = 3V, f_{CUTOFF} = 128kHz, where the filter cutoff frequency error is typically <1% when a 0.1% external 10k resistor is used. With different resistor values and internal divider settings, the cutoff frequency can be accurately varied from 2kHz to 150kHz/300kHz (single 3V/5V supply). As shown in Figure 1, the divider is controlled by the DIV/CLK (Pin 5). Table 1 summarizes the cutoff frequency vs external resistor values for the divide-by-1 mode.

In the divide-by-4 and divide-by-16 modes, the cutoff frequencies in Table 1 will be lowered by 4 and 16 respectively. When the LTC1569-7 is in the divide-by-4 and divide-by-16 modes the power is automatically reduced. This results in a 60% power savings with a single 5V supply.

Table1. f_{CUTOFF} vs R_{EXT}, V_S = 3V, T_A = 25°C, Divide-by-1 Mode

R_{EXT}	Typical f_{CUTOFF}	Typical Variation of f_{CUTOFF}
3844Ω	320kHz	±3.0%
5010Ω	256kHz	±2.5%
10k	128kHz	±1%
20.18k	64kHz	±2.0%
40.2k	32kHz	±3.5%

The power reduction in the divide-by-4 and divide-by-16 modes, however, effects the fundamental oscillator frequency. Hence, the effective divide ratio will be slightly different from 4:1 or 16:1 depending on V_S, T_A and R_{EXT}. Typically this error is less than 1% (Figures 4 and 6).

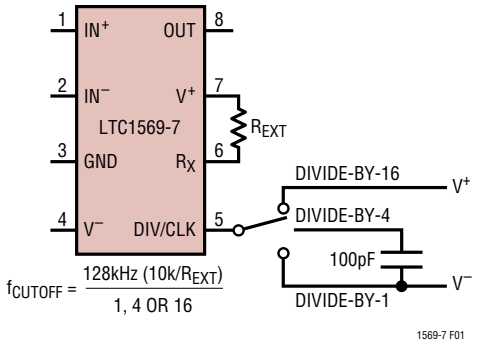


Figure 1

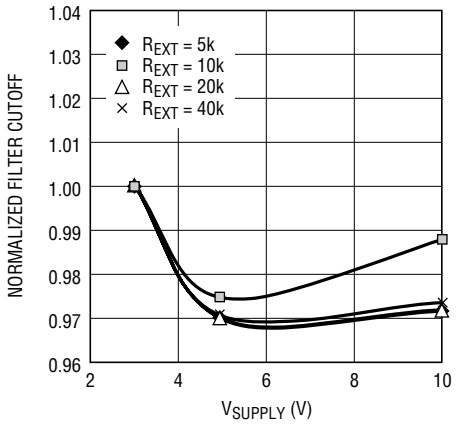


Figure 2. Filter Cutoff vs V_{SUPPLY}, Divide-by-1 Mode, T_A = 25°C

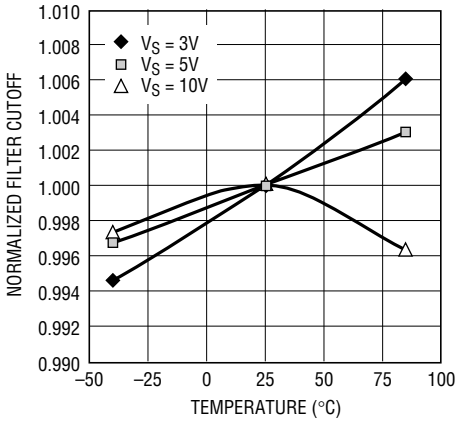


Figure 3. Filter Cutoff vs Temperature, Divide-by-1 Mode, R_{EXT} = 10k

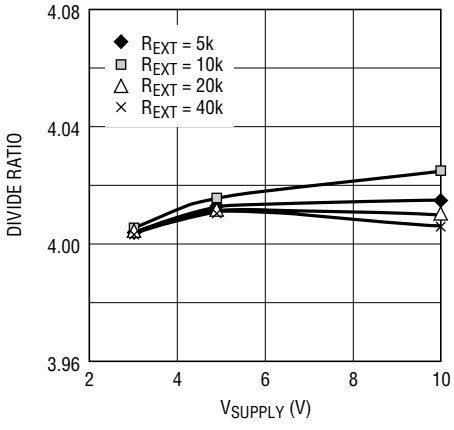


Figure 4. Typical Divide Ratio in the Divide-by-4 Mode, T_A = 25°C

APPLICATIONS INFORMATION

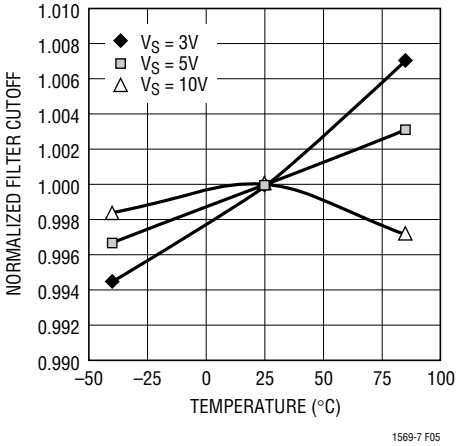


Figure 5. Filter Cutoff vs Temperature, Divide-by-4 Mode, R_{EXT} = 10k

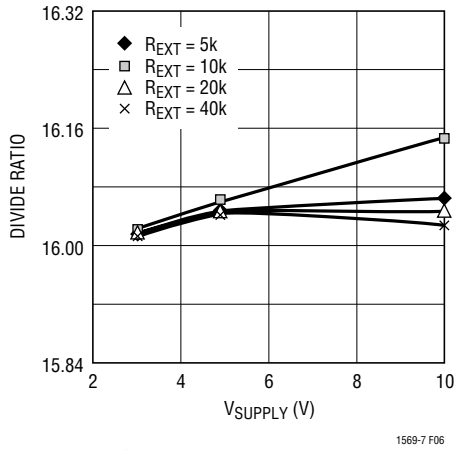


Figure 6. Typical Divide Ratio in the Divide-by-16 Mode, T_A = 25°C

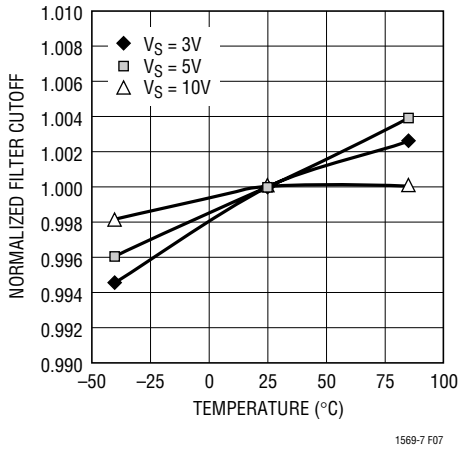


Figure 7. Filter Cutoff vs Temperature, Divide-by-16 Mode, R_{EXT} = 10k

The cutoff frequency is easily estimated from the equation in Figure 1. Examples 1 and 2 illustrate how to use the graphs in Figures 2 through 7 to get a more precise estimate of the cutoff frequency.

Example 1: LTC1569-7, R_{EXT} = 20k, V_S = 3V, divide-by-16 mode, DIV/CLK (Pin 5) connected to V^+ (Pin 7), T_A = 25°C.

Using the equation in Figure 1, the approximate filter cutoff frequency is f_{CUTOFF} = 128kHz • (10k/20k) • (1/16) = 4kHz.

For a more precise f_{CUTOFF} estimate, use Table 1 to get a value of f_{CUTOFF} when R_{EXT} = 20k and use the graph in Figure 6 to find the correct divide ratio when V_S = 3V and R_{EXT} = 20k. Based on Table 1 and Figure 6, f_{CUTOFF} = 64kHz • (20.18k/20k) • (1/16.02) = 4.03kHz.

From Table 1, the part-to-part variation of f_{CUTOFF} will be ±2%. From the graph in Figure 7, the 0°C to 70°C drift of f_{CUTOFF} will be –0.2% to 0.2%.

Example 2: LTC1569-7, R_{EXT} = 5k, V_S = 5V, divide-by-1 mode, DIV/CLK (Pin 5) connected to V^- (Pin 4), T_A = 25°C.

Using the equation in Figure 1, the approximate filter cutoff frequency is f_{CUTOFF} = 128kHz • (10k/5k) • (1/1) = 256kHz.

For a more precise f_{CUTOFF} estimate, use Table 1 to get f_{CUTOFF} frequency for R_{EXT} = 5k and use Figure 2 to correct for the supply voltage when V_S = 5V. From Table 1 and Figure 2, f_{CUTOFF} = 256k • (5.01k/5k) • 0.970 = 249kHz.

APPLICATIONS INFORMATION

The oscillator is sensitive to transients on the positive supply. The IC should be soldered to the PC board and the PCB layout should include a 1µF ceramic capacitor between V^+ (Pin 7) and V^- (Pin 4) , as close as possible to the IC to minimize inductance. Avoid parasitic capacitance on R_X and avoid routing noisy signals near R_X (Pin 6). Use a ground plane connected to V^- (Pin 4) for single supply applications. Connect a ground plane to GND (Pin 3) for dual supply applications and connect V^- (Pin 4) to a copper trace with low thermal resistance.

Input and Output Range

The input signal range includes the full power supply range. The output voltage range is typically (V^- + 50mV) to (V^+ – 0.8V) when V_S = 3V. To maximize the undistorted peak-to-peak signal swing of the filter, the GND (Pin 3) voltage should be set to 2V (1.11V) in single 5V (3V) supply applications.

The LTC1569-7 can be driven with a single-ended or differential signal. When driven differentially, the voltage between IN^+ and IN^- (Pin 1 and Pin 2) is filtered with a DC gain of 1. The single-ended output voltage OUT (Pin 8) is referenced to the voltage of the GND (Pin 3). The common mode voltage of IN^+ and IN^- can be any voltage that keeps the input signals within the power supply range.

For noninverting single-ended applications, connect IN^- to GND or to a quiet DC reference voltage and apply the input signal to IN^+. If the input is DC coupled then the DC gain from IN^+ to OUT will be 1. This is true given IN^+ and OUT are referenced to the same voltage, i.e., GND, V^- or some other DC reference. To achieve the distortion levels shown in the Typical Performance Characteristics the input signal at IN^+ should be centered around the DC voltage at IN^-. The input can also be AC coupled, as shown in the Typical Applications section.

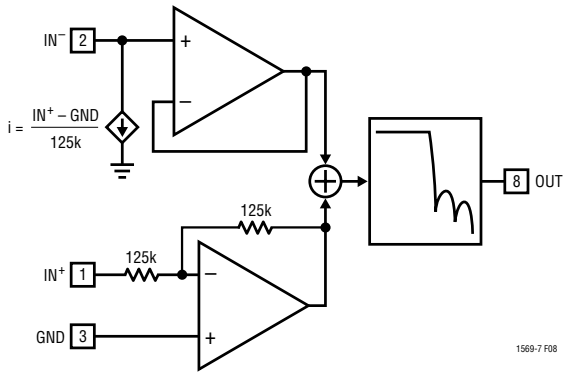


Figure 8

For inverting single-ended filtering, connect IN^+ to GND or to quiet DC reference voltage. Apply the signal to IN^-. The DC gain from IN^- to OUT is –1, assuming IN^- is referenced to IN^+ and OUT is reference to GND.

Refer to the Typical Performance Characteristics section to estimate the THD for a given input level.

Dynamic Input Impedance

The unique input sampling structure of the LTC1569-7 has a dynamic input impedance which depends on the configuration, i.e., differential or single-ended, and the clock frequency. The equivalent circuit in Figure 8 illustrates the input impedance when the cutoff frequency is 128kHz. For other cutoff frequencies replace the 125k value with 125k • (128kHz/f_{CUTOFF}).

When driven with a single-ended signal into IN^- with IN^+ tied to GND, the input impedance is very high (~10MΩ). When driven with a single-ended signal into IN^+ with IN^- tied to GND, the input impedance is a 125k resistor to GND. When driven with a complementary signal whose common mode voltage is GND, the IN^+ input appears to have 125k to GND and the IN^- input appears to have –125k to GND. To make the effective IN^- impedance 125k when driven differentially, place a 62.5k resistor from IN^- to GND. For other cutoff frequencies use 62.5k • (128kHz/f_{CUTOFF}), as shown in the Typical Applications section. The typical variation in dynamic input impedance for a given clock frequency is ±10%.

Wideband Noise

The wideband noise of the filter is the RMS value of the device's output noise spectral density. The wideband noise data is used to determine the operating signal-to-noise at a given distortion level. The wideband noise is nearly independent of the value of the clock frequency and excludes the clock feedthrough. Most of the wideband noise is concentrated in the filter passband and cannot be removed with post filtering (Table 2). Table 3 lists the typical wideband noise for each supply.

APPLICATIONS INFORMATION

Table 2. Wideband Noise vs Supply Voltage, Single 3V Supply

Bandwidth	Total Integrated Noise
DC to f_{CUTOFF}	105μV_{RMS}
DC to 2 • f_{CUTOFF}	125μV_{RMS}
DC to f_{CLK}	155μV_{RMS}

Table 3. Wideband Noise vs Supply Voltage, f_{CUTOFF} = 128kHz

Power Supply	Total Integrated Noise DC to 2 • f_{CUTOFF}
3V	125μV_{RMS}
5V	135μV_{RMS}
±5V	145μV_{RMS}

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's OUT pin (Pin 8). The clock feedthrough is measured with IN^+ and IN^- (Pins 1 and 2) grounded and depends on the PC board layout and the power supply decoupling. Table 4 shows the clock feedthrough (the RMS sum of the first 11 harmonics) when the LTC1569-7 is self-clocked with R_{EXT} = 10k, DIV/CLK (Pin 5) open (divide-by-4 mode). The clock feedthrough can be reduced with a simple RC post filter.

Table 4. Clock Feedthrough

Power Supply	Feedthrough
3V	0.4mV_{RMS}
5V	0.6mV_{RMS}
±5V	0.9mV_{RMS}

DC Accuracy

DC accuracy is defined as the error in the output voltage after DC offset and DC gain errors are removed. This is similar to the definition of the integral nonlinearity in A/D converters. For example, after measuring values of $V_{OUT(DC)}$ vs $V_{IN(DC)}$ for a typical LTC1569-7, a linear regression shows that $V_{OUT(DC)} = V_{IN(DC)} • 0.99854 + 0.00134V$ is the straight line that best fits the data. The DC accuracy describes how much the actual data deviates from this straight line (i.e., DCERROR = $V_{OUT(DC)} - (V_{IN(DC)} • 0.99854 + 0.00134V)$. In a 12-bit system with a full-scale value of 2V, the LSB is 488µV. Therefore, if the DCERROR of the filter is less than 488µV over a 2V range, the filter has 12-bit DC accuracy. Figure 9 illustrates the typical DC accuracy of the LTC1569-7 on a single 5V supply.

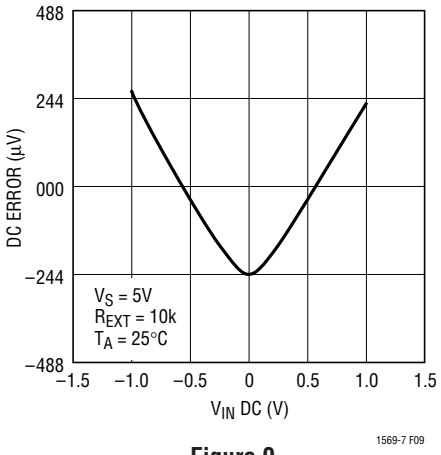


Figure 9

DC Offset

The output DC offset of the LTC1569-7 is trimmed to less than ±5mV. The trimming is performed with V_S = 1.9V, –1.1V with the filter cutoff frequency set to 8kHz (R_{EXT} = 10k, DIV/CLK shorted to V^+). To obtain optimum DC offset performance, appropriate PC layout techniques should be used. The filter IC should be soldered to the PC board. The power supplies should be well decoupled including a 1µF ceramic capacitor from V^+ (Pin 7) to V^- (Pin 4). A ground plane should be used. Noisy signals should be isolated from the filter input pins.

When the power supply is 3V, the output DC offset typically change less than ±2mV when the clock frequency varies from 64kHz to 8192kHz. When the clock frequency is fixed, the output DC offset will typically change by ±4mV (±13mV) when the power supply varies from 3V to 5V (±5V) in the divide-by-1 mode. In the divide-by-4 or divide-by-16 modes, the output DC offset will typically change –9mV (–27mV) when the power supply varies from 3V to 5V (±5V). The offset is measured with respect to GND (Pin 3).

Aliasing

Aliasing is an inherent phenomenon of sampled data filters. In lowpass filters significant aliasing only occurs when the frequency of the input signal approaches the sampling frequency or multiples of the sampling frequency. The LTC1569-7 samples the input signal twice

APPLICATIONS INFORMATION

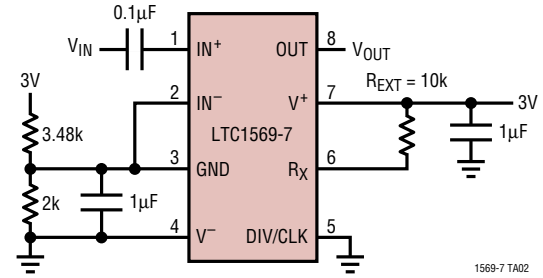
every clock period. Therefore, the sampling frequency is twice the clock frequency and 64 times the filter cutoff frequency. Input signals with frequencies near 2 • f_{CLK} ± f_{CUTOFF} will be aliased to the passband of the filter and appear at the output unattenuated.

Power Supply Current

The power supply current depends on the operating mode. When the LTC1569-7 is in the divide-by-1 mode, or when clocked externally, the supply current is reduced by 50% for supply voltages below 4V. For the divide-by-4 and divide-by-16 modes, the supply current is reduced by 60% relative to the current when clocked externally, independent of the power supply voltage. Power supply current versus cutoff frequency for various operating modes is shown in the "Typical Performance Characteristics" section.

TYPICAL APPLICATIONS

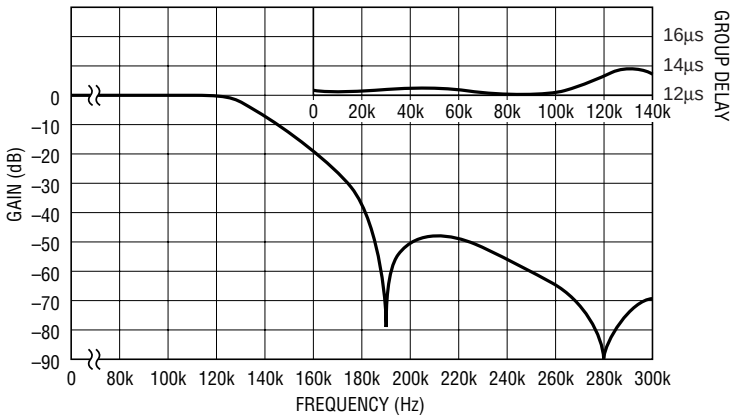
Single 3V Operation, AC Coupled Input, 128kHz Cutoff Frequency



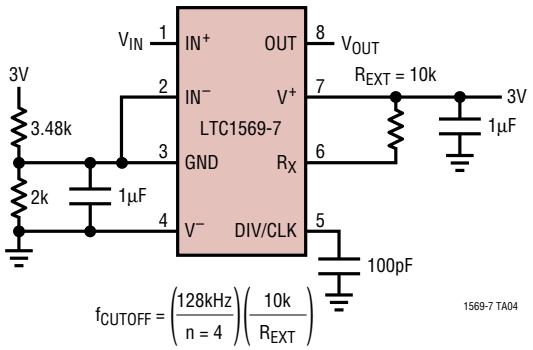
$$f_{CUTOFF} = \left(\frac{128kHz}{n = 1}\right)\left(\frac{10k}{R_{EXT}}\right)$$

n = 1, 4, 16 FOR PIN 5 AT GROUND, OPEN, V^+

Single 3V, AC Coupled Input, 128kHz Cutoff Frequency



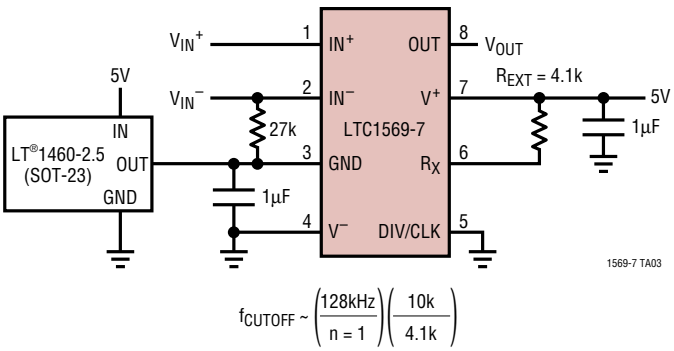
Single 3V Supply Operation, DC Coupled, 32kHz Cutoff Frequency



$$f_{CUTOFF} = \left(\frac{128kHz}{n = 4}\right)\left(\frac{10k}{R_{EXT}}\right)$$

n = 1, 4, 16 FOR PIN 5 AT GROUND, OPEN, V^+

Single 5V Operation, 300kHz Cutoff Frequency, DC Coupled Differential Inputs with Balanced Input Impedance

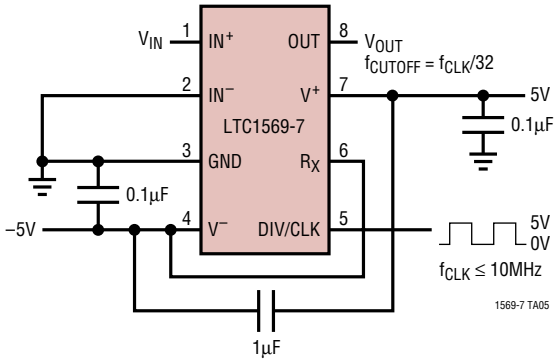


$$f_{CUTOFF} \sim \left(\frac{128kHz}{n = 1}\right)\left(\frac{10k}{4.1k}\right)$$

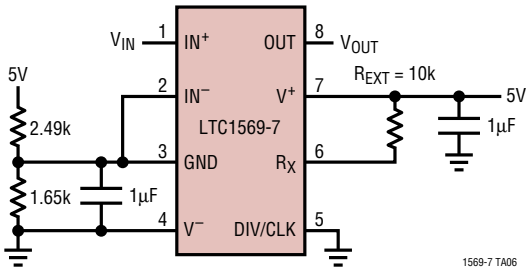
n = 1, 4, 16 FOR PIN 5 AT GROUND, OPEN, V^+

TYPICAL APPLICATION

**Dual 5V Supply Operation,
DC Coupled Filter with External Clock Source**



**Single 5V Supply Operation, DC Coupled Input,
128kHz Cutoff Frequency**



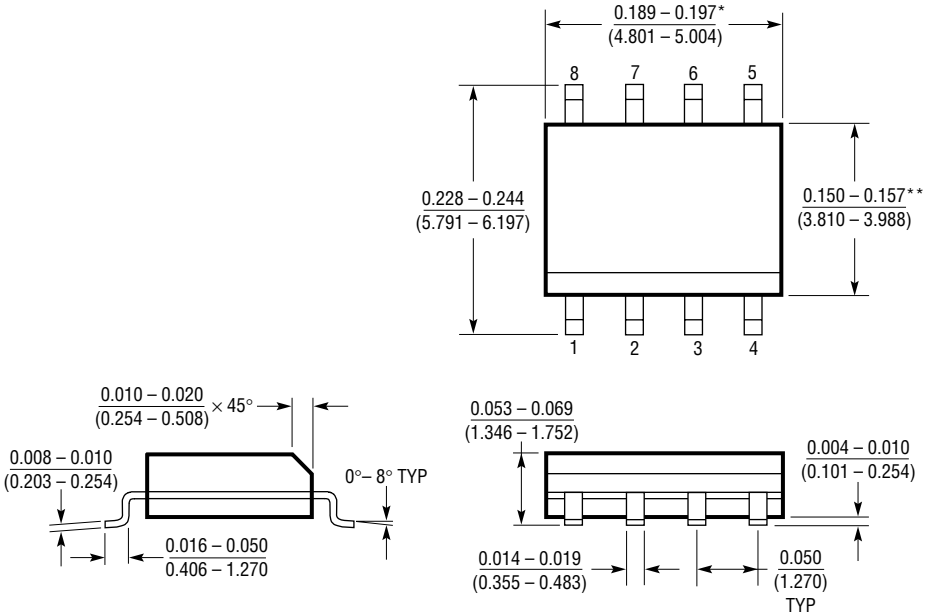
$$f_{CUTOFF} = \left(\frac{128kHz}{n=1}\right)\left(\frac{10k}{R_{EXT}}\right)$$

n = 1, 4, 16 FOR PIN 5 AT
GROUND, OPEN, V+

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

**S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)**
(LTC DWG # 05-08-1610)



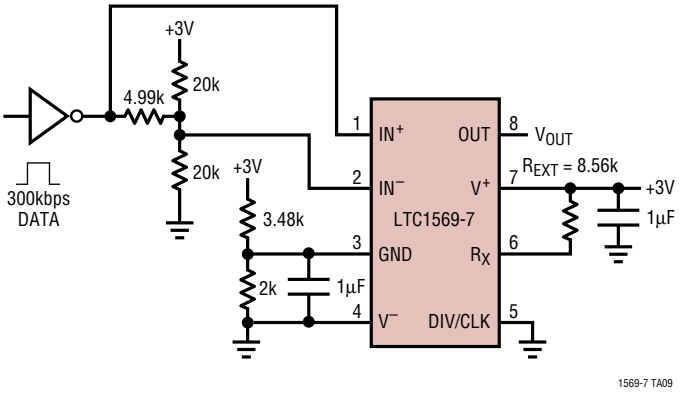
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

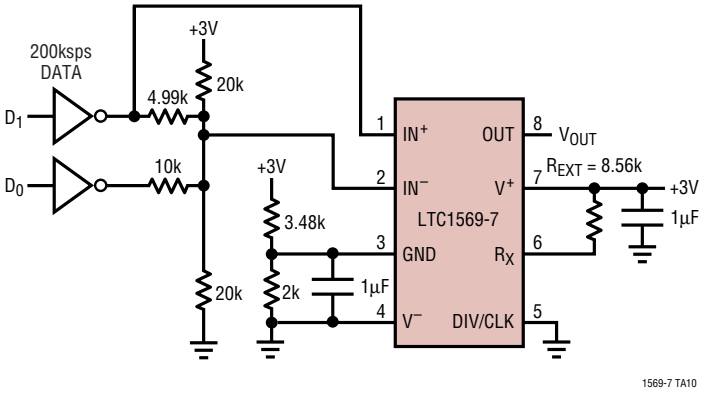
S08 0996

TYPICAL APPLICATIONS

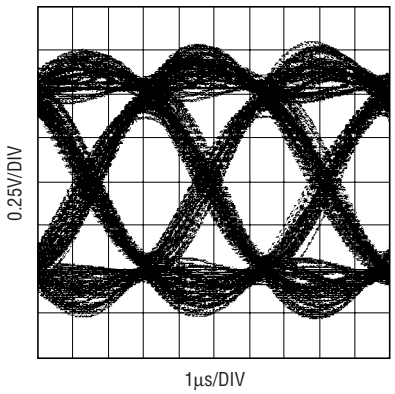
Pulse Shaping Circuit for Single 3V Operation, 300kbps 2 level data, 150kHz Cutoff Filter



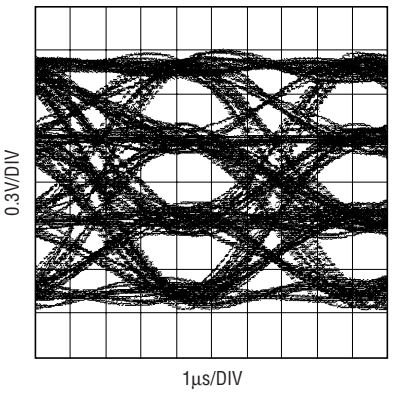
Pulse Shaping Circuit for Single 3V Operation, 400kbps (200ksps) 4 Level Data, 128kHz Cutoff Filter



2-Level, 300kbps Eye Diagram



4-Level, 400kbps (200ksps) Eye Diagram



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064-3	Linear Phase, Bessel 8th Order Filter	f_{CLK}/f_{CUTOFF} = 75/1 or 150/1, Very Low Noise
LTC1064-7	Linear Phase, 8th Order Lowpass Filter	f_{CLK}/f_{CUTOFF} = 50/1 or 100/1, $f_{CUTOFF(MAX)}$ = 100kHz
LTC1068-x	Universal, 8th Order Filter	f_{CLK}/f_{CUTOFF} = 25/1, 50/1, 100/1 or 200/1, $f_{CUTOFF(MAX)}$ = 200kHz
LTC1069-7	Linear Phase, 8th Order Lowpass Filter	f_{CLK}/f_{CUTOFF} = 25/1, $f_{CUTOFF(MAX)}$ = 200kHz, SO-8
LTC1164-7	Low Power, Linear Phase Lowpass Filter	f_{CLK}/f_{CUTOFF} = 50/1 or 100/1, I_S = 2.5mA, V_S = 5V
LTC1264-7	Linear Phase, 8th Order Lowpass Filter	f_{CLK}/f_{CUTOFF} = 25/1 or 50/1, $f_{CUTOFF(MAX)}$ = 200kHz
LTC1562/LTC1562-2	Universal, 8th Order Active RC Filter	$f_{CUTOFF(MAX)}$ = 150kHz (LTC1562) $f_{CUTOFF(MAX)}$ = 300kHz (LTC1562-2)

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