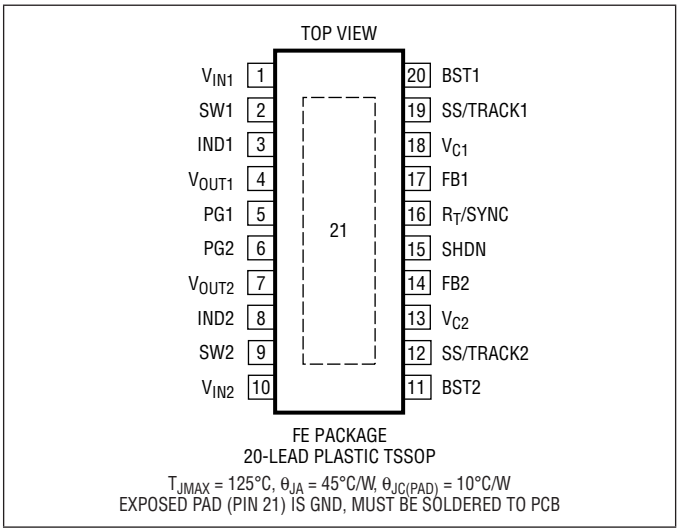
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN1/2}$, SHDN, PG1/2 ..... 25V/–0.3V
SW1/2 ..... $V_{IN1/2}$
BST1/2 ..... 35V/–0.3V
BST1/2 Pins Above SW1/2 ..... 25V
IND1/2 ..... ±5A
$V_{OUT1/2}$ ..... $V_{IN1/2}$/–0.3V
FB1/2, SS1/2, R_T/SYNC 5.5V
$V_{C1/2}$ ..... ±1mA
Operating Junction Temperature Range
LT3501EFE (Notes 2, 8) ..... –40°C to 125°C
LT3501IFE (Notes 2, 8) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3501EFE#PBF	LT3501EFE#TRPBF	LT3501	20-Lead Plastic TSSOP	–40°C to 125°C
LT3501IFE#PBF	LT3501IFE#TRPBF	LT3501	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. $V_{VIN1/2}$ = 15V, $V_{BST1/2}$ = open, $V_{RT/SYNC}$ = 2V, $V_{VOUT1/2}$ = open, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SHDN Threshold	$V_{OUT1/2}$ = 0V, R_T/SYNC = 133k	●	1.23	1.28	1.37	V
SHDN Input Current	V_{SHDN} = 1.375V V_{SHDN} = 1.225V		7 2	10 3	13 5	µA µA
Minimum Input Voltage Ch 1 (Note 3)	$V_{FB1/2}$ = 0V, $V_{VOUT1/2}$ = 0V, $V_{IND1/2}$ = 0V, R_T/SYNC = 133k			2.8	3	V
Minimum Input Voltage Ch 2	$V_{FB1/2}$ = 0V, $V_{VOUT1/2}$ = 0V, $V_{IND1/2}$ = 0V			2.8	3	V
Supply Shutdown Current Ch 1	V_{SHDN} = 0V	●		9	30	µA
Supply Shutdown Current Ch 2	V_{SHDN} = 0V			0	5	µA
Supply Quiescent Current Ch 1	$V_{FB1/2}$ = 0.9V			3.5	5	mA
Supply Quiescent Current Ch 2	$V_{FB1/2}$ = 0.9V			200	500	µA
Feedback Voltage Ch 1/Ch 2	$V_{VC1/2}$ = 1V	●	0.784	0.8	0.816	V
Feedback Voltage Line Regulation	$V_{VIN1/2}$ = 3V to 25V	●	–1	0	1	%
Feedback Voltage Offset Ch 1 to Ch 2	$V_{VC1/2}$ = 1V	●	–16	0	16	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. $V_{VIN1/2}$ = 15V, $V_{BST1/2}$ = open, $V_{RT/SYNC}$ = 2V, $V_{VOUT1/2}$ = open, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Bias Current Ch 1/Ch 2	$V_{FB1/2}$ = 0.8V, $V_{VC1/2}$ = 1V	●	–250	75	250	nA
Error Amplifier g_m Ch 1/Ch 2	$V_{VC1/2}$ = 1V, $I_{VC1/2}$ = ±5µA	●	150	275	450	µmho
Error Amplifier Gain Ch 1/Ch 2				1000		V/V
Error Amplifier to Switch Gain Ch 1/Ch 2				3.3		A/V
Error Amplifier Source Current Ch 1/Ch 2	$V_{FB1/2}$ = 0.6V, $V_{VC1/2}$ = 1V		10	15	25	µA
Error Amplifier Sink Current Ch 1/Ch 2	$V_{FB1/2}$ = 1V, $V_{VC1/2}$ = 1V		15	20	30	µA
Error Amplifier High Clamp Ch 1/Ch 2	$V_{FB1/2}$ = 0.7V		1.75	2.0	2.25	V
Error Amplifier Switching Threshold Ch 1/Ch 2	$V_{OUT1/2}$ = 5V, R_T/SYNC = 133k		0.5	0.7	1	V
Soft-Start Source Current Ch 1/Ch 2	$V_{FB1/2}$ = 0.6V, $V_{SS1/2}$ = 0.4V	●	2	3	4.2	µA
Soft-Start V_{OH} Ch 1/Ch 2	$V_{FB1/2}$ = 0.9V		1.9	2	2.4	V
Soft-Start Sink Current Ch 1/Ch 2	$V_{FB1/2}$ = 0.6V, $V_{SS1/2}$ = 1V		200	600	1000	µA
Soft-Start V_{OL} Ch 1/Ch 2	$V_{FB1/2}$ = 0V		50	80	125	mV
Soft-Start to Feedback Offset Ch 1/Ch 2	$V_{VC1/2}$ = 1V, $V_{SS1/2}$ = 0.4V	●	–16	0	16	mV
Soft-Start Sink Current Ch 1/Ch 2 POR	$V_{SS1/2}$ = 0.4V (Note 4), V_{VC} = 1V		0.5	1.5	2	mA
Soft-Start POR Threshold Ch 1/Ch 2	$V_{FB1/2}$ = 0V (Note 4)		55	80	105	mV
Soft-Start Switching Threshold Ch 1/Ch 2	$V_{FB1/2}$ = 0V		30	50	70	mV
Power Good Leakage Ch 1/Ch 2	$V_{FB1/2}$ = 0.9V, $V_{PG1/2}$ = 25V, $V_{VIN1/2}$ = 25V			0	1	µA
Power Good Threshold Ch 1/Ch 2	$V_{FB1/2}$ Rising, PG1/2 = 20k to 5V	●	87	90	93	%
Power Good Hysteresis Ch 1/Ch 2	$V_{FB1/2}$ Falling, PG1/2 = 20k to 5V		20	30	50	mV
Power Good Sink Current Ch 1/Ch 2	$V_{FB1/2}$ = 0.65V, $V_{PG1/2}$ = 0.4V		400	800	1200	µA
Power Good Shutdown Sink Current Ch 1/Ch 2	$V_{VIN1/2}$ = 2V, $V_{FB1/2}$ = 0V, $V_{PG1/2}$ = 0.4V		10	50	100	µA
R_T/SYNC Reference Voltage	$V_{FB1/2}$ = 0.9V, $I_{RT/SYNC}$ = –40µA		0.93	0.975	1	V
Switching Frequency	R_T/SYNC = 133k, $V_{FB1/2}$ = 0.6V, $V_{BST1/2}$ = V_{SW} + 3V R_T/SYNC = 15.4k, $V_{FB1/2}$ = 0.6V, $V_{BST1/2}$ = V_{SW} + 3V		200 1.2	250 1.5	300 1.8	kHz MHz
Switching Phase Angle Ch A to Ch B	R_T/SYNC = 133k, $V_{FB1/2}$ = 0.6V, $V_{BST1/2}$ = V_{SW} + 3V		120	180	210	Deg
Minimum Boost for 100% Duty Cycle Ch 1/Ch 2	$V_{FB1/2}$ = 0.7V, $I_{RT/SYNC}$ = –35µA (Note 5), V_{OUT} = 0V			1.7	2	V
SYNC Frequency Range	$V_{BST1/2}$ = V_{SW} + 3V		250		1500	kHz
SYNC Switching Phase Angle Ch A to Ch B	SYNC Frequency = 250kHz, $V_{BST1/2}$ = V_{SW} + 3V		120	180	210	Deg
IND + V_{OUT} Current Ch 1/Ch 2	$V_{VOUT1/2}$ = 0V, $V_{FB1/2}$ = 0.9V $V_{VOUT1/2}$ = 5V		40	70 0	100 1	µA µA
IND to V_{OUT} Maximum Current Ch 1/Ch 2	$V_{VOUT1/2}$ = 0.5V (Note 6), $V_{FB1/2}$ = 0.7V, $V_{BST1/2}$ = 20V $V_{VOUT1/2}$ = 5V (Note 6), R_T/SYNC = 133k, $V_{BST1/2}$ = 20V		3.25 3.5	4 4	5 5	A A
Switch Leakage Current Ch 1/Ch 2	$V_{SW1/2}$ = 0V, $V_{VIN1/2}$ = 25V	●		0	50	µA
Switch Saturation Voltage Ch 1/Ch 2	$I_{SW1/2}$ = 3A, $V_{BST1/2}$ = 20V, $V_{FB1/2}$ = 0.7V	●		250	600	mV
Boost Current Ch 1/Ch 2	$I_{SW1/2}$ = 3A, $V_{BST1/2}$ = 20V, $V_{FB1/2}$ = 0.7V		25	60	100	mA
Minimum Boost Voltage Ch 1/Ch 2	$I_{SW1/2}$ = 3A, $V_{BST1/2}$ = 20V, $V_{FB1/2}$ = 0.7V			1.4	2.5	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3501EFE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3501IFE is guaranteed and tested over the full –40°C to 125°C operating junction temperature range.

Note 3: Minimum input voltage is defined as the voltage where internal bias lines are regulated so that the reference voltage and oscillator remain constant. Actual minimum input voltage to maintain a regulated output will depend upon output voltage and load current. See Applications Information.

ELECTRICAL CHARACTERISTICS

Note 4: An internal power-on reset (POR) latch is set on the positive transition of the SHDN pin through its threshold. The output of the latch activates current sources on each SS pin which typically sink 1.5mA, discharging the SS capacitor. The latch is reset when both SS pins are driven below the soft-start POR threshold or the SHDN pin is taken below its threshold.

Note 5: To enhance dropout operation, the output switch will be turned off for the minimum off-time only when the voltage across the boost capacitor drops below the minimum boost for 100% duty cycle threshold.

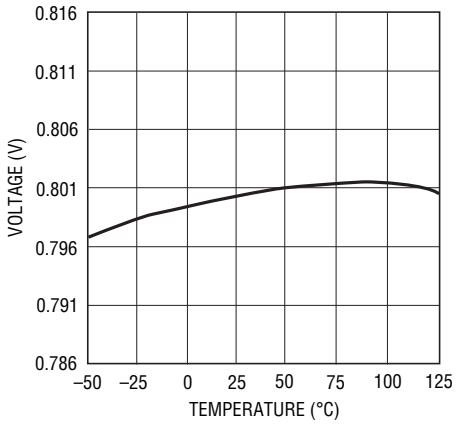
Note 6: The IND to V_{OUT} maximum current is defined as the value of current flowing from the IND pin to the V_{OUT} pin which resets the switch latch when the V_C pin is at its high clamp.

Note 7: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

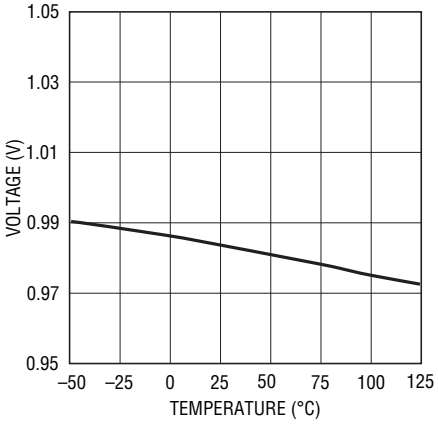
Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

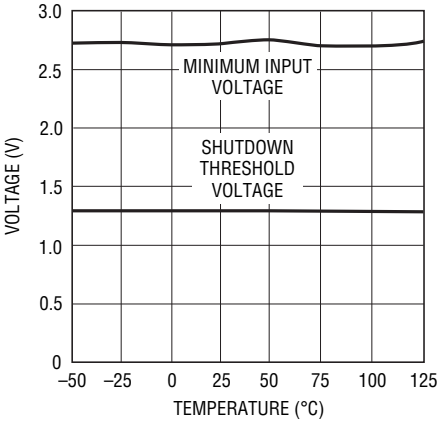
Feedback Voltage vs Temperature



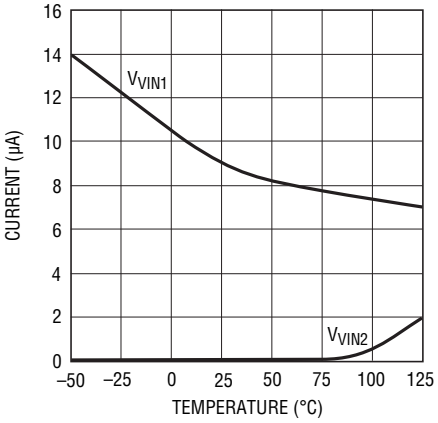
R_T/SYNC Voltage vs Temperature



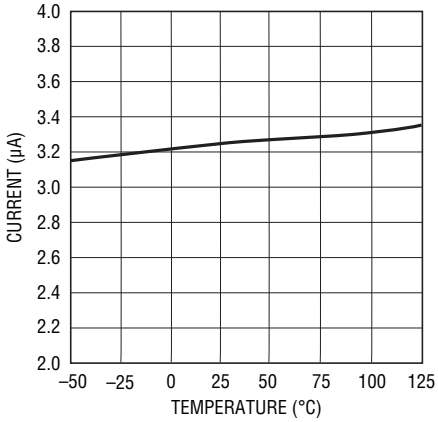
Shutdown Threshold and Minimum Input Voltage vs Temperature



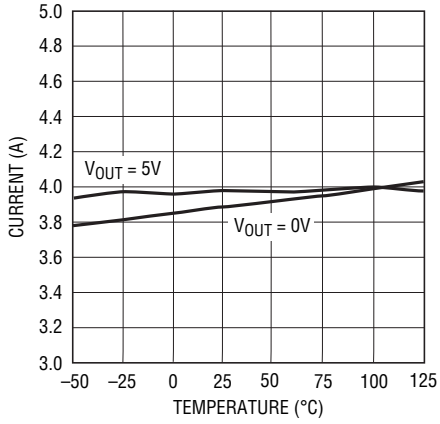
Shutdown Quiescent Current vs Temperature



Soft-Start Source Current vs Temperature

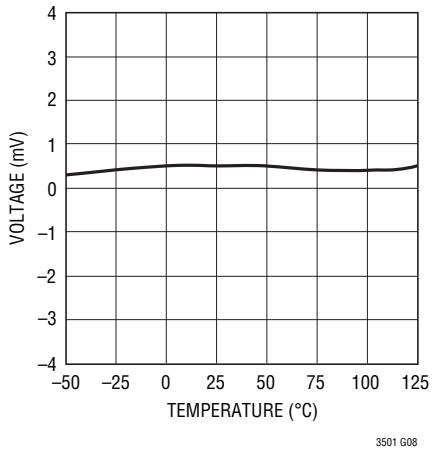


IND to V_{OUT} Maximum Current vs Temperature

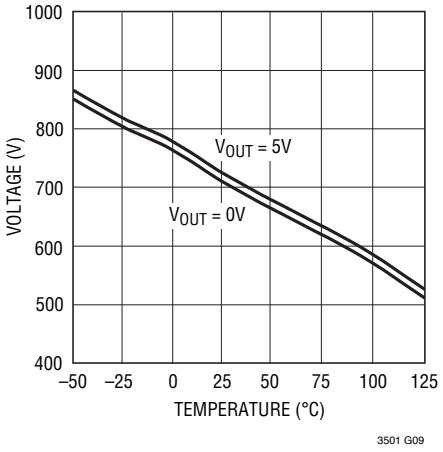


TYPICAL PERFORMANCE CHARACTERISTICS

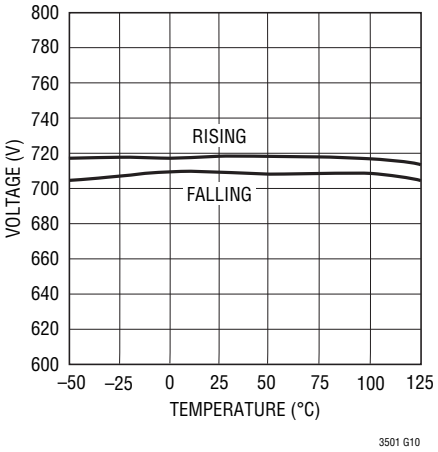
Soft-Start to Feedback Offset Voltage vs Temperature



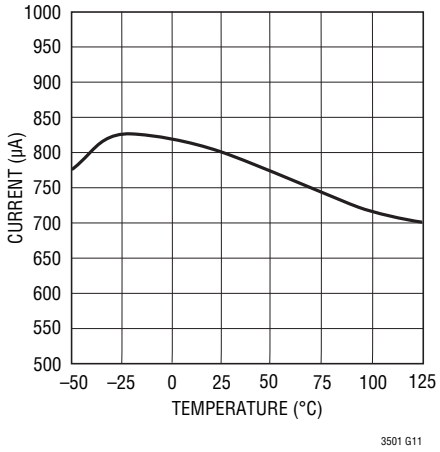
V_C Switching Threshold Voltage vs Temperature



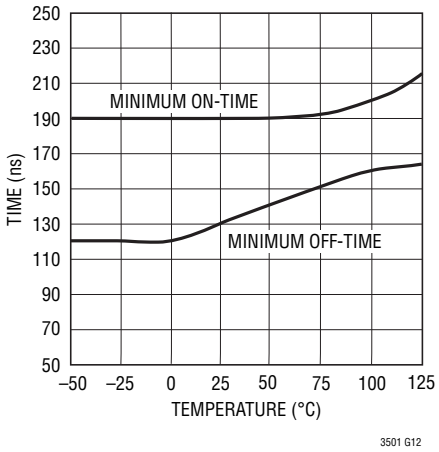
Power Good Threshold Voltage vs Temperature



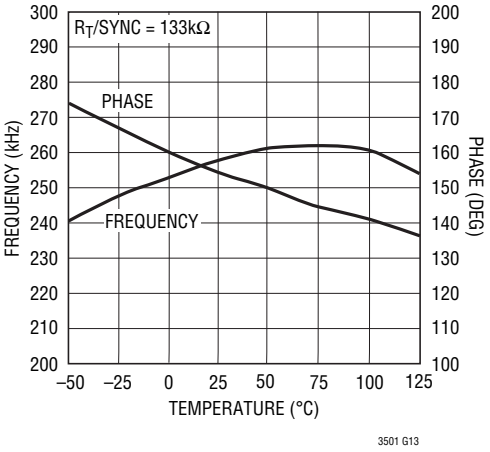
Power Good Sink Current vs Temperature



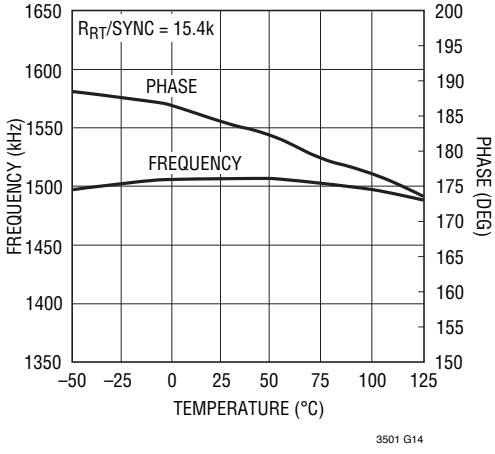
Minimum Switching Times vs Temperature



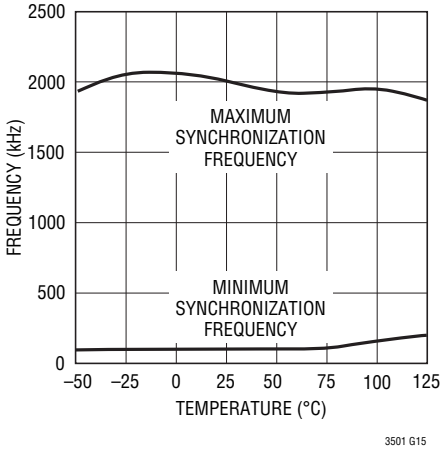
Switching Frequency and Channel Phase vs Temperature



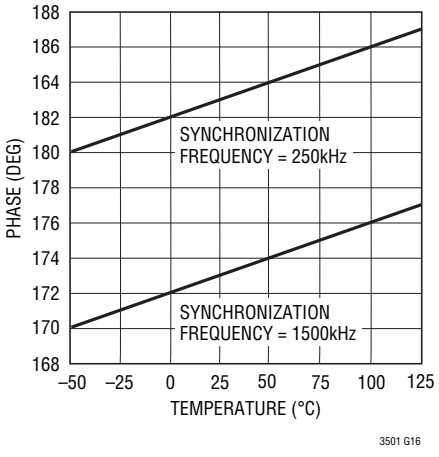
Switching Frequency and Channel Phase vs Temperature



Synchronization Clock Frequency Range vs Temperature

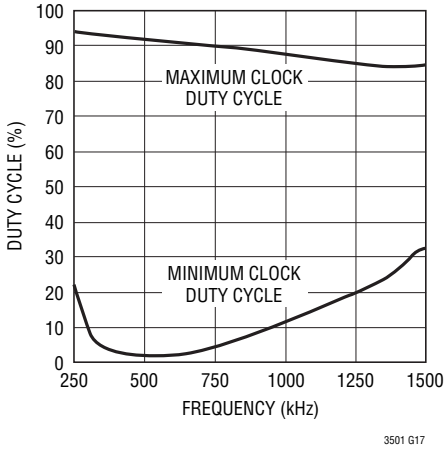


Channel Phase vs Temperature with External Synchronization

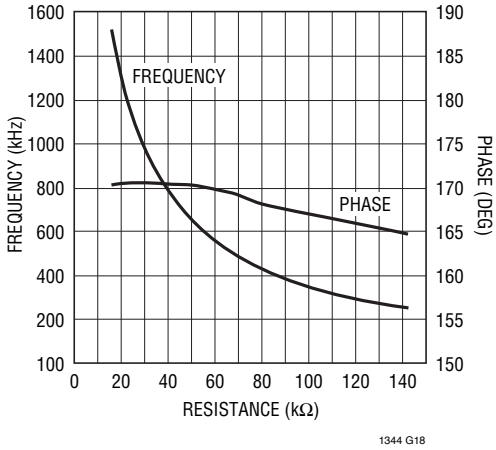


TYPICAL PERFORMANCE CHARACTERISTICS

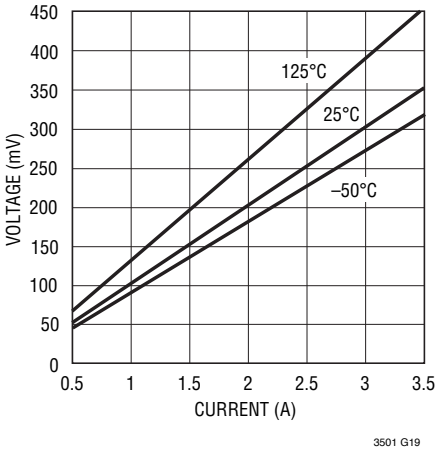
External Sync Duty Cycle Range vs External Sync Frequency



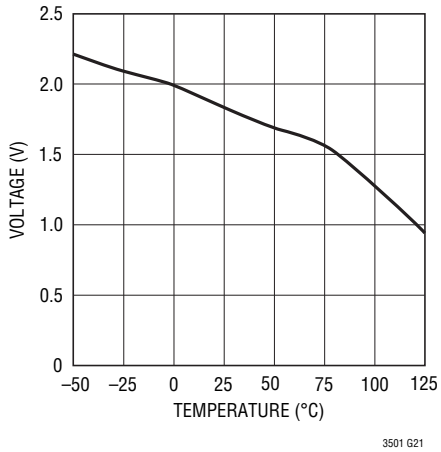
Frequency and Phase vs R_T/SYNC Pin Resistance



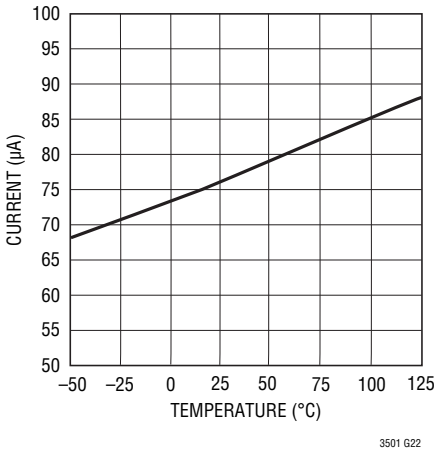
Switch Saturation Voltage vs Switch Current



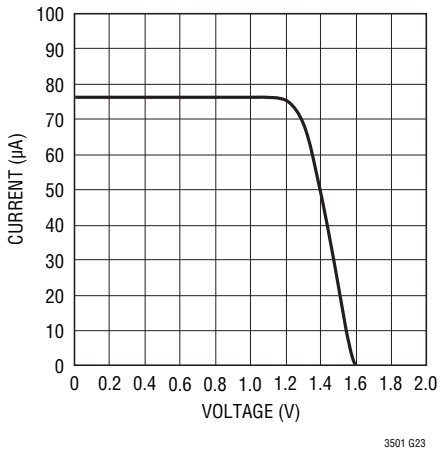
Minimum Boost Voltage vs Temperature



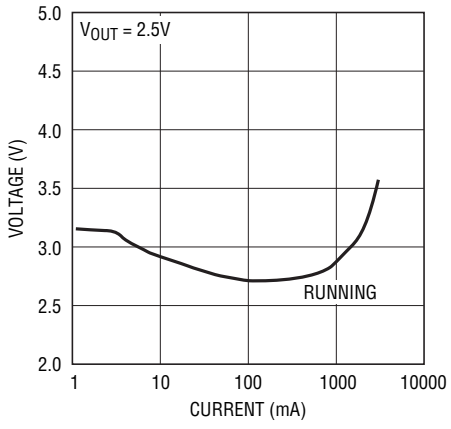
V_{OUT} + IND Current vs Temperature



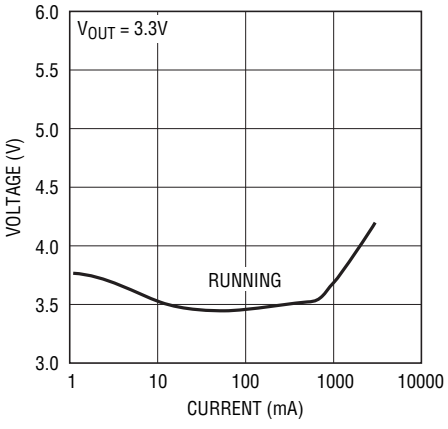
V_{OUT} + IND Current vs Voltage



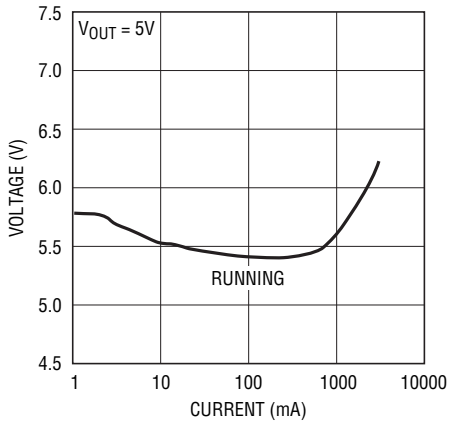
Minimum Input Voltage vs Load Current



Minimum Input Voltage vs Load Current

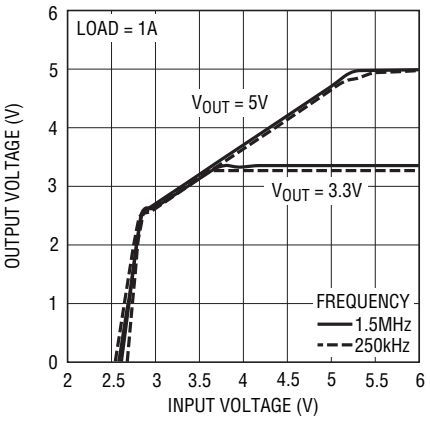


Minimum Input Voltage vs Load Current



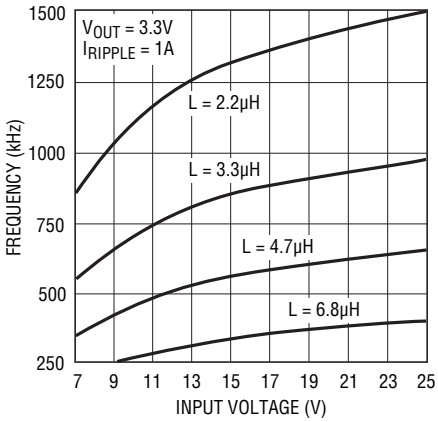
TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Operation



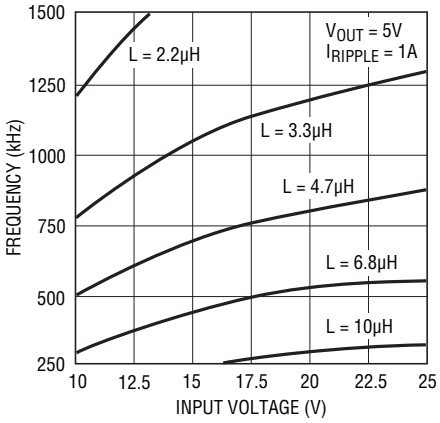
3501 G27

Inductor Value vs Frequency for 3A Maximum Load Current



3501 G28

Inductor Value vs Frequency for 3A Maximum Load Current



3501 G29

PIN FUNCTIONS

V_{IN1} (Pin 1): The V_{IN1} pin powers the internal control circuitry for both channels and is monitored by the undervoltage lockout comparator. The V_{IN1} pin is also connected to the collector of channel 1's on-chip power NPN switch. The V_{IN1} pin has high dI/dt edges and must be decoupled to ground close to the pin of the device.

SW1/SW2 (Pins 2, 9): The SW pin is the emitter of the on-chip power NPN. At switch-off, the inductor will drive this pin below ground with a high dV/dt. An external Schottky catch diode to ground, close to the SW pin and respective V_{IN} decoupling capacitor's ground, must be used to prevent this pin from excessive negative voltages.

IND1/IND2 (Pins 3, 8): The IND pin is the input to the on-chip sense resistor that measures current flowing in the inductor. When the current in the resistor exceeds the current dictated by the V_C pin, the SW latch is held in reset, disabling the output switch. Bias current flows out of the IND pin when IND is less than 1.6V.

V_{OUT1}/V_{OUT2} (Pins 4, 7): The V_{OUT} pin is the output to the on-chip sense resistor that measures current flowing in the inductor. When the current in the resistor exceeds the current dictated by the V_C pin, the SW latch is held in reset, disabling the output switch. Bias current flows out of the V_{OUT} pin when V_{OUT} is less than 1.6V.

PG1/PG2 (Pins 5, 6): The power good pin is an open-collector output that sinks current when the feedback falls below 90% of its nominal regulating voltage. For V_{IN1} above 1V, its output state remains true, although during shutdown, V_{IN1} undervoltage lockout or thermal shutdown, its current sink capability is reduced. The PG pins can be left open circuit or tied together to form a single power good signal.

V_{IN2} (Pin 10): The V_{IN2} pin is the collector of channel 2's on-chip power NPN switch. This pin is independent of V_{IN1} and may be connected to the same or a separate supply. In either case, high dI/dt edges are present and decoupling to ground must be used close to this pin.

SS1/SS2 (Pins 19, 12): The SS1/2 pins control the soft-start and sequence of their respective outputs. A single capacitor from the SS pin to ground determines the output ramp rate. For soft-start and output tracking/sequencing details, see the Applications Information section.

V_{C1}/V_{C2} (Pins 18, 13): The V_C pin is the output of the error amplifier and the input to the peak switch current comparator. It is normally used for frequency compensation, but can also be used as a current clamp or control loop override. If the error amplifier drives V_C above the maximum switch current level, a voltage clamp activates. This indicates that the output is overloaded and current is pulled from the SS pin, reducing the regulation point.

FB1/FB2 (Pins 17, 14): The FB pin is the negative input to the error amplifier. The output switches regulate this pin to 0.8V, with respect to the exposed ground pad. Bias current flows out of the FB pin.

SHDN (Pin 15): The shutdown pin is used to turn off both channels and control circuitry to reduce quiescent current to a typical value of 9µA. The accurate 1.28V threshold and input current hysteresis can be used as an undervoltage lockout, preventing the regulator from operating until the input voltage has reached a predetermined level. Force the SHDN pin above its threshold or let it float for normal operation.

R_T/SYNC (Pin 16): This R_T/SYNC pin provides two modes of setting the constant switch frequency.

Connecting a resistor from the R_T/SYNC pin to ground will set the R_T/SYNC pin to a typical value of 0.975V. The resultant switching frequency will be set by the resistor value. The minimum value of 15.4k and maximum value of 133k sets the switching frequency to 1.5MHz and 250kHz, respectively.

Driving the R_T/SYNC pin with an external clock signal will synchronize the switch to the applied frequency. Synchronization occurs on the rising edge of the clock signal after

PIN FUNCTIONS

the clock signal is detected, with switch 1 in phase with the synchronization signal. Each rising clock edge initiates an oscillator ramp reset. A gain control loop servos the oscillator charging current to maintain a constant oscillator amplitude. Hence, the slope compensation and channel phase relationship remain unchanged. If the clock signal is removed, the oscillator reverts to resistor mode and reapplies the 0.975V bias to the R_T/SYNC pin after the synchronization detection circuitry times out. The clock source impedance should be set such that the current out of the R_T/SYNC pin in resistor mode generates a frequency roughly equivalent to the synchronization frequency.

BST1/BST2 (Pins 20, 11): The BST pin provides a higher than V_{IN} base drive to the power NPN to ensure a low switch drop. A comparator to V_{IN} imposes a minimum off-time on the SW pin if the BST pin voltage drops too low. Forcing a SW off-time allows the boost capacitor to recharge.

Exposed Pad (Pin 21): GND. The Exposed Pad GND pin is the **only** ground connection for the device. The Exposed Pad should be soldered to a large copper area to reduce thermal resistance. The GND pin is common to both channels and also serves as small-signal ground. For ideal operation all small-signal ground paths should connect to the GND pin at a single point, avoiding any high current ground returns.

BLOCK DIAGRAM

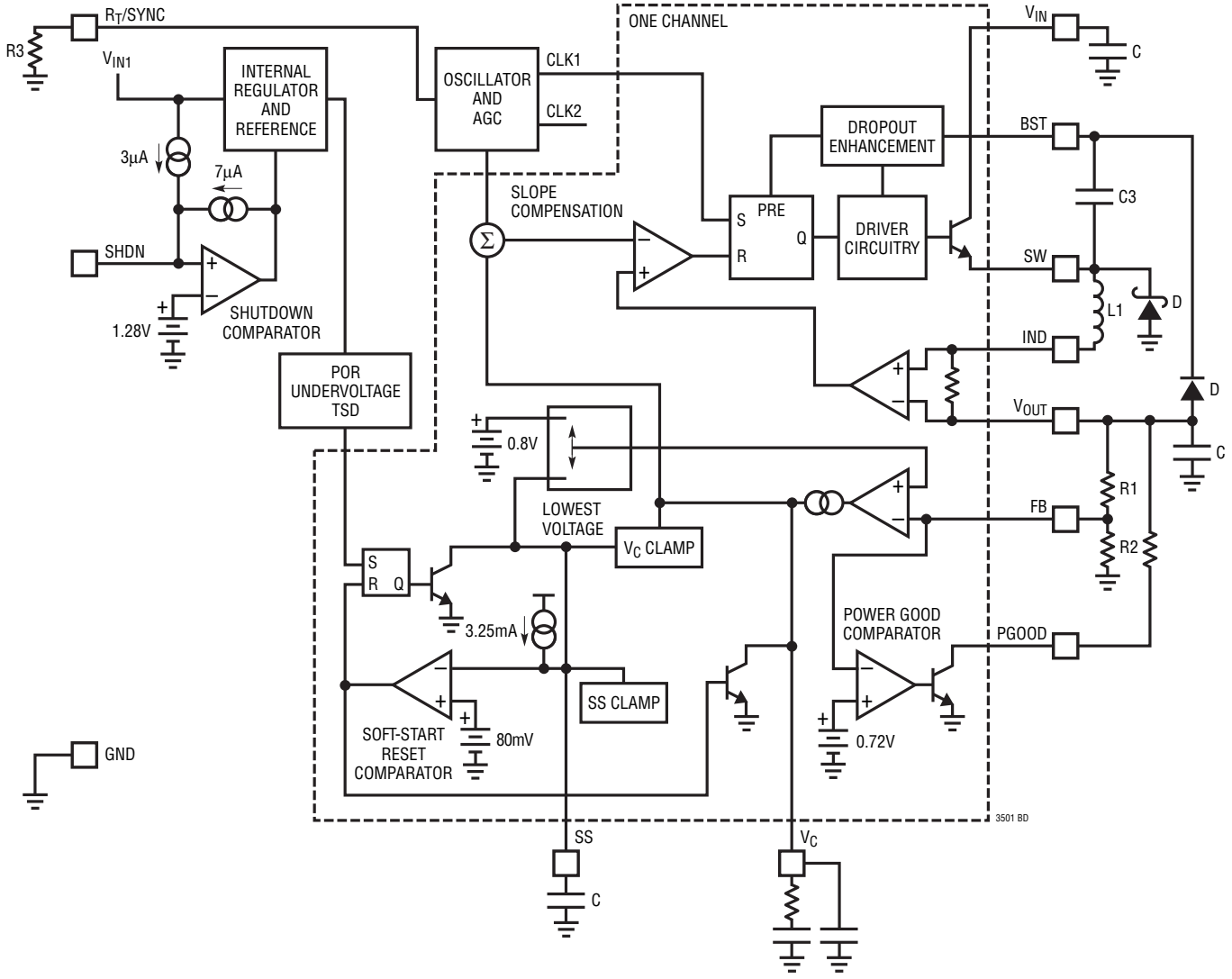


Figure 1. Block Diagram (One of Two Switching Regulators Shown)

The LT3501 is dual-channel, constant-frequency, current mode buck converter with internal 3A switches. Each channel is identical with a common shutdown pin, internal regulator, oscillator, undervoltage detect, thermal shutdown and power-on reset.

If the SHDN pin is taken below its 1.28V threshold the LT3501 will be placed in a low quiescent current mode. In this mode the LT3501 typically draws 9µA from V_{IN1} and <1µA from V_{IN2}. In shutdown mode the PG is active with a typical sink capability of 50µA for V_{IN1} voltage greater than 2V.

When the SHDN pin is opened or driven above 1.28V, the internal bias circuits turn on generating an internal regulated voltage, $0.8V_{FB}$, 0.975V R_T/SYNC references, and a POR signal which sets the soft-start latch.

As the R_T/SYNC pin reaches its 0.975V regulation point, the internal oscillator will start generating two clock signals 180° out of phase for each regulator at a frequency determined by the resistor from the R_T/SYNC pin to ground. Alternatively, if a synchronization signal is detected by the LT3501 at the R_T/SYNC pin, clock signals 180° out of phase

BLOCK DIAGRAM

will be generated at the incoming frequency on the rising edge of the synchronization pulse with switch 1 in phase with the synchronization signal. In addition, the internal slope compensation will be automatically adjusted to prevent subharmonic oscillation during synchronization.

The two regulators are constant-frequency, current mode step-down converters. Current mode regulators are controlled by an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180°, shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

The Block Diagram in Figure 1 shows only one of the switching regulators whose operation will be discussed below. The additional regulator will operate in a similar manner with the exception that its clock will be 180° out of phase with the other regulator.

When, during power-up, the POR signal sets the soft-start latch, both SS pins will be discharged to ground to ensure proper start-up operation. When the SS pin voltage drops below 80mV, the V_C pin is driven low disabling switching and the soft-start latch is reset. Once the latch is reset the soft-start capacitor starts to charge with a typical value of 3.25µA.

As the voltage rises above 80mV on the SS pin, the V_C pin will be driven high by the error amplifier. When the voltage on the V_C pin exceeds 0.7V, the clock set-pulse sets the driver flip-flop which turns on the internal power NPN switch. This causes current from V_{IN}, through the NPN switch, inductor and internal sense resistor, to increase. When the voltage drop across the internal sense resistor exceeds a predetermined level set by the voltage on the V_C pin, the flip-flop is reset and the internal NPN switch is turned off. Once the switch is turned off the inductor will drive the voltage at the SW pin low until the external Schottky diode starts to conduct, decreasing the current in the inductor. The cycle is repeated with the start of each clock cycle. However, if the internal sense resistor voltage exceeds the predetermined level at the start of a clock cycle, the flip-flop will not be set resulting in a further decrease in inductor current. Since the output current is controlled by the V_C voltage, output regulation is achieved by the error amplifier continually adjusting the V_C pin voltage.

The error amplifier is a transconductance amplifier that compares the FB voltage to the lowest voltage present at either the SS pin or an internal 0.8V reference. Compensation of the loop is easily achieved with a simple capacitor or series resistor/capacitor from the V_C pin to ground.

Since the SS pin is driven by a constant current source, a single capacitor on the soft-start pin will generate controlled linear ramp on the output voltage.

If the current demanded by the output exceeds the maximum current dictated by the V_C pin clamp, the SS pin will be discharged, lowering the regulation point until the output voltage can be supported by the maximum current. When overload is removed, the output will soft-start from the overload regulation point.

V_{IN1} undervoltage detection or thermal shutdown will set the soft-start latch, resulting in a complete soft-start sequence.

The switch driver operates from either the V_{IN} or BST voltage. An external diode and capacitor are used to generate a drive voltage higher than V_{IN} to saturate the output NPN and maintain high efficiency. If the BST capacitor voltage is sufficient, the switch is allowed to operate to 100% duty cycle. If the boost capacitor discharges towards a level insufficient to drive the output NPN, a BST pin comparator forces a minimum cycle off-time, allowing the boost capacitor to recharge.

A power good comparator with 30mV of hysteresis trips at 90% of regulated output voltage. The PG output is an open-collector NPN that is off when the output is in regulation allowing a resistor to pull the PG pin to a desired voltage.

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Choosing the Output Voltage

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

R2 should be 10k or less to avoid bias current errors. Reference designators refer to the Block Diagram in Figure 1.

Choosing the Switching Frequency

The LT3501 switching frequency is set by resistor R3 in Figure 1. The R_T/SYNC pin is internally regulated at 0.975V. Setting resistor R3 sets the current in the R_T/SYNC pin which determines the oscillator frequency as illustrated in Figure 2.

The switching frequency is typically set as high as possible to reduce overall solution size. The LT3501 employs techniques to enhance dropout at high frequencies but efficiency and maximum input voltage decrease due to switching losses and minimum switch on-times. The maximum recommended frequency can be approximated by the equation:

$$\text{Frequency (Hz)} = \frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D} \bullet \frac{1}{t_{ON(MIN)}}$$

where V_D is the forward-voltage drop of the catch diode (D1 Figure 2), V_{SW} is the voltage drop of the internal switch, and $t_{ON(MIN)}$ in the minimum on-time of the switch, all at maximum load current.

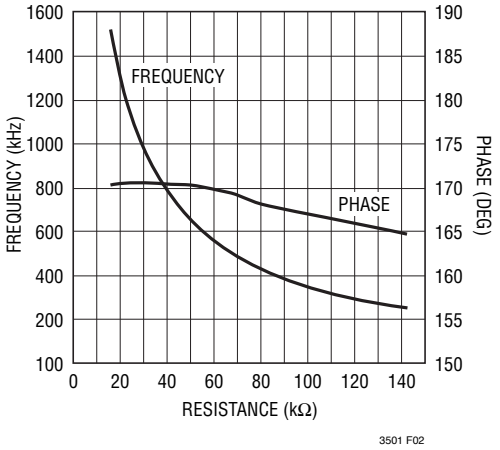

Figure 2. Frequency and Phase vs R_T/SYNC Resistance

The following example along with the data in Table 1 illustrates the trade-offs of switch frequency selection.

Example:

V_{IN} = 25V, V_{OUT} = 3.3V, I_{OUT} = 2.5A,
Temperature = 0°C to 85°C

$t_{ON(MIN)}$ = 200ns (85°C from Typical Characteristics graph), V_D = 0.6V, V_{SW} = 0.4V (85°C)

$$\text{Max Frequency} = \frac{3.3 + 0.6}{25 - 0.4 + 0.6} \bullet \frac{1}{200e\text{-}9} \sim 750\text{kHz}$$

R_T/SYNC ~ 42k (Figure 2)

Input Voltage Range

Once the switching frequency has been determined, the input voltage range of the regulator can be determined. The minimum input voltage is determined by either the LT3501's minimum operating voltage of ~2.8V, or by its maximum

Table 1. Efficiency and Size Comparisons for Different $R_{RT/SYNC}$ Values. 3.3V Output

FREQUENCY	R_T/SYNC	EFFICIENCY $V_{VIN1/2}$ = 12V	$V_{IN(MAX)}$†	L*	C*	C + L
1.2MHz	20.5k	79.0%	16	1.5µH	22µH	63mm^2
1.0MHz	26.7k	80.9%	18	2.2µH	47µH	66mm^2
750kHz	38.3k	81.2%	22	3.3µH	47µF	66mm^2
500kHz	61.9k	82.0%	24	4.7µH	47µF	66mm^2
250kHz	133k	83.9%	24	10µH	100µF	172mm^2

†$V_{IN(MAX)}$ is defined as the highest input voltage that maintains constant output voltage ripple.
*Inductor and capacitor values chosen for stability and constant ripple current.

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duty cycle. The duty cycle is the fraction of time that the internal switch is on during a clock cycle. Unlike most fixed frequency regulators, the LT3501 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C3 in Figure 1) to fully saturate the output switch. Forced switch-off for a minimum time will only occur at the end of a clock cycle when the boost capacitor needs to be recharged. This operation has the same effect as lowering the clock frequency for a fixed off-time, resulting in a higher duty cycle and lower minimum input voltage. The resultant duty cycle depends on the charging times of the boost capacitor and can be approximated by the following equation:

$$DC_{MAX} = \frac{1}{1+\frac{1}{B}}$$

where B is 3A divided by the typical boost current from the Electrical Characteristics table.

This leads to a minimum input voltage of:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_D}{DC_{MAX}} - V_D + V_{SW}$$

where V_{SW} is the voltage drop of the internal switch.

Figure 3 shows a typical graph of minimum input voltage vs load current for the 3.3V and 1.8V application on the first page of this data sheet. The maximum input voltage is determined by the absolute maximum ratings of the V_{IN} and BST pins and by the frequency and minimum duty cycle. The minimum duty cycle is defined as :

$DC_{MIN} = t_{ON(MIN)} \bullet Frequency$

Maximum input voltage as:

$$V_{IN(MAX)} = \frac{V_{OUT} + V_D}{DC_{MIN}} - V_D + V_{SW}$$

Note that the LT3501 will regulate if the input voltage is taken above the calculated maximum voltage as long as maximum ratings of the V_{IN} and BST pins are not violated. However operation in this region of input voltage will exhibit pulse skipping behavior.

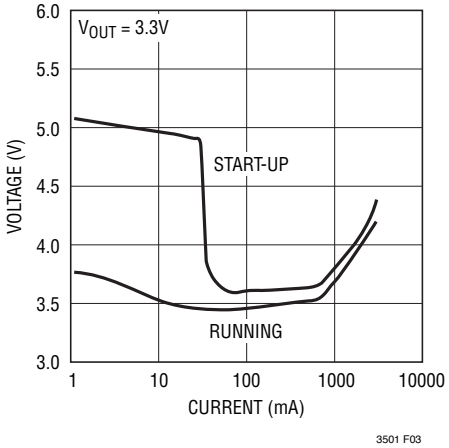

Figure 3. Minimum Input Voltage vs Load Current

Example:

V_{OUT} = 3.3V, I_{OUT} = 1A, Frequency = 1MHz, Temperature = 25°C

V_{SW} = 0.1V, B = 50 (from from boost characteristics specification), V_D = 0.4V, $t_{ON(MIN)}$ = 200ns

$$DC_{MAX} = \frac{1}{1+\frac{1}{50}} = 98\%$$

$$V_{IN(MIN)} = \frac{3.3+0.4}{0.98} - 0.4 + 0.1 = 3.48V$$

$$DC_{MIN} = t_{MIN(ON)} \bullet f = 0.200$$

$$V_{IN(MAX)} = \frac{3.3+0.4}{0.200} - 0.4 + 0.1 = 18.2V$$

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{V_{IN} \bullet f}$$

where f is frequency in MHz and L is in µH.

With this value the maximum load current will be ~3A, independent of input voltage. The inductor's RMS current rating must be greater than your maximum load current

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and its saturation current should be about 30% higher. To keep efficiency high, the series resistance (DCR) should be less than 0.05Ω.

For applications with a duty cycle of about 50%, the inductor value should be chosen to obtain an inductor ripple current less than 40% of peak switch current.

Of course, such a simple design guide will not always result in the optimum inductor for your application. A larger value provides a slightly higher maximum load current, and will reduce the output voltage ripple. If your load is lower than 2.5A, then you can decrease the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3501 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3501 will deliver depends on the current limit, the inductor value, switch frequency, and the input and output voltages. The inductor is chosen based on output current requirements, output voltage ripple requirements, size restrictions and efficiency goals.

When the switch is off, the inductor sees the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC)(V_{OUT}+V_D)}{L \bullet f}$$

where f is the switching frequency of the LT3501 and L is the value of the inductor. The peak inductor and switch current is

$$I_{SW(PK)} = I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3501's switch current limit I_{LIM}. I_{LIM} is 3.5A over the entire duty cycle range. The maximum output current is a function of the chosen inductor value:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} = 3.5 - \frac{\Delta I_L}{2}$$

If the inductor value is chosen so that the ripple current is small, then the available output current will be near the switch current limit.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors and choose one to meet cost or space goals. Then use these equations to check that the LT3501 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $I_L/2$ as calculated above.

Figure 4 illustrates the inductance value needed for a 3.3V output with a maximum load capability of 3A. Referring to Figure 4, an inductor value between 3.3µH and 4.7µH will be sufficient for a 15V input voltage and a switch frequency of 750kHz. There are several graphs in the Typical Performance Characteristics section of this data sheet that show inductor selection as a function of input voltage and switch frequency for several popular output voltages and output ripple currents. Also, low inductance

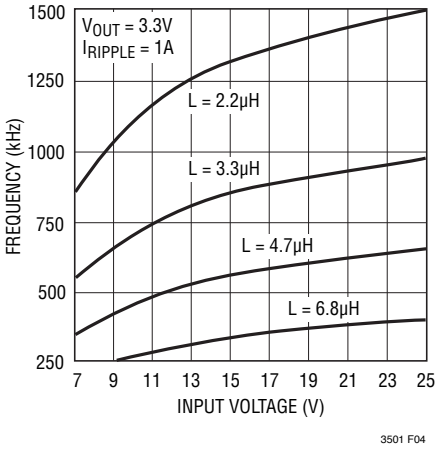

Figure 4. Inductor Values for 3A Maximum Load Current vs Frequency and Input Voltage

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may result in discontinuous mode operation, which is okay, but further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology Application Note 44. Finally, for duty cycles greater than 50% (V_{OUT}/V_{IN} > 0.5), there is a minimum inductance required to avoid subharmonic oscillations. See Application Note 19 for more information.

Input Capacitor Selection

Bypass the inputs of the LT3501 circuit with a 4.7µF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type can be used if there is additional bypassing provided by bulk electrolytic or tantalum capacitors. The following paragraphs describe the input capacitor considerations in more detail.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3501 and to force this very high frequency switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively, and it must have an adequate ripple current rating. With two switchers operating at the same frequency but with different phases and duty cycles, calculating the input capacitor RMS current is not simple. However, a conservative value is the RMS input current for the channel that is delivering most power ($V_{OUT} \bullet I_{OUT}$). This is given by:

$$I_{CIN(RMS)} = \frac{I_{OUT}\sqrt{V_{OUT} \bullet (V_{IN} - V_{OUT})}}{V_{IN}} < \frac{I_{OUT}}{2}$$

and is largest when $V_{IN} = 2V_{OUT}$ (50% duty cycle). As the second, lower power channel draws input current, the input capacitor's RMS current actually decreases as the out-of-phase current cancels the current drawn by the higher power channel. Considering that the maximum load current from a single channel is ~3A, RMS ripple current will always be less than 1.5A.

The frequency, V_{IN} to V_{OUT} ratio, and maximum load current requirement of the LT3501 along with the input supply source impedance, determine the energy storage requirements of the input capacitor. Determine the worst-case condition for input ripple current and then size the input capacitor such that it reduces input voltage ripple to an acceptable level. Typical values for input capacitors run from 10µF at low frequencies to 2.2µF at higher frequencies. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors make them the preferred choice. The low ESR results in very low voltage ripple and the capacitors can handle plenty of ripple current. They are also comparatively robust and can be used in this application at their rated voltage. X5R and X7R types are stable over temperature and applied voltage, and give dependable service. Other types (Y5V and Z5U) have very large temperature and voltage coefficients of capacitance, so they may have only a small fraction of their nominal capacitance in your application. While they will still handle the RMS ripple current, the input voltage ripple may become fairly large, and the ripple current may end up flowing from your input supply or from other bypass capacitors in your system, as opposed to being fully sourced from the local input capacitor. An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1µF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10µF will be required to meet the ESR and ripple current requirements. Because the input capacitor is likely to see high surge currents when the input source is applied, tantalum capacitors should be surge rated. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the V_{IN} and GND pins on the IC for optimal noise immunity.

When the LT3501's input supplies are operated at different input voltages, an input capacitor sized for that channel should be placed as close as possible to the respective V_{IN} pins.

A final caution regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example by plugging the circuit into a live power source) this tank can ring, doubling the input voltage and damaging the LT3501. The solution is to

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either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see Application Note 88.

Output Capacitor Selection

Typically step-down regulators are easily compensated with an output crossover frequency that is one-tenth of the switching frequency. This means that the time that the output capacitor must supply the output load during a transient step is ~2 or 3 switching periods. With an allowable 5% drop in output voltage during the step, a good starting value for the output capacitor can be expressed by:

$$C_{VOUT} = \frac{\text{Max Load Step}}{\text{Frequency} \bullet 0.05 \bullet V_{OUT}}$$

Example:

V_{OUT} = 3.3V, Frequency = 1MHz, Max Load Step = 3A

$$C_{VOUT} = \frac{2}{1e6 \bullet 0.05 \bullet 3.3V} = 12\mu F$$

The calculated value is only a suggested starting value. Increase the value if transient response needs improvement or reduce the capacitance if size is a priority.

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order to satisfy transient loads and to stabilize the LT3501's control loop. The switching frequency of the LT3501 determines the value of output capacitance required. Also, the current mode control loop doesn't require the presence of output capacitor series resistance (ESR). For these reasons, you are free to use ceramic capacitors to achieve very low output ripple and small circuit size.

Estimate output ripple with the following equations:

$V_{RIPPLE} = \Delta I_L/(8f\ C_{OUT})$ for ceramic capacitors,

and

$V_{RIPPLE} = \Delta I_L$ ESR for electrolytic capacitors (tantalum and aluminum)

where ΔI_L is the peak-to-peak ripple current in the inductor.

The RMS content of this ripple is very low, and the RMS current rating of the output capacitor is usually not of concern.

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor is transferred to the output, you would like the resulting voltage step to be small compared to the regulation voltage. For a 5% overshoot, this requirement becomes

$$C_{OUT} > 10\ L\left(\frac{I_{LIM}}{V_{OUT}}\right)^2$$

Finally, there must be enough capacitance for good transient performance. The last equation gives a good starting point. Alternatively, you can start with one of the designs in this data sheet and experiment to get the desired performance. This topic is covered more thoroughly in the section on loop compensation.

The high performance (low ESR), small size and robustness of ceramic capacitors make them the preferred type for LT3501 applications. However, all ceramic capacitors are not the same. As mentioned above, many of the high value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and temperature extremes. Because the loop stability and transient response depend on the value of C_{OUT}, you may not be able to tolerate this loss. Use X7R and X5R types. You can also use electrolytic capacitors. The ESRs of most aluminum electrolytics are too large to deliver low output ripple. Tantalum and newer, lower ESR organic electrolytic capacitors intended for power supply use, are suitable and the manufacturers will specify the ESR. The choice of capacitor value will be based on the ESR required for low ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give you similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 2 lists several capacitor vendors.

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Table 2

VENDOR	TYPE	SERIES
Taiyo Yuden	Ceramic X5R, X7R	
AVX	Ceramic X5R, X7R Tantalum	
Kemet	Tantalum TA Organic AL Organic	T491, T494, T495 T520 A700
Sanyo	TA/AL Organic	POSCAP
Panasonic	AL Organic	SP CAP
TDK	Ceramic X5R, X7R	

Catch Diode

The diode D1 conducts current only during switch off-time. Use a Schottky diode to limit forward-voltage drop to increase efficiency. The Schottky diode must have a peak reverse voltage that is equal to regulator input voltage and sized for average forward current in normal operation. Average forward current can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}}{V_{IN}} \bullet (V_{IN} - V_{OUT})$$

The only reason to consider a larger diode is the worst-case condition of a high input voltage and shorted output. With a shorted condition, diode current will increase to a typical value of 4A, determined by the peak switch current limit of the LT3501. This is safe for short periods of time, but it would be prudent to check with the diode manufacturer if continuous operation under these conditions can be tolerated.

BST Pin Considerations

The capacitor and diode tied to the BST pin generate a voltage that is higher than the input voltage. In most cases a 0.47µF capacitor and fast switching diode (such as the CMDSH-3 or FMMD914) will work well. Almost any type of film or ceramic capacitor is suitable, but the ESR should be <1Ω to ensure it can be fully recharged during the off-time of the switch. The capacitor value can be approximated by:

$$C_{BST} = \frac{I_{OUT(MAX)} \bullet DC}{B \bullet \left(V_{OUT} - V_{BST(MIN)}\right) \bullet f}$$

where $I_{OUT(MAX)}$ is the maximum load current, and $V_{BST(MIN)}$ is the minimum boost voltage to fully saturate the switch.

Figure 5 shows four ways to arrange the boost circuit. The BST pin must be more than 1.4V above the SW pin for full efficiency. Generally, for outputs of 3.3V and higher the standard circuit (Figure 5a) is the best. For outputs between 2.8V and 3.3V, replace the D2 with a small Schottky diode such as the PMEG4005. For lower output voltages the boost diode can be tied to the input (Figure 5b). The circuit in Figure 5a is more efficient because the BST pin current comes from a lower voltage source. Figure 5c shows the boost voltage source from available DC sources that are greater than 3V. The highest efficiency is attained by choosing the lowest boost voltage above 3V. For example, if you are generating 3.3V and 1.8V and the 3.3V is on whenever the 1.8V is on, the 1.8V boost diode can be connected to the 3.3V output. In any case, you must also be sure that the maximum voltage at the BST pin is less than the maximum specified in the Absolute Maximum Ratings section.

The boost circuit can also run directly from a DC voltage that is higher than the input voltage by more than 3V, as in Figure 5d. The diode is used to prevent damage to the LT3501 in case V_X is held low while V_{IN} is present. The circuit saves several components (both BST pins can be tied to D2). However, efficiency may be lower and dissipation in the LT3501 may be higher. Also, if V_X is absent, the LT3501 will still attempt to regulate the output, but will do so with very low efficiency and high dissipation because the switch will not be able to saturate, dropping 1.5V to 2V in conduction.

The minimum input voltage of an LT3501 application is limited by the minimum operating voltage (<3V) and by the maximum duty cycle as outlined above. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3501 is turned on with its SS pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on

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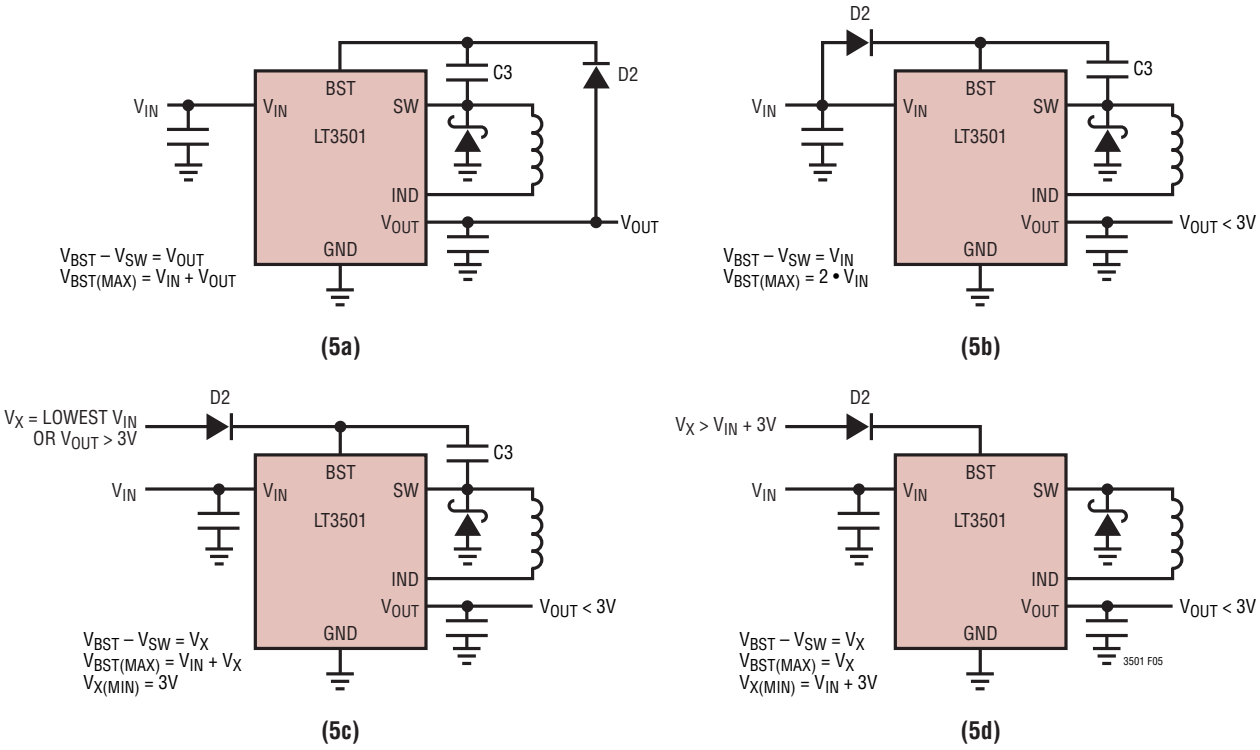


Figure 5. BST Pin Considerations

input and output voltages, and on the arrangement of the boost circuit. The Typical Performance Characteristics section shows plots of the minimum load current to start and to run as a function of input voltage for 3.3V and 5V outputs. In many cases the discharged output capacitor will present a load to the switcher which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly. Use a Schottky diode for the lowest start-up voltage.

Frequency Compensation

The LT3501 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3501 does not require the ESR of the output capacitor for stability so you are free to use ceramic capacitors to achieve low output ripple and small circuit size.

Frequency compensation is provided by the components tied to the V_C pin. Generally a capacitor and a resistor in series to ground determine loop gain. In addition, there is a lower value capacitor in parallel. This capacitor is not part of the loop compensation but is used to filter noise at the switching frequency.

Loop compensation determines the stability and transient performance. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 6 shows an equivalent circuit for the LT3501 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that

APPLICATIONS INFORMATION

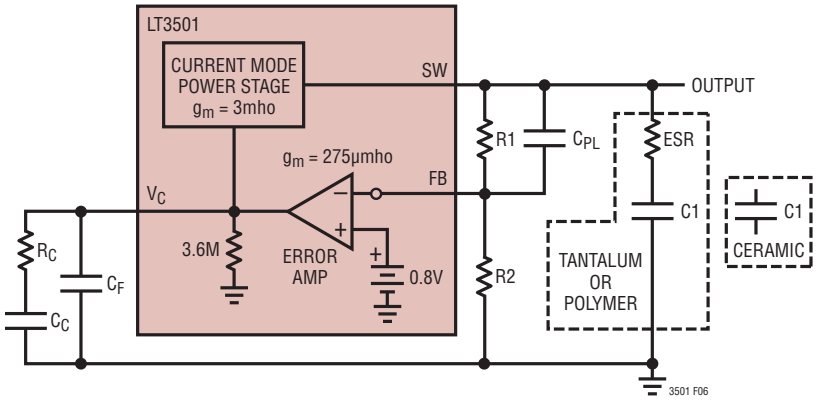


Figure 6. Model for Loop Response

the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the output capacitor ESR or from a resistor in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response.

Synchronization

The R_T/SYNC pin can be used to synchronize the regulators to an external clock source. Driving the R_T/SYNC resistor with a clock source triggers the synchronization detection circuitry. Once synchronization is detected, the rising edge of SW1 will be synchronized to the rising edge of the R_T/SYNC pin signal. An AGC loop will adjust the internal oscillators to maintain a 180 degree phase between SW1 and SW2, and also adjust slope compensation to avoid subharmonic oscillation.

The synchronizing clock signal input to the LT3501 must have a frequency between 250kHz and 1.5MHz, a duty cycle between 20% and 80%, a low state below 0.5V and a high state above 1.6V. Synchronization signals outside of these parameters will cause erratic switching behavior. The R_T/SYNC resistor should be set such that the free running frequency ($(V_{RT/SYNC} – V_{SYNCLO})/R_{RT/SYNC}$) is approximately equal to the synchronization frequency. If the synchronization signal is halted, the synchronization detection circuitry will timeout in typically 10µs at which

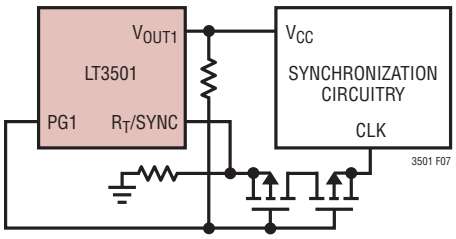


Figure 7. Synchronous Signal Powered from Regulator's Output

time the LT3501 reverts to the free-running frequency based on the current through R_T/SYNC. If the R_T/SYNC resistor is held above 1.6V at any time, switching will be disabled.

If the synchronization signal is not present during regulator start-up (for example, the synchronization circuitry is powered from the regulator output) the R_T/SYNC pin must see an equivalent resistance to ground between 15.4k and 133k until the synchronization circuitry is active for proper start-up operation.

If the synchronization signal powers up in an undetermined state (V_{OL}, V_{OH}, Hi-Z), connect the synchronization clock to the LT3501 as shown in Figure 7. The circuit as shown will isolate the synchronization signal when the output voltage is below 90% of the regulated output. The LT3501 will start-up with a switching frequency determined by the resistor from the R_T/SYNC pin to ground.

If the synchronization signal powers up in a low impedance state (V_{OL}), connect a resistor between the R_T/SYNC pin and the synchronizing clock. The equivalent resistance seen from the R_T/SYNC pin to ground will set the start-up frequency.

APPLICATIONS INFORMATION

If the synchronization signal powers up in a high impedance state (Hi-Z), connect a resistor from the R_T/SYNC pin to ground. The equivalent resistance seen from the R_T/SYNC pin to ground will set the start-up frequency.

If the synchronization signal changes between high and low impedance states during power-up (V_{OL}, Hi-Z), connect the synchronization circuitry to the LT3501 as shown in the Typical Applications section. This will allow the LT3501 to start-up with a switching frequency determined by the equivalent resistance from the R_T/SYNC pin to ground.

Shutdown and Undervoltage Lockout

Figure 8 shows how to add undervoltage lockout (UVLO) to the LT3501. Typically, UVLO is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

An internal comparator will force the part into shutdown below the minimum V_{IN1} of 2.8V. This feature can be used to prevent excessive discharge of battery-operated systems.

Since V_{IN2} supplies the output stage of channel 2 and is not monitored, care must be taken to insure that V_{IN2} is present before channel 2 is allowed to switch.

If an adjustable UVLO threshold is required, the SHDN pin can be used. The threshold voltage of the SHDN pin comparator is 1.28V. A 3µA internal current source

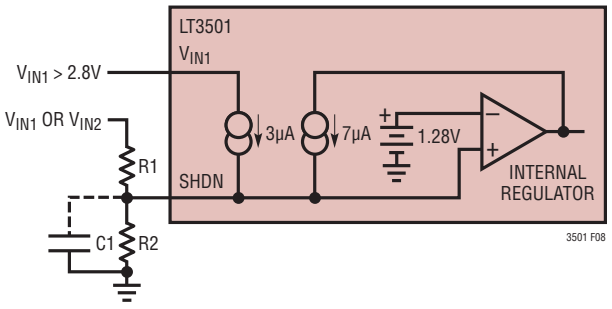


Figure 8. Undervoltage Lockout

defaults the open-pin condition to be operating (see Typical Performance Characteristics). Current hysteresis is added above the SHDN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R1 = \frac{V_H - V_L}{7\mu A}$$

$$R2 = \frac{1.28}{\frac{V_H - 1.28}{R1} + 3\mu A}$$

V_H = Turn-on threshold

V_L = Turn-off threshold

Example: switching should not start until the input is above 4.75V and is to stop if the input falls below 3.75V.

V_H = 4.75V

V_L = 3.75V

$$R1 = \frac{4.75 - 3.75}{7\mu A} \cong 143k$$

$$R2 = \frac{1.28}{\frac{4.75 - 1.28}{143k} + 3\mu A} \cong 47k$$

Keep the connections from the resistors to the SHDN pin short and make sure that the interplane or surface capacitance to switching nodes is minimized. If high resistor values are used, the SHDN pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

Soft-Start

The output of the LT3501 regulates to the lowest voltage present at either the SS pin or an internal 0.8V reference. A capacitor from the SS pin to ground is charged by an internal 3.25µA current source resulting in a linear output ramp from 0V to the regulated output whose duration is given by:

$$t_{RAMP} = \frac{C_{SS} \bullet 0.8V}{3.25\mu A}$$

APPLICATIONS INFORMATION

At power-up, a reset signal sets the soft-start latch and discharges both SS pins to approximately 0V to ensure proper start-up. When both SS pins are fully discharged the latch is reset and the internal 3.25µA current source starts to charge the SS pin.

When the SS pin voltage is below 50mV, the V_C pin is pulled low which disables switching. This allows the SS pin to be used as an individual shutdown for each channel.

As the SS pin voltage rises above 50mV, the V_C pin is released and the output is regulated to the SS voltage. When the SS pin voltage exceeds the internal 0.8V reference, the output is regulated to the reference. The SS pin voltage will continue to rise until it is clamped at 2V.

In the event of a V_{IN1} undervoltage lockout, the SHDN pin driven below 1.28V, or the internal die temperature exceeding its maximum rating during normal operation, the soft-start latch is set, triggering a start-up sequence.

In addition, if the load exceeds the maximum output switch current, the output will start to drop causing the V_C pin clamp to be activated. As long as the V_C pin is clamped, the SS pin will be discharged. As a result, the output will be regulated to the highest voltage that the maximum output current can support. For example, if a 6V output is loaded by 1Ω the SS pin will drop to 0.53V, regulating the output at 4V (4A • 1Ω). Once the overload condition is removed, the output will soft-start from the temporary voltage level to the normal regulation point.

Since the SS pin is clamped at 2V and has to discharge to 0.8V before taking control of regulation, momentary overload conditions will be tolerated without a soft-start recovery. The typical time before the SS pin takes control is:

$$t_{SS(CONTROL)} = \frac{C_{SS} \bullet 1.2V}{700\mu A}$$

Power Good Indicators

The PG pin is the open-collector output of an internal comparator. The comparator compares the FB pin voltage to 90% of the reference voltage with 30mV of hysteresis. The PG pin has a sink capability of 800µA when the FB pin is below the threshold and can withstand 25V when the threshold is exceeded. The PG pin is active (sink capability is reduced in shutdown and undervoltage lockout mode) as long as the V_{IN1} pin voltage exceeds 1V.

Output Tracking/Sequencing

Complex output tracking and sequencing between channels can be implemented using the LT3501's SS and PG pins. Figure 9 shows several configurations for output tracking/sequencing for a 3.3V and 1.8V application.

Independent soft-start for each channel is shown in Figure 9a. The output ramp time for each channel is set by the soft-start capacitor as described in the soft-start section.

Ratiometric tracking is achieved in Figure 9b by connecting both SS pins together. In this configuration, the SS pin source current is doubled (6.5µA) which must be taken into account when calculating the output rise time.

By connecting a feedback network from V_{OUT1} to the SS2 pin with the same ratio that sets V_{OUT2} voltage, absolute tracking shown in Figure 9c is implemented. The minimum value of the top feedback resistor (R1) should be set such that the SS pin can be driven all the way to ground with 700µA of sink current when V_{OUT1} is at its regulated voltage. In addition, a small V_{OUT2} voltage offset will be present due to the SS2 3.25µA source current. This offset can be corrected for by slightly reducing the value of R2.

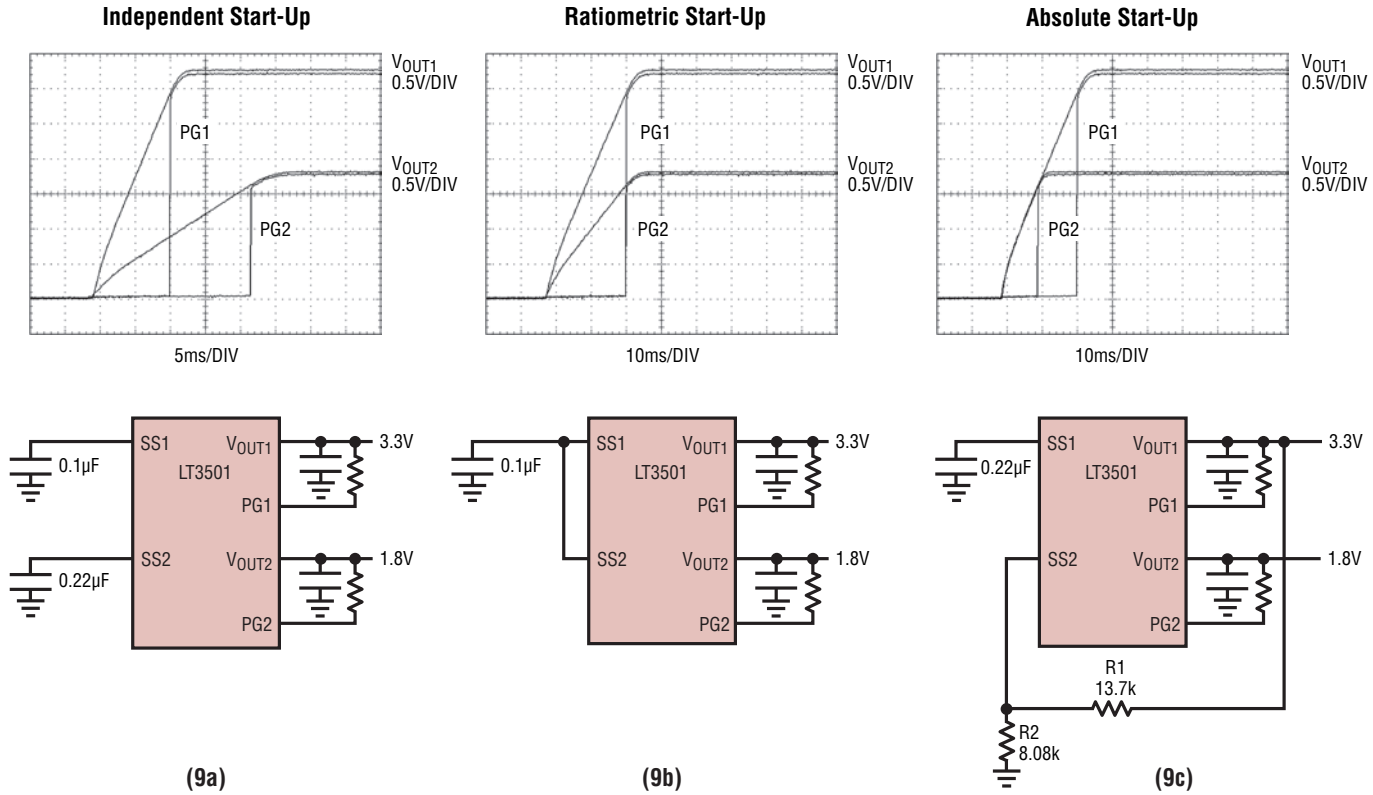
Figure 9d illustrates output sequencing. When V_{OUT1} is within 10% of its regulated voltage, PG1 releases the SS2 soft-start pin allowing V_{OUT2} to soft-start. In this case PG1 will be pulled up to 2V by the SS pin. If a greater voltage is needed for PG1 logic, a pull-up resistor to V_{OUT1} can be used. This will decrease the soft-start ramp time and increase tolerance to momentary shorts.

If precise output ramp up and down is required, drive the SS pins as shown in Figure 9e. The minimum value of resistor (R3) should be set such that the SS pin can be driven all the way to ground with 700µA of sink current during power-up and fault conditions.

Multiple Input Voltages

For applications requiring large inductors due to high V_{IN} to V_{OUT} ratios, a 2-stage step-down approach may reduce

APPLICATIONS INFORMATION



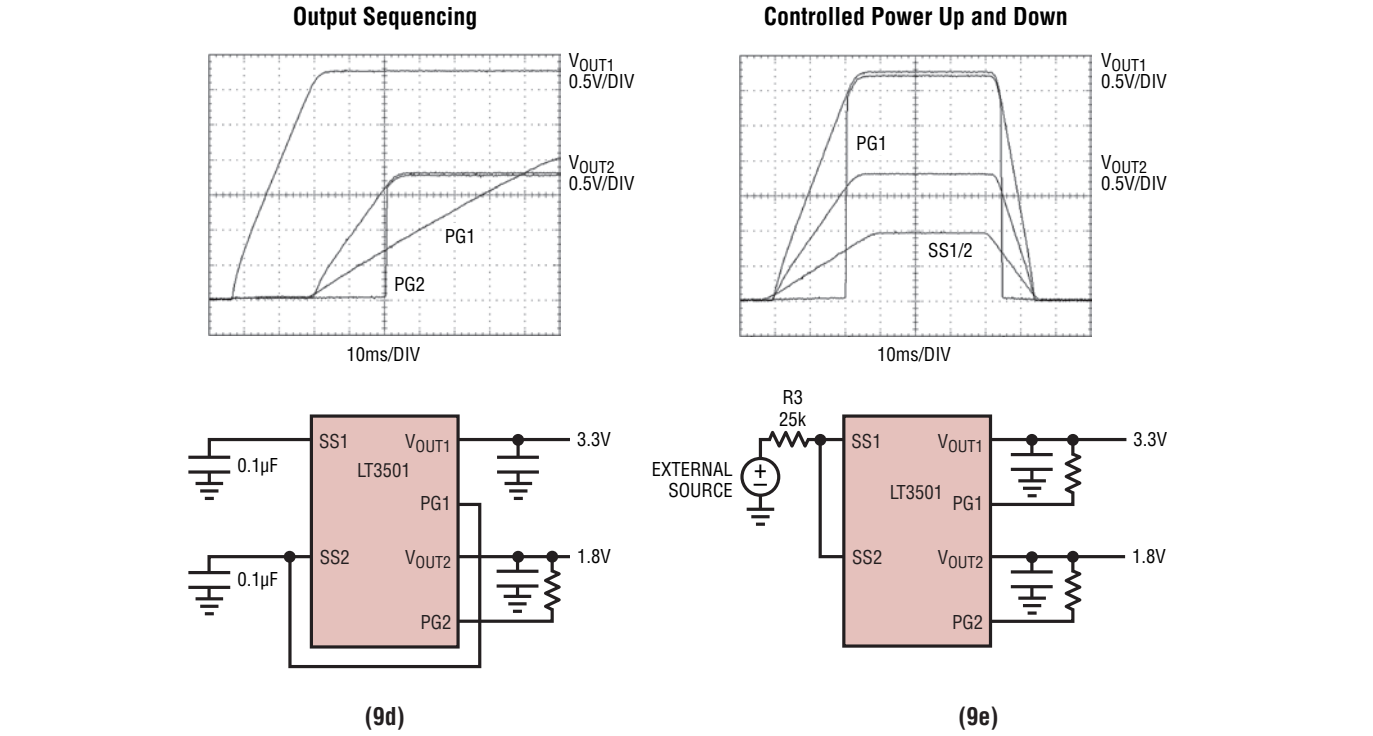


Figure 9

APPLICATIONS INFORMATION

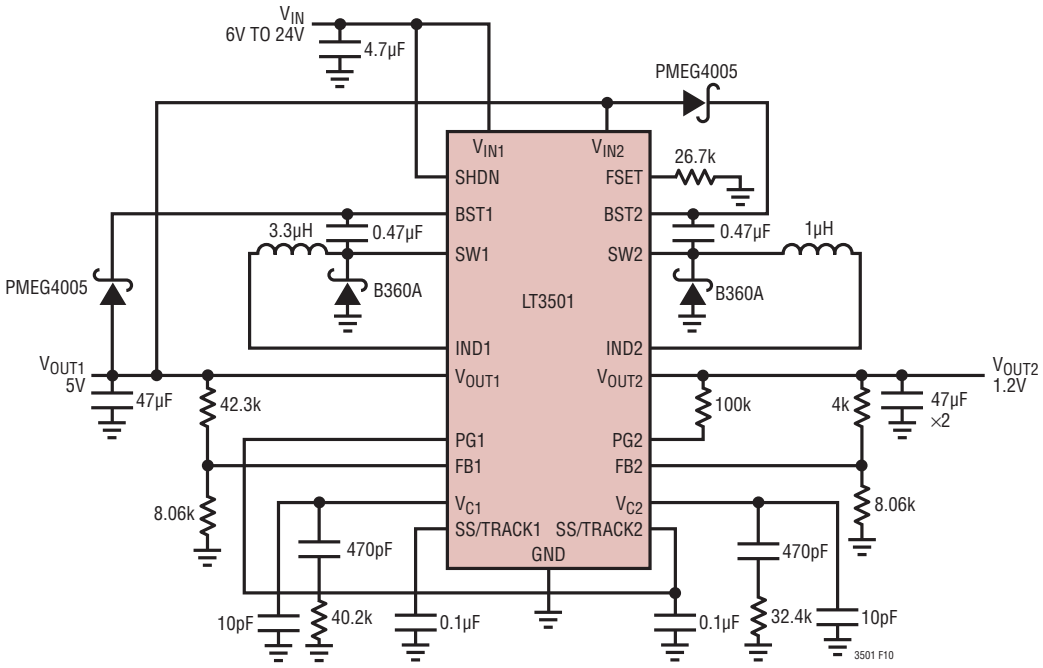


Figure 10. 5V and 1.2V 2-Stage Step-Down Converter with Output Sequencing

inductor size by allowing an increase in frequency. A dual step-down application (Figure 10) steps down the input voltage (V_{IN1}) to the highest output voltage then uses that voltage to power the second output (V_{IN2}). V_{OUT1} must be able to provide enough current for its output plus V_{OUT2} maximum load. Note that the V_{OUT1} must be above V_{IN2} minimum input voltage (2V) when the second channel starts to switch. Delaying channel 2 can be accomplished by either independent soft-start capacitors or sequencing with the PG1 output.

For example, assume a maximum input of 24V:

V_{IN} = 24V, V_{OUT1} = 5V at 1.5A and V_{OUT2} = 1.2V at 1.5A

$$\text{Frequency (Hz)} \le \frac{V_{OUT} + V_D}{\dfrac{V_{IN} - V_{SW} + V_D}{t_{MIN(ON)}}}$$

$$L \ge \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{V_{IN} \bullet f}$$

Single step-down:

$$\text{Frequency (Hz)} \le \frac{1.2 + 0.6}{\dfrac{24 - 0.4 + 0.6}{190\text{ns}}} = 392\text{kHz}$$

$$L1 = \frac{(24 - 5) \bullet 5}{24 \bullet 392\text{kHz}} \ge 10\mu\text{H}$$

$$L2 = \frac{(24 - 1.2) \bullet 1.2}{24 \bullet 392\text{kHz}} \ge 2.7\mu\text{H}$$

2-Stage Step-Down:

$$\text{Frequency} \le \frac{5 + 0.6}{\dfrac{24 - 0.4 + 0.6}{190\text{ns}}} = 1.2\text{MHz}$$

$$\text{Max Frequency} = 1.2\text{MHz}$$

$$L1 = \frac{(24 - 5) \bullet 5}{24 \bullet 1.2\text{MHz}} \ge 3.3\mu\text{H}$$

$$L2 = \frac{(5 - 1.2) \bullet 1.2}{5 \bullet 1.2\text{MHz}} \ge 0.76\mu\text{H}$$

APPLICATIONS INFORMATION

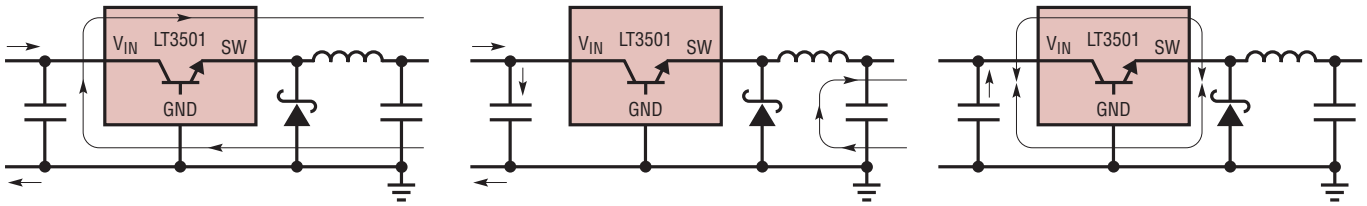


Figure 11. Subtracting the Current When the Switch Is On (11a) from the Current When the Switch is Off (11b) Reveals the Path of the High Frequency Switching Current (11c). Keep This Loop Small. The Voltage on the SW and BST Traces Will Also Be Switched; Keep These Traces as Short as Possible. Finally, Make Sure the Circuit Is Shielded with a Local Ground Plane

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 11 shows the high di/dt paths in the buck regulator circuit.

Note that large switched currents flow in the power switch, the catch diode and the input capacitor. The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board and their connections should be made on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor C2. Additionally, the SW and BST traces should be kept as short as possible. The topside metal from the DC964A demonstration board in Figure 12 illustrates proper component placement and trace routing.

Thermal Considerations

The PCB must also provide heat sinking to keep the LT3501 cool. The exposed metal on the bottom of the package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3501.

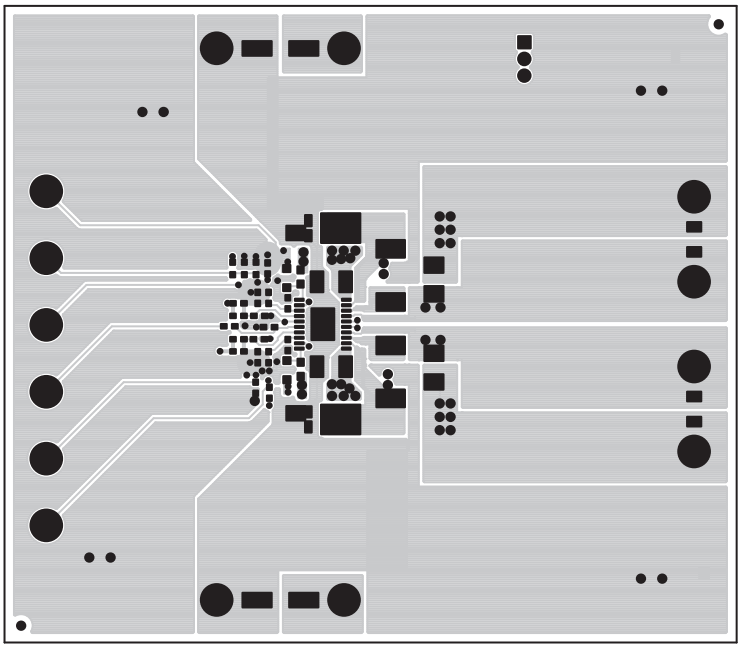


Figure 12. Topside PCB Layout DC964A

APPLICATIONS INFORMATION

Place additional vias near the catch diodes. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can further reduce thermal resistance. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 45°C/W.

The power dissipation in the other power components such as catch diodes, boost diodes and inductors, cause additional copper heating and can further increase what the IC sees as ambient temperature. See the LT1767 data sheet's Thermal Considerations section.

Single, Low Ripple 6A Output

The LT3501 can generate a single, low ripple 6A output if the outputs of the two switching regulators are tied together and share a single output capacitor. By tying the two FB pins together and the two V_C pins together, the two channels will share the load current. There are several advantages to this 2-phase buck regulator. Ripple currents at the input and output are reduced, reducing voltage ripple and allowing the use of smaller, less expensive capacitors. Although two inductors are required, each will be smaller than the inductor required for a single-phase regulator. This may be important when there are tight height restrictions on the circuit.

There is one special consideration regarding the 2-phase circuit. When the difference between the input voltage and output voltage is less than 2.5V, then the boost circuits may prevent the two channels from properly sharing current. If, for example, channel 1 gets started first, it can supply the load current, while channel 2 never switches enough current to get its boost capacitor charged.

In this case, channel 1 will supply the load until it reaches current limit, the output voltage drops, and channel 2 gets started. Two solutions to this problem are shown in the Typical Applications section.

The single 3.3V/6A output converter generates a boost supply from either SW that will service both switch pins.

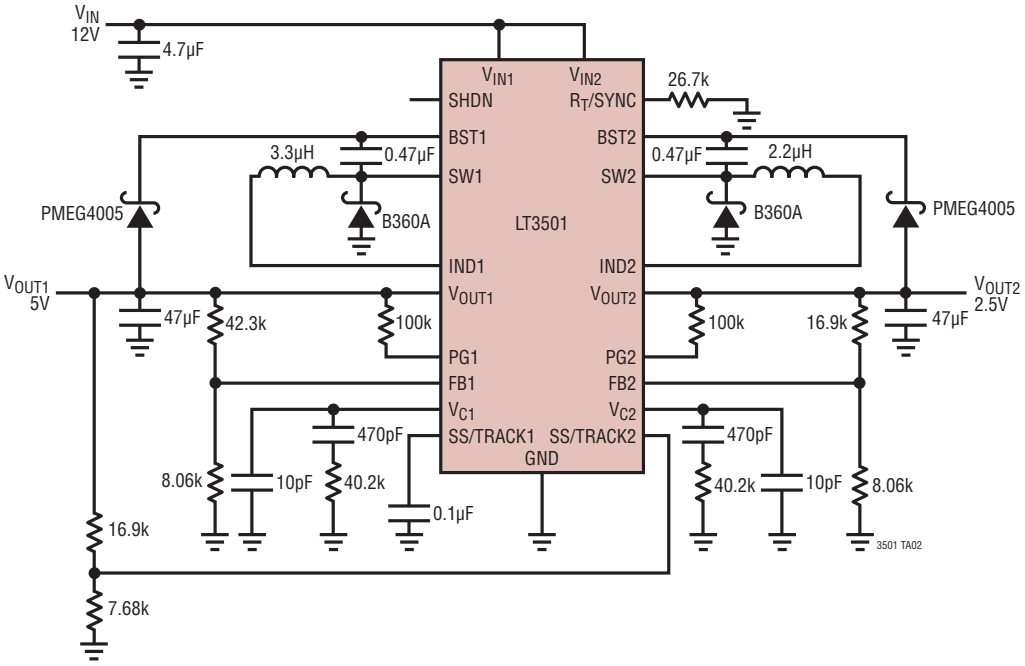
The synchronized 3.3V/12A output converter utilizes undervoltage lockout to prevent the start-up condition.

Other Linear Technology Publications

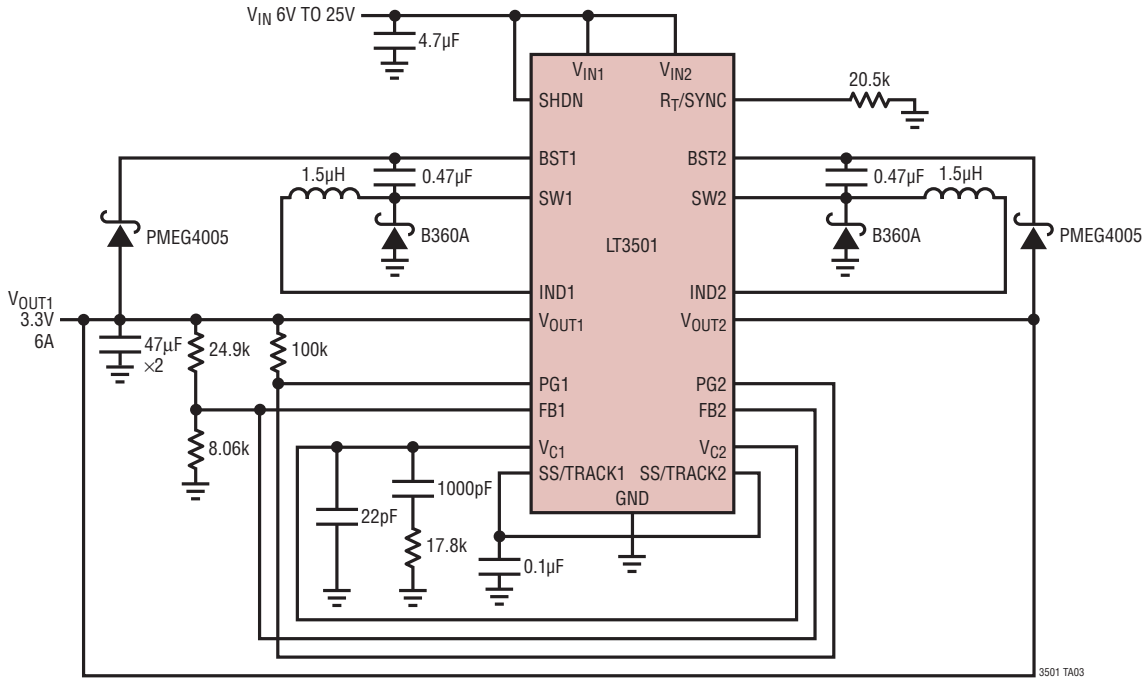
Application notes AN19, AN35 and AN44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note DN100 shows how to generate a dual (+ and –) output supply using a buck regulator.

TYPICAL APPLICATIONS

5V and 2.5V with Absolute Tracking

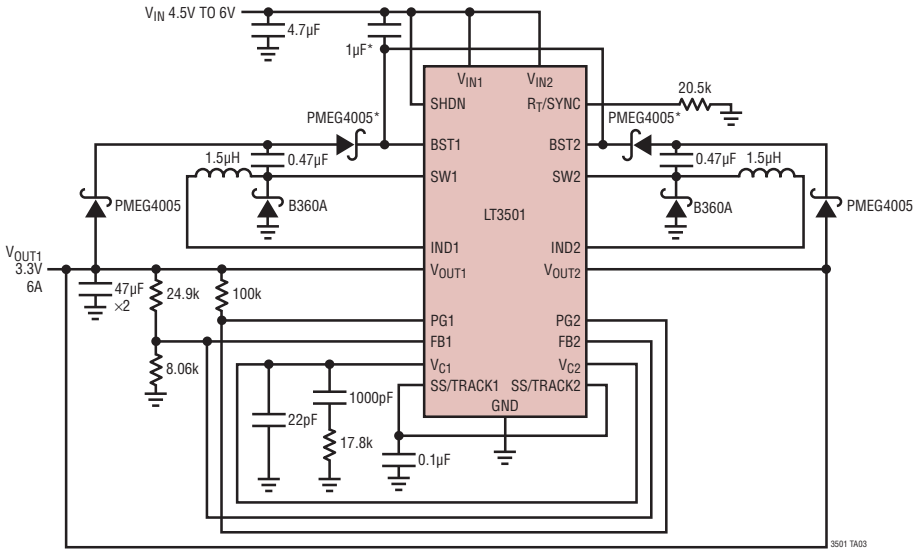


1.25MHz Single 3.3V/6A Low Ripple Output



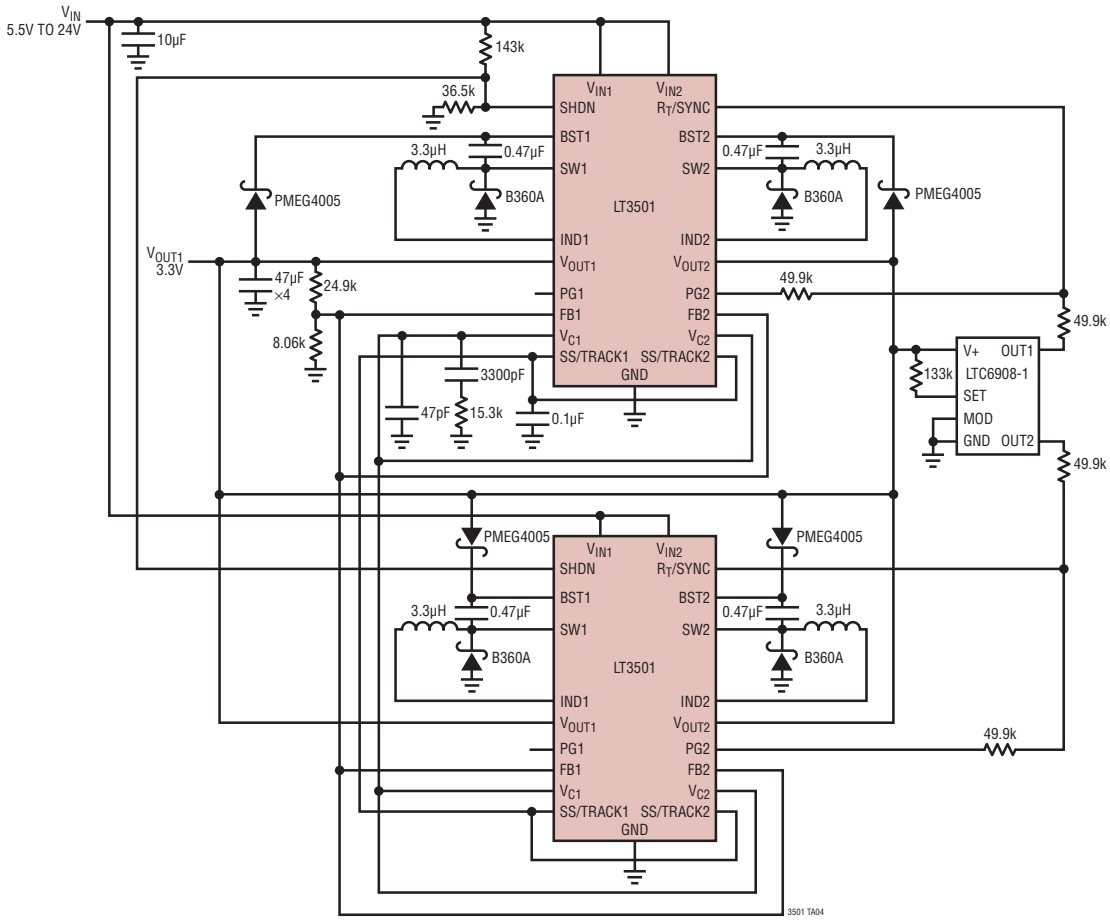
TYPICAL APPLICATIONS

1.25MHz Single 3.3V/6A Low Ripple Output



*ADDITIONAL COMPONENTS ADDED TO SHOW THE BOOST VOLTAGE WHEN V_{IN} <6V. THIS IS REQUIRED TO ENSURE LOAD SHARING BETWEEN THE TWO CHANNELS.

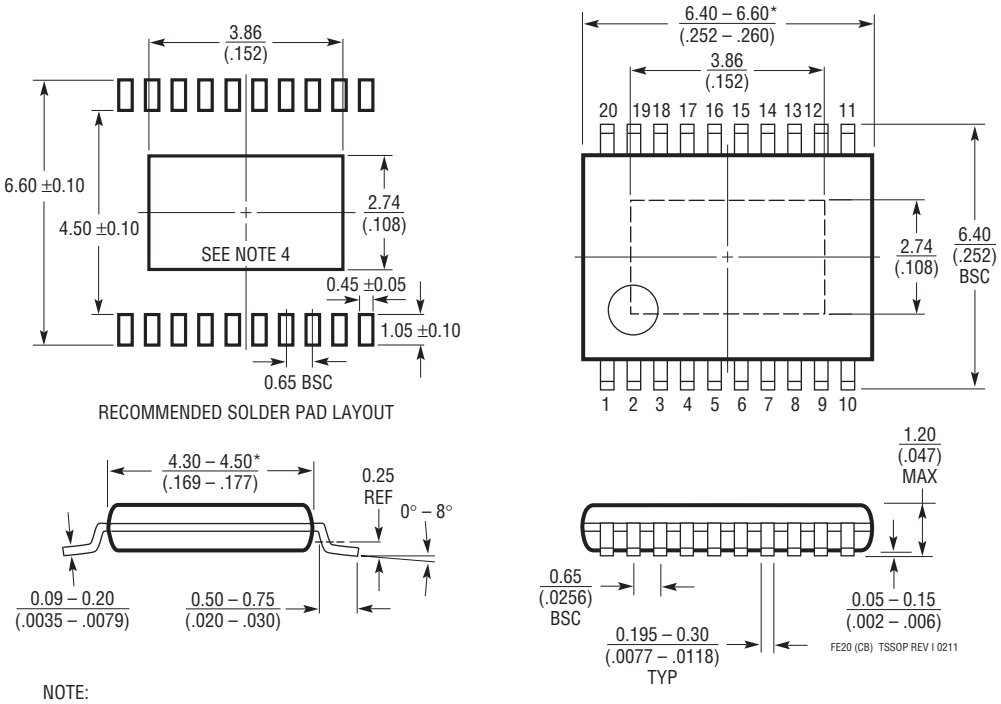
Dual LT3501 Synchronized 3.3V/12A Output, 3MHz Effective Switch Frequency



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	6/12	Part Marking clarification	2
		Solder pad clarification	28

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1766	60V, 1.2A (I_{OUT}), 200kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} = 25µA, 16-Lead TSSOPE Package
LT1933	500mA (I_{OUT}), 500kHz Step-Down Switching Regulator in SOT-23	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.6mA, I_{SD} < 1µA, ThinSOT™ Package
LT1936	36V, 1.4A (I_{OUT}), 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.9mA, I_{SD} < 1µA, 8-Lead MS8E Package
LT1940	Dual 25V, 1.4A (I_{OUT}), 1.1MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 3.8mA, I_{SD} < 30µA, 16-Lead TSSOPE Package
LT1976/LT1977	60V, 1.2A (I_{OUT}), 200kHz/500kHz High Efficiency Step-Down DC/DC Converters with Burst Mode® Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100µA, I_{SD} < 1µA, 16-Lead TSSOPE Package
LTC®3407/LTC3407-2	Dual 600mA/800mA, 1.5MHz/2.25MHz Synchronous Step-Down DC/DC Converters	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 3mm × 3mm DFN and 10-Lead MSE Packages
LT3434/LT3435	60V, 2.4A (I_{OUT}), 200kHz/500kHz High Efficiency Step-Down DC/DC Converters with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100µA, I_{SD} < 1µA, 16-Lead TSSOPE Package
LT3437	60V, 400mA (I_{OUT}), Micropower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 100µA, I_{SD} < 1µA, DFN Package
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, DFN Package
LT3505	36V, 1.2A (I_{OUT}), 3MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} < 2µA, 3mm × 3mm DFN and 8-Lead MSE Packages
LT3506/LT3506A	Dual 25V, 1.6A (I_{OUT}), 575kHz/1.1MHz High Efficiency Step-Down DC/DC Converters	V_{IN}: 3.6V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.8mA, I_{SD} < 30µA, 4mm × 5mm DFN Package
LT3510	Dual 25V, 3A (I_{OUT}), 1.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.5mA, I_{SD} < 1µA, 20-Lead TSSOPE Package
LTC3548	Dual 400mA/800mA, 2.25MHz Synchronous Step-Down DC/DC Converters	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 3mm × 3mm DFN and 10-Lead MSE Packages

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