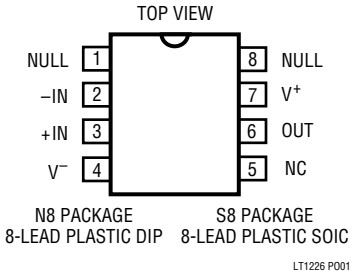
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
LT1226C ..... 0°C to 70°C
Maximum Junction Temperature
Plastic Package ..... 150°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1226CN8 LT1226CS8
S8 PART MARKING
1226

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.3	1.0	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	µA
e_n	Input Noise Voltage	f = 10kHz		2.6		nV/√Hz
i_n	Input Noise Current	f = 10kHz		1.5		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±12V Differential	24	40 15		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			–13	–12	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	94	103		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	94	110		dB
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 500Ω	50	150		V/mV
V_{OUT}	Output Swing	R_L = 500Ω	12.0	13.3		±V
I_{OUT}	Output Current	V_{OUT} = ±12V	24	40		mA
SR	Slew Rate	(Note 3)	250	400		V/µs
	Full Power Bandwidth	10V Peak, (Note 4)		6.4		MHz
GBW	Gain Bandwidth	f = 1MHz		1		GHz
t_r, t_f	Rise Time, Fall Time	A_{VCL} = +25,10% to 90%, 0.1V		5.5		ns
	Overshoot	A_{VCL} = +25, 0.1V		35		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		5.5		ns
t_s	Settling Time	10V Step, 0.1%, A_V = –25		100		ns
	Differential Gain	f = 3.58MHz, A_V = +25, R_L = 150Ω		0.7		%
	Differential Phase	f = 3.58MHz, A_V = +25, R_L = 150Ω		0.6		Deg
R_O	Output Resistance	A_{VCL} = +25, f = 1MHz		3.1		Ω
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		1.0	1.4	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	µA
	Input Voltage Range +		2.5	4		V
	Input Voltage Range –			–3	–2.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm2.5V$	94	103		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$ $V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	50	100 75		V/mV V/mV
V_{OUT}	Output Voltage	$R_L = 500\Omega$ $R_L = 150\Omega$	3.0 3.0	3.7 3.3		±V ±V
I_{OUT}	Output Current	$V_{OUT} = \pm3V$	20	40		mA
SR	Slew Rate	(Note 3)		250		V/µs
	Full Power Bandwidth	3V Peak, (Note 4)		13.3		MHz
GBW	Gain Bandwidth	f = 1MHz		700		MHz
t_r, t_f	Rise Time, Fall Time	A_{VCL} = +25, 10% to 90%, 0.1V		8		ns
	Overshoot	A_{VCL} = +25, 0.1V		25		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		8		ns
t_s	Settling Time	– 2.5V to 2.5V, 0.1%, $A_V = -24$		60		ns
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm15V$, (Note 2) $V_S = \pm$ 5V, (Note 2)		0.3 1.0	1.3 1.8	mV mV
	Input V_{OS} Drift			6		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm15V$ and $V_S = \pm5V$		100	600	nA
I_B	Input Bias Current	$V_S = \pm15V$ and $V_S = \pm5V$		4	9	µA
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$ and $V_S = \pm5V$, $V_{CM} = \pm2.5V$	92	103		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	92	110		dB
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 500\Omega$ $V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	35 35	150 100		V/mV V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 500\Omega$ $V_S = \pm5V$, $R_L = 500\Omega$ or 150Ω	12.0 3.0	13.3 3.3		±V ±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$ $V_S = \pm5V$, $V_{OUT} = \pm3V$	24 20	40 40		mA mA
SR	Slew Rate	$V_S = \pm15V$, (Note 3)	250	400		V/µs
I_S	Supply Current	$V_S = \pm15V$ and $V_S = \pm5V$		7	10.5	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

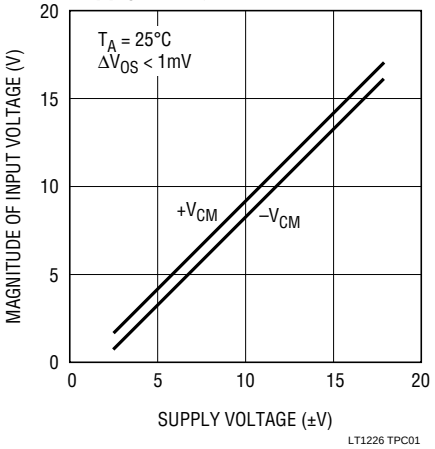
Note 2: Input offset voltage is tested with automated test equipment in <1 second.

Note 3: Slew rate is measured between ±10V on an output swing of ±12V on ±15V supplies, and ±2V on an output swing of ±3.5V on ±5V supplies.

Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

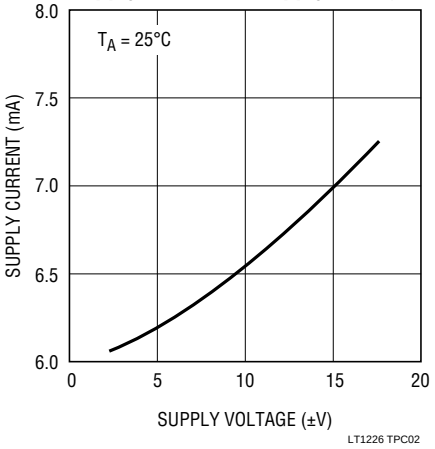
TYPICAL PERFORMANCE CHARACTERISTICS

Input Common Mode Range vs Supply Voltage



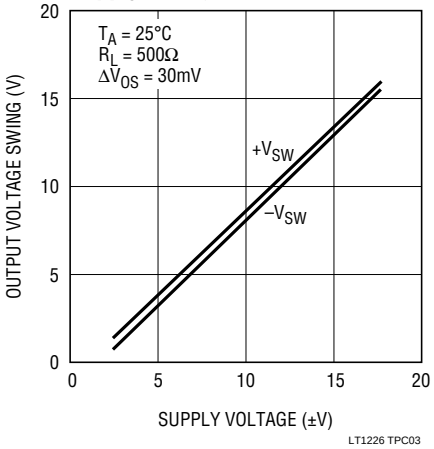
LT1226 TPC01

Supply Current vs Supply Voltage



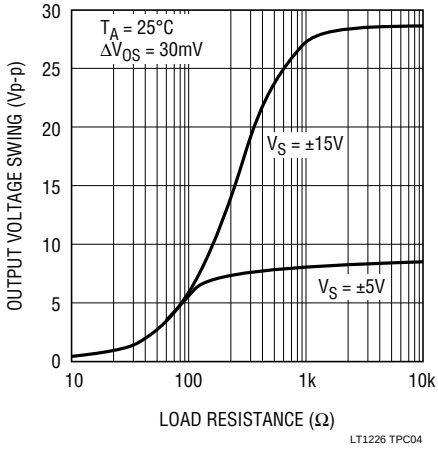
LT1226 TPC02

Output Voltage Swing vs Supply Voltage



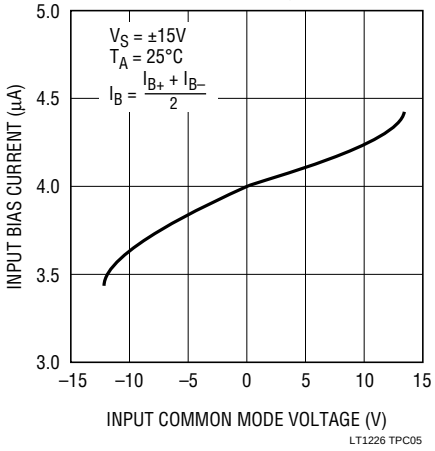
LT1226 TPC03

Output Voltage Swing vs Resistive Load



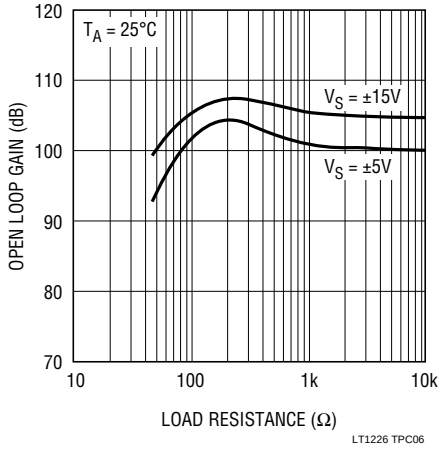
LT1226 TPC04

Input Bias Current vs Input Common Mode Voltage



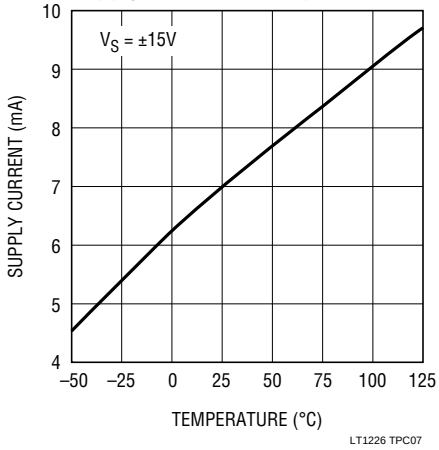
LT1226 TPC05

Open Loop Gain vs Resistive Load



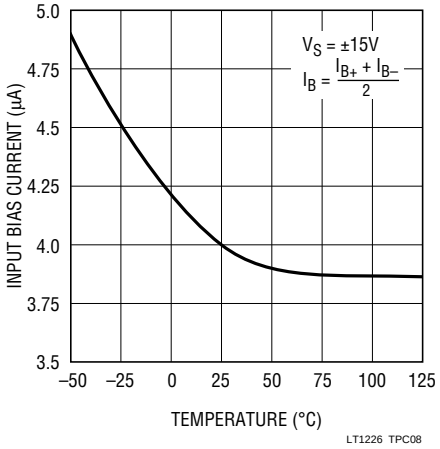
LT1226 TPC06

Supply Current vs Temperature



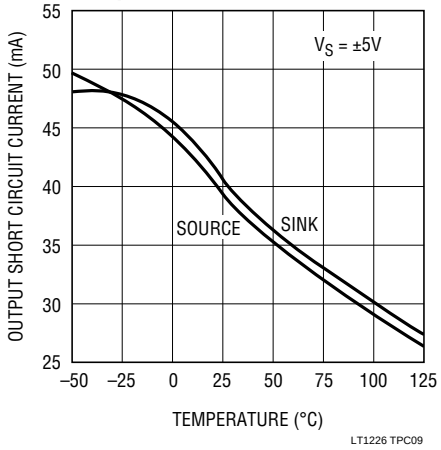
LT1226 TPC07

Input Bias Current vs Temperature



LT1226 TPC08

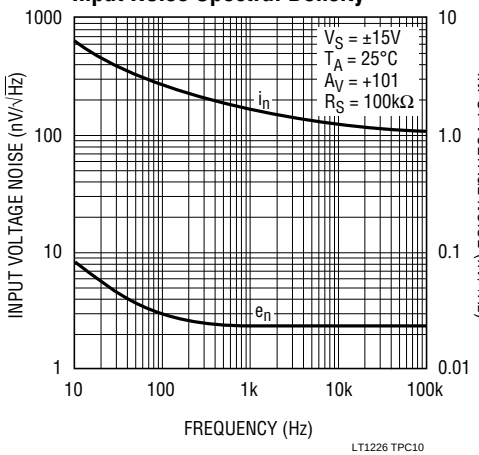
Output Short Circuit Current vs Temperature



LT1226 TPC09

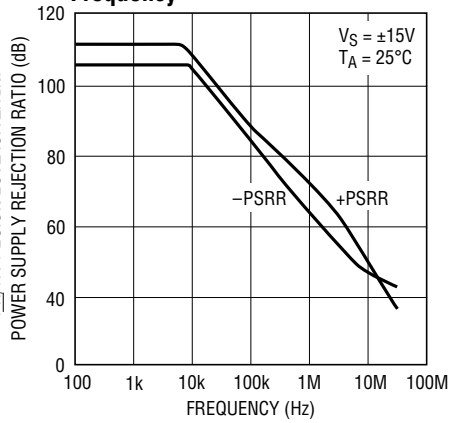
TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Spectral Density



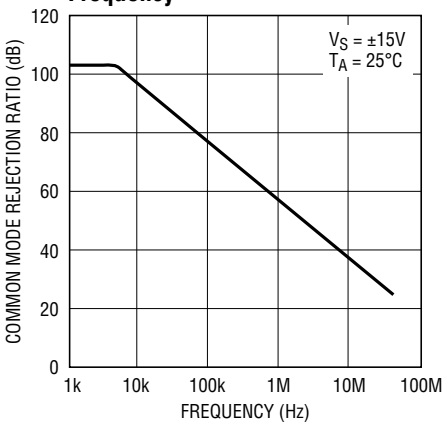
LT1226 TPC10

Power Supply Rejection Ratio vs Frequency



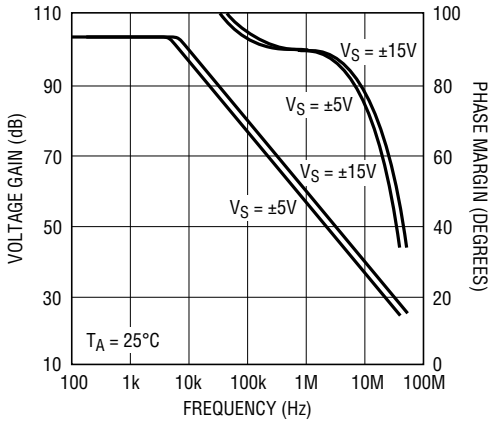
LT1226 TPC11

Common Mode Rejection Ratio vs Frequency



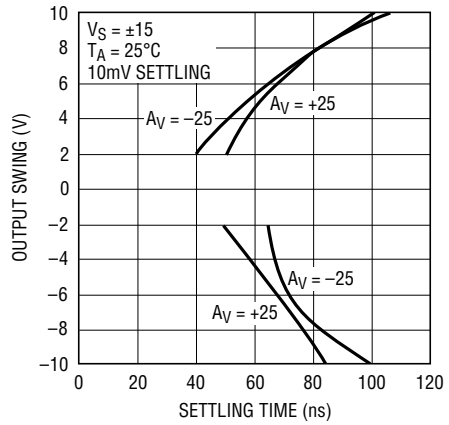
LT1226 TPC12

Voltage Gain and Phase vs Frequency



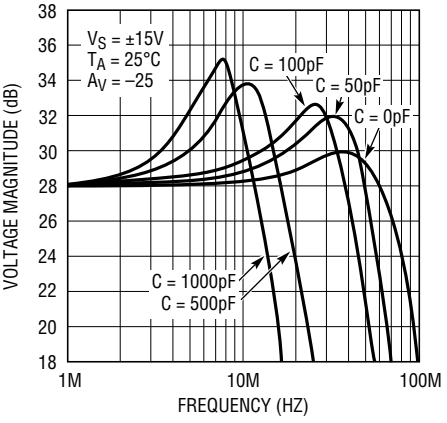
LT1226 TPC13

Output Swing vs Settling Time



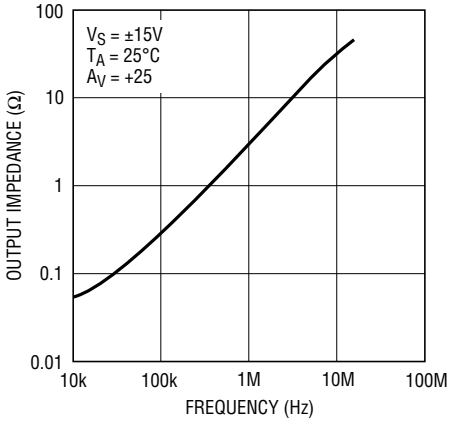
LTC1226 TPC14

Frequency Response vs Capacitive Load



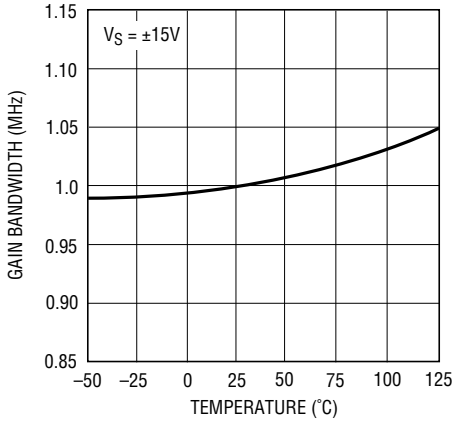
LT1226 TPC15

Closed Loop Output Impedance vs Frequency



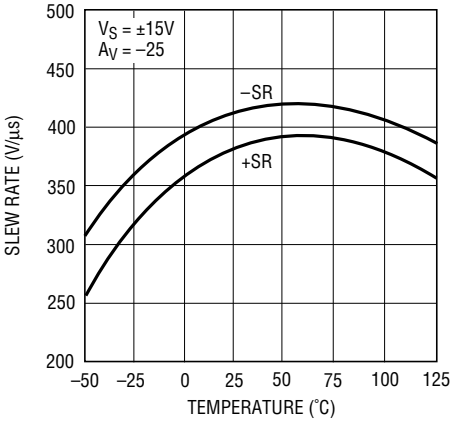
LT1226 TPC16

Gain Bandwidth vs Temperature



LT1226 TPC17

Slew Rate vs Temperature

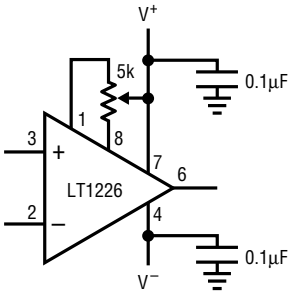


LT1226 TPC18

APPLICATIONS INFORMATION

The LT1226 may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the amplifier configuration is a noise gain of 25 or greater, and the nulling circuitry is removed. The suggested nulling circuit for the LT1226 is shown below.

Offset Nulling



LT1226 AI01

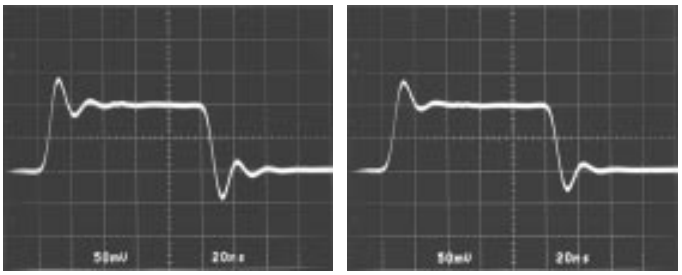
Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistors greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking. If feedback resistors greater than 5kΩ are used, a parallel capacitor of 5pF to 10pF should be used to cancel the input pole and optimize dynamic performance.

Transient Response

The LT1226 gain bandwidth is 1GHz when measured at 1MHz. The actual frequency response in a gain of +25 is considerably higher than 40MHz due to peaking caused by a second pole beyond the gain of 25 crossover point. This is reflected in the small signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of 25 response.

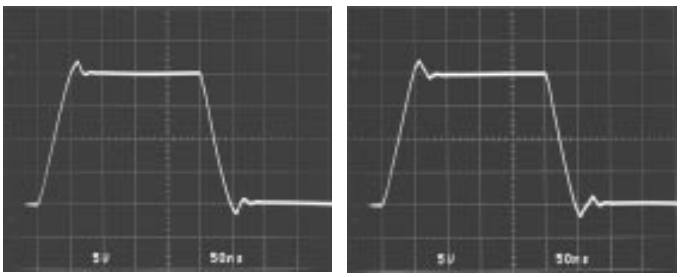
Small Signal, A_V = +25 **Small Signal, A_V = –25**



LT1226 AI02

The large signal response in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1226 so that the falling edge slew rate is enhanced which balances the noninverting slew rate response.

Large Signal, A_V = +25 **Large Signal, A_V = –25**



LT1226 AI03

Input Considerations

Resistors in series with the inputs are recommended for the LT1226 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

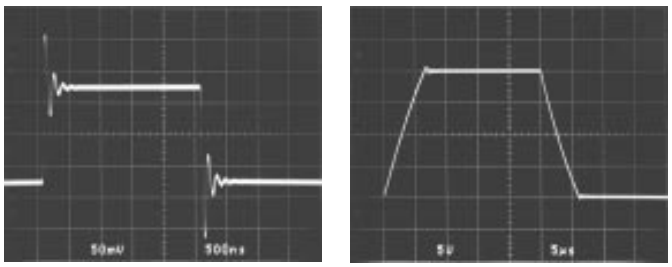
Capacitive Loading

The LT1226 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the

APPLICATIONS INFORMATION

frequency domain and in the transient response. The photo of the small signal response with 1000pF load shows 55% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited by the short circuit current.

A_V = –25, C_L = 1000pF **A_V = +25, C_L = 10,000pF**



LT1226 AI04

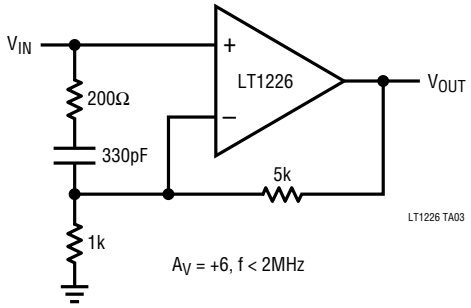
The LT1226 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

Compensation

The LT1226 has a typical gain bandwidth product of 1GHz which allows it to have wide bandwidth in high gain configurations (i.e., in a gain of 1000 it will have a bandwidth of about 1MHz). The amplifier is stable in a noise gain of 25 so the ratio of the output signal to the inverting input must be 1/25 or less. Straightforward gain configurations of +25 or –24 are stable, but there are a few configurations that allow the amplifier to be stable for lower signal gains (the noise gain, however, remains 25 or more). One example is the inverting amplifier shown in the typical applications sections below. The input signal has a gain of $-R_F/R_{IN}$ to the output, but it is easily seen that this configuration is equivalent to a gain of –24 as far as the amplifier is concerned. Lag compensation can also be used to give a low frequency gain less than 25 with a high frequency gain of 25 or greater. The example below has a DC gain of 6, but an AC gain of +31. The break frequency of the RC combination across the amplifier inputs should be at least a factor of 10 less than the gain bandwidth of the amplifier divided by the high frequency gain (in this case 1/10 of 1GHz/31 or 3MHz).

TYPICAL APPLICATIONS

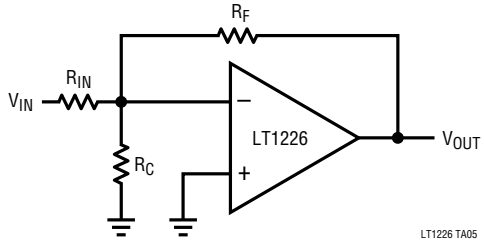
Lag Compensation



LT1226 TA03

A_V = +6, f < 2MHz

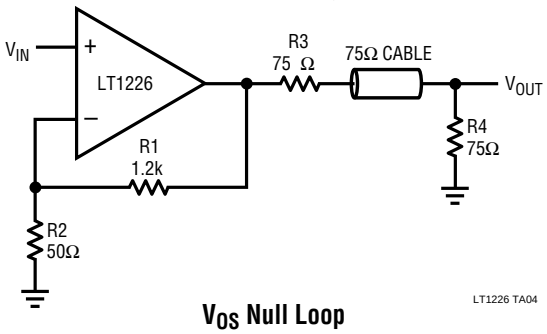
Compensation for Lower Closed-Loop Gains



LT1226 TA05

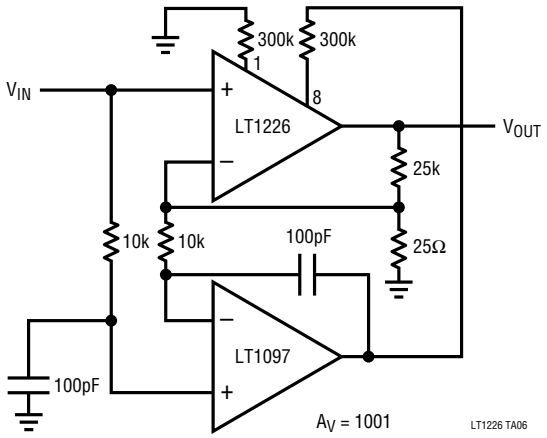
$$A_V = -\frac{R_F}{R_{IN}} ; R_F \geq 24 \times (R_{IN} \parallel R_C)$$

Cable Driving



LT1226 TA04

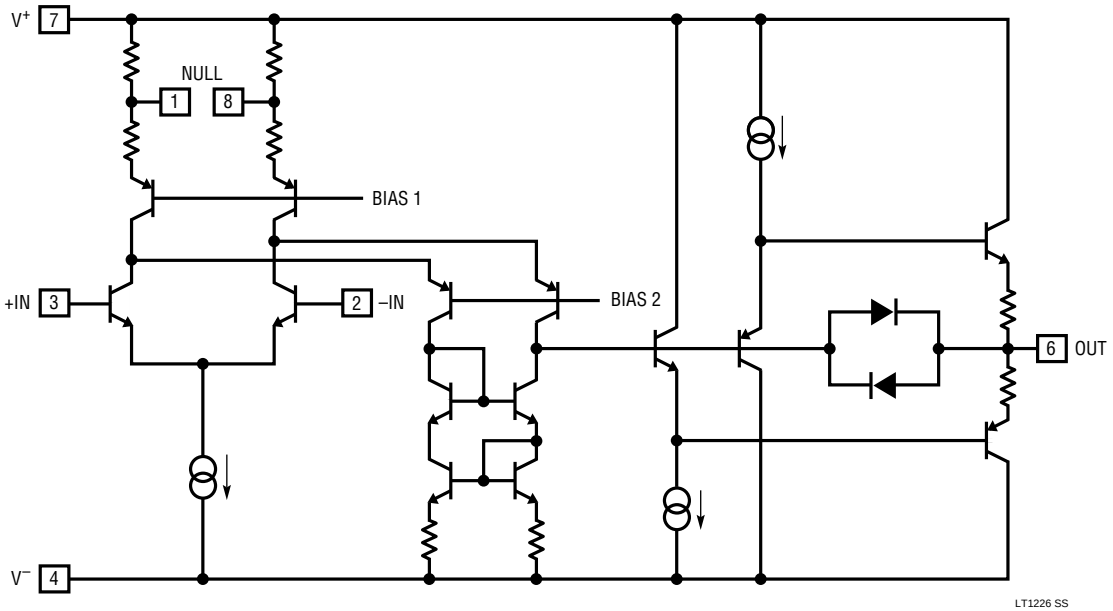
V_{OS} Null Loop



A_V = 1001

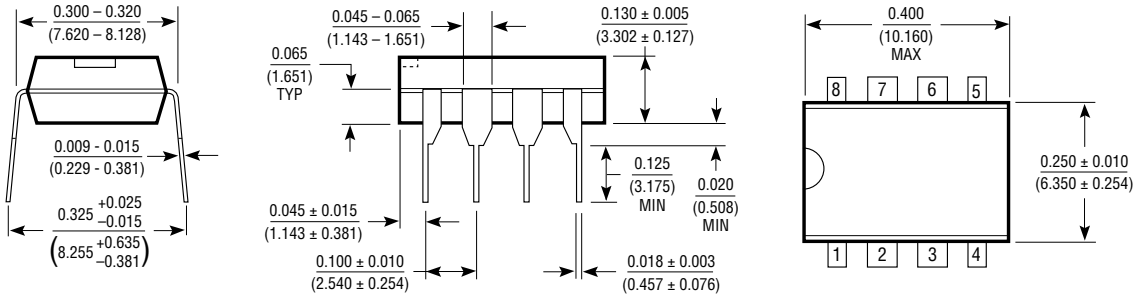
LT1226 TA06

SIMPLIFIED SCHEMATIC



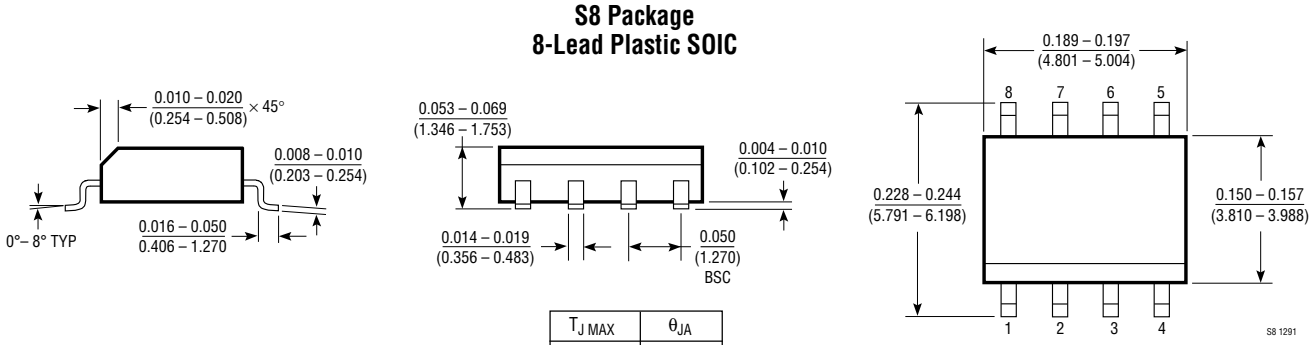
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



$T_{J\,MAX}$	θ_{JA}
150°C	130°C/W

S8 Package
8-Lead Plastic SOIC



$T_{J\,MAX}$	θ_{JA}
150°C	220°C/W

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