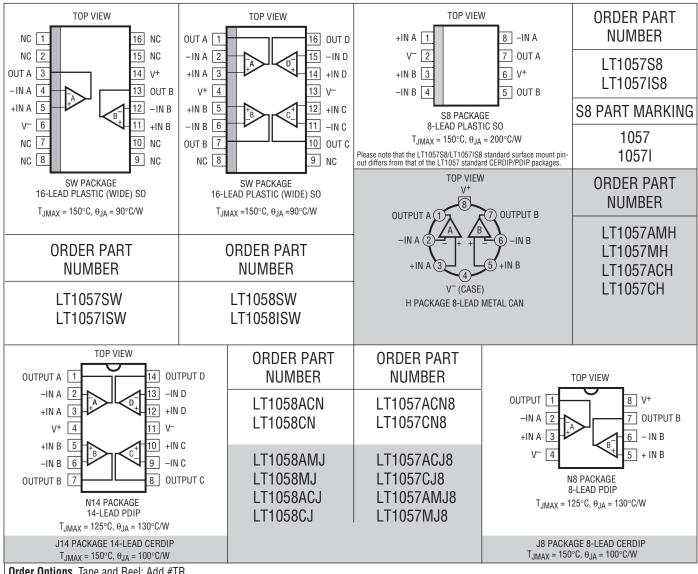
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±20V
Differential Input Voltage	±40V
Input Voltage	±20V
Output Short-Circuit Duration	
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Temperature Range LT1057AM/LT1057M/ LT1058AM/LT1058M (**OBSOLETE**).....-55°C to 125°C LT1057AC/LT1057C/LT1057S LT1058AC/LT1058C/LT1058S......0°C to 70°C LT1057I/LT1058I....-40°C $\leq T_A \leq 85$ °C

PACKAGE/ORDER INFORMATION



Order Options Tape and Reel: Add #TR

Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15 V$, $T_A = 25 ^{\circ} C$, $V_{CM} = 0 V$ unless otherwise noted. (Note 2)

				7AM/LT1 57AC/LT1			57M/LT1 57C/LT1		
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT1057 LT1057 (S8 Package) LT1058		150 180	450 600		200 220 250	800 1200 1000	μV μV μV
I _{OS}	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
I _B	Input Bias Current	Fully Warmed Up		±5	±50		±7	±75	pA
	Input Resistance	Differential Common Mode V _{CM} = -11V to 8V Common Mode V _{CM} = 8V to 11V		10 ¹² 10 ¹² 10 ¹¹			10 ¹² 10 ¹² 10 ¹¹		Ω Ω Ω
	Input Capacitance			4			4		pF
e _n	Input Noise Voltage	0.1Hz to 10Hz LT1057 LT1058			2.0 2.4			2.1 2.5	μV _{P-P} μV _{P-P}
e _n	Input Noise Voltage Density	$f_0 = 10$ Hz $f_0 = 1$ kHz (Note 3)		26 13	22		28 14	24	nV/√Hz nV/√Hz
in	Input Noise Current Density	f ₀ = 10Hz, 1kHz (Note 4)		1.5	4		1.8	6	fA/√Hz
A _{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V$, $R_L = 2k$ $V_0 = \pm 10V$, $R_L = 1k$	150 120	350 250		100 80	300 220		V/mV V/mV
	Input Voltage Range		±10.5	14.3 –11.5		±10.5	14.3 -11.5		V
CMRR	Common Mode Rejection Ratio	, LT1057 LT1058	86 84	100 98		82 80	98 96		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	103		86	102		dB
V _{OUT}	Output Voltage Swing	R _L = 2k	±12	±13		±12	±13		V
SR	Slew Rate		10	14		8	13		V/µs
GBW	Gain-Bandwidth Product	f = 1MHz (Note 6)	3.5	5		3	5		MHz
Is	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, V _{IN} = ±10V		132			130		dB

(LT1057/LT1058 SW Package Only), $V_S = \pm 15V$, $T_A = 25^{\circ}C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT1057 LT1058			0.3 0.35	2 2.5	mV
I_{0S}	Input Offset Current	Fully Warmed Up			5	50	pA
I _B	Input Bias Current	Fully Warmed Up			±10	±100	pA
	Input Resistance –Differential –Common Mode	V _{CM} = -11V to 8V V _{CM} = 8V to 11V			0.4 0.4 0.05		TΩ
	Input Capacitance				4		pF
e _n	Input Noise Voltage	0.1Hz to 10Hz	LT1057 LT1058		2.1 2.5		μV _{P-P}
e _n	Input Noise Voltage Density	f ₀ = 10Hz f ₀ = 1kHz			26 13		nV/√Hz

ELECTRICAL CHARACTERISTICS (LT1057/LT1058 SW Package Only), $V_S = \pm 15V$, $T_A = 25^{\circ}C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
i _n	Input Noise Current Density	f ₀ = 10Hz, 1kHz			1.8		fA/√Hz
$\overline{A_{VOL}}$	Large-Signal Voltage Gain	V ₀ = ±10V	R _L = 2k R _L = 1k	100 50	300 220		V/mV
	Input Voltage Range			±10.5	14.3 -11.5		V
CMRR	Common Mode Rejection Ratio	V _{CM} = ±15V	LT1057 LT1058	82 80	98 98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 18V$		86	102		dB
V_{OUT}	Output Voltage Swing	R _L = 2k		±12	±13		V
SR	Slew Rate			8	13		V/µs
GBW	Gain-Bandwidth Product	f = 1MHz (Note 6)		3	5		MHz
Is	Supply Current Per Amplifier				1.7	2.8	mA
	Channel Separation	DC to 5kHz, V _{IN} = ±10V			130		dB

The ullet denotes the specifications which apply over the temperature range of 0°C \leq T_A \leq 70°C or -40°C \leq T_A \leq 85°C (LT1057IS8), otherwise specifications are T_A = 25°C. V_S = \pm 15V, V_{CM} = 0V, unless noted.

				LT1057AC LT1058AC			LT1057C LT1058C			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT1057 LT1057IS8 LT1057S8 LT1058	•		250 300	800 1200		330 500 400 400	1400 2300 1900 1800	μV μV μV
	Average Temperature Coefficient of Input (Offset Voltage)	LT1057 H/J8 Package N8 Package LT1057S8 (Note 5) LT1057IS8 (Note 5) LT1058 J Package (Note 5) N Package (Note 5)	• • • •		1.8 3 2.5 4	7 10 10 15		2.3 4 4 4.5 3 5	12 16 16 16 15 22	μV/°C μV/°C μV/°C μV/°C μV/°C
I _{OS}	Input Offset Current	Warmed Up, T _A = 70°C LT1057IS8	•		18	150		20 35	250 600	pA
I _B	Input Bias Current	Warmed Up, T _A = 70°C LT1057IS8	•		±50	±250		±60 ±100	±350 ±900	pA
A _{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V, R_L = 2k$	•	70	220		50	200		V/mV
CMRR	Common Mode Rejection Ratio	V _{CM} = ±10.4V	•	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	V _S = ±10V to ±18V	•	87	102		84	100		dB
V _{OUT}	Output Voltage Swing	R _L = 2k	•	±12	±12.8		±12	±12.8		V
I _S	Supply Current Per Amplifier	T _A = 70°C	•		14	2.8		1.5	3.2	mA mA

ELECTRICAL CHARACTERISTICS (LT1057/LT1058 SW Package Only). The \bullet denotes specifications which apply over the temperature range of $V_S=\pm15V,\,V_{CM}=0V,\,0^{\circ}C\leq T_A\leq70^{\circ}C$ (LT1057SW, LT1058SW) or $-40^{\circ}C\leq T_A\leq85^{\circ}C$ (LT1057ISW, LT1058ISW), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT1057 LT1058S LT1058IS		•		0.5 0.6 0.7	2.5 3.0 4.0	mV
	Average Temperature Coefficient of Input Offset Voltage			•		5		μV/°C
I _{OS}	Input Offset Current	Warmed Up, T _A = 70°C Warmed Up, T _A = 85°C				20 35	250 400	pA
I _B	Input Bias Current	Warmed Up, T _A = 70°C Warmed Up, T _A = 85°C				±60 ±100	±400 ±700	pA
A _{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V, R_L = 2k$	LT1057 LT1058	•	50 40	200 200		mV
CMRR	Common Mode Rejection Ratio	V _{CM} = ±10.5V	LT1057 LT1058	•	80 78	96 96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 18V$	LT1057 LT1058	•	84 82	100 100		dB
V _{OUT}	Output Voltage Swing	R _L = 2k		•	±12	±12.8		V

The ullet denotes the specifications which apply over the temperature range of $-55^{\circ}C \le T_A \le 125^{\circ}C$, $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted.

					.T1057AI .T1058AI			LT1057N LT1058N	-	
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT1057 LT1058	•		300 380	1100 1600		400 550	2000 2500	μV μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057 LT1058 (Note 5)	•		2.0 2.5	7 10		2.5 3	12 15	μV/°C μV/°C
I _{OS}	Input Offset Current	Warmed Up, T _A = 125°C			0.15	2		0.2	3	nA
I _B	Input Bias Current	Warmed Up, T _A = 125°C			±0.6	±4.5		±0.7	±6	nA
A _{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V, R_L = 2k$	•	40	120		30	110		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	•	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 17V$	•	86	100		83	98		dB
V _{OUT}	Output Voltage Swing	R _L = 2k	•	±12	±12.7		±12	±12.6		V
I _S	Supply Current Per Amplifier	T _A = 125°C			1.25	1.9		1.3	2.2	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; (i.e., out of 100 LT1058s or, 100 LT1057s, typically 240 op amps, or 120 for the LT1057, will be better than the indicated specification).

Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula:

 $i_n = (2ql_b)^{1/2}$

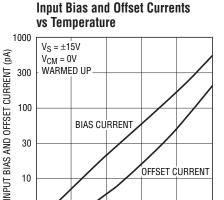
where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 1G swamps the contribution of current noise.

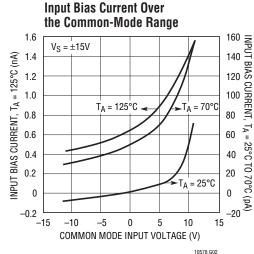
Note 5: This parameter is not 100% tested.

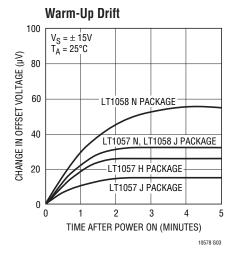
Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.



TYPICAL PERFORMANCE CHARACTERISTICS







Distribution of Offset Voltage Drift with Temperature (H and J Package)

AMBIENT TEMPERATURE (°C)

50

75

100

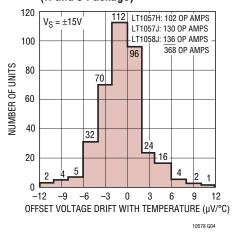
125

10578 G01

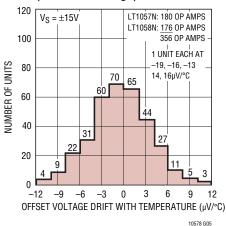
3

0

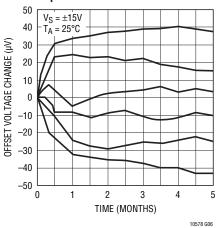
25



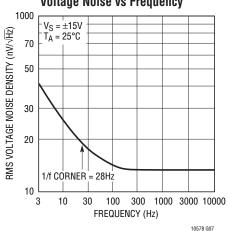
Distribution of Offset Voltage Drift with Temperature (Plastic N Package)



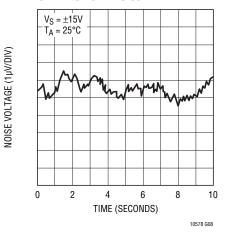
Long-Term Drift of Representative Units



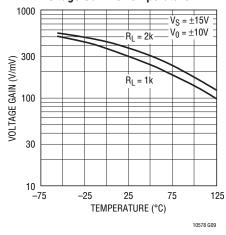
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise



Voltage Gain vs Temperature

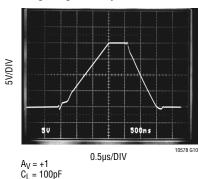




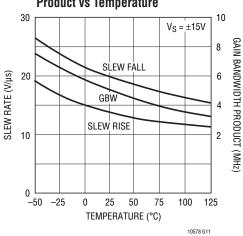


TYPICAL PERFORMANCE CHARACTERISTICS

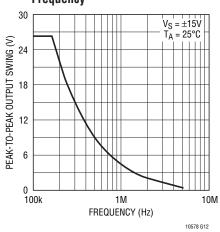




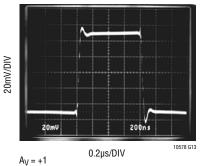
Slew Rate, Gain-Bandwidth **Product vs Temperature**



Undistorted Output Swing vs Frequency

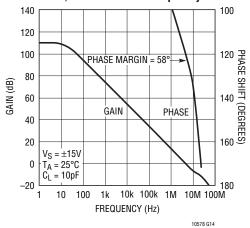


Small-Signal Response

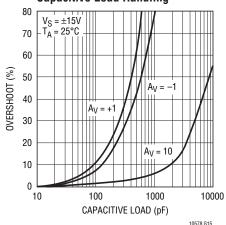




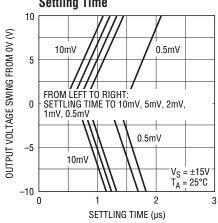
Gain, Phase Shift vs Frequency



Capacitive Load Handling

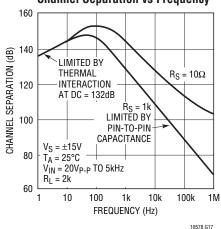


Settling Time

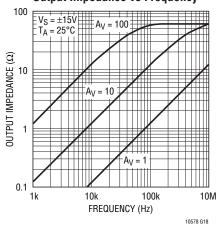


10578 G16

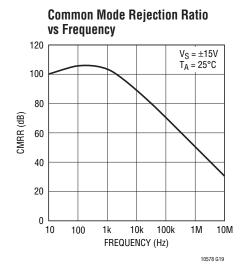
Channel Separation vs Frequency

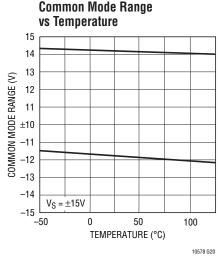


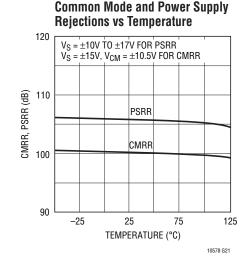
Output Impedance vs Frequency

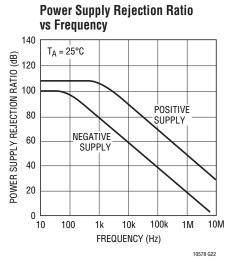


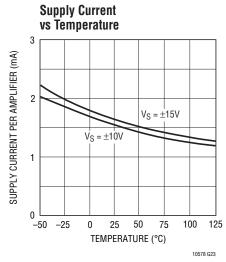
TYPICAL PERFORMANCE CHARACTERISTICS

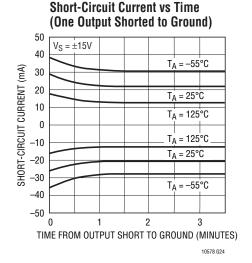












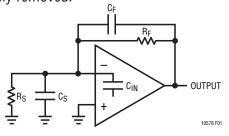
APPLICATIONS INFORMATION

The LT1057 may be inserted directly in LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074 and TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

High Speed Operation

When the feedback around the op amp is resistive (R_F) a pole will be created with R_F , the source resistance and capacitance (R_S , C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and

with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.





APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations, the guard ring should be tied to ground, in noninverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers (because the transconductance of FETs is considerably lower than that of bipolar transistors). Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Teflon is a trademark of DuPont.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical $40\mu V$ hysteresis $(50\mu V)$ on the M grades) when cycled over the $-55^{\circ}C$ to $125^{\circ}C$ temperature range. Temperature cycling from $0^{\circ}C$ to $70^{\circ}C$ has a negligible (less than $20\mu V$) hysteresis effect.

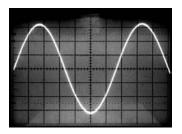
The offset voltage and drift performance are also affected by packaging. In the plastic N package, the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently for best drift performance, as shown in the Typical Performance Characteristics distribution plots, the J or H packages are recommended.

In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

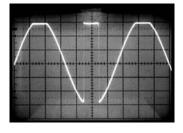
Phase Reversal Protection

Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common mode limit at the input is exceeded (i.e., below -12V with $\pm 15V$ supplies). The photos below show a $\pm 16V$ sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

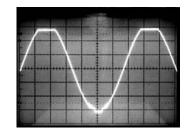
The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.



(A) ±16V Sine Wave Input



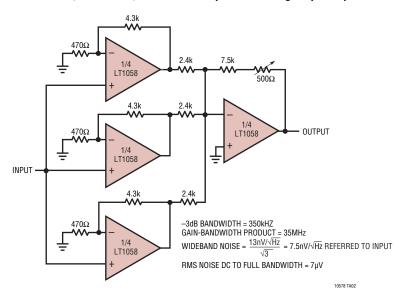
(B) LF412A Output



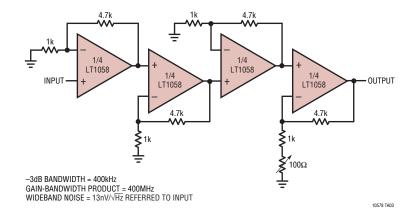
(C) LT1057/LT1058 Output

All Photos 5V/Div Vertical Scale, 50µs/Div Horizontal Scale

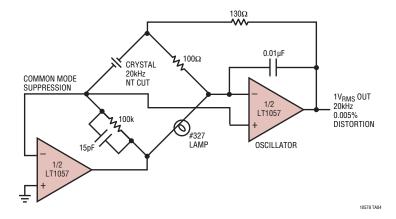
Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



Wideband, High Input Impedance, Gain = 1000 Amplifier

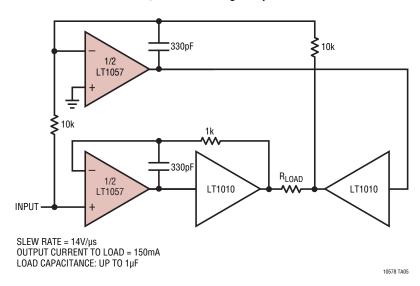


Low Distortion, Crystal Stabilized Oscillator

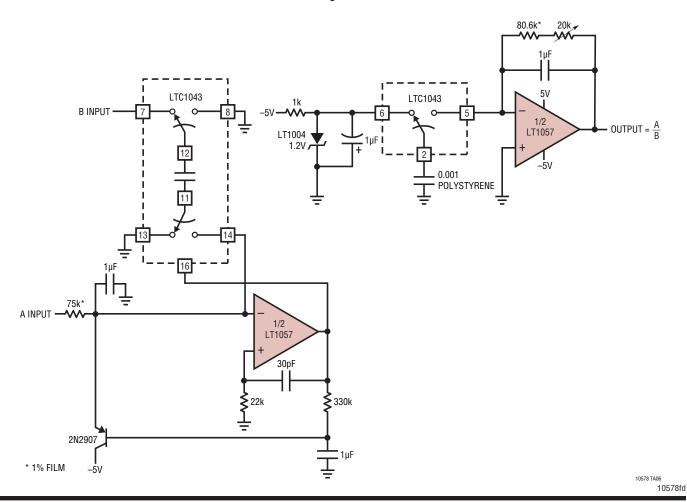




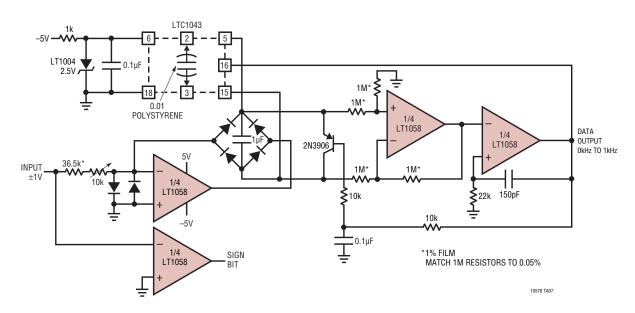
Fast, Precision Bridge Amplifier



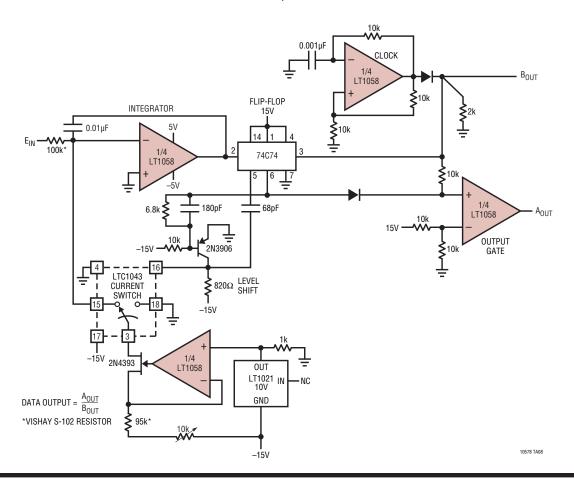
Analog Divider



Bipolar Input (AC) V/F Converter

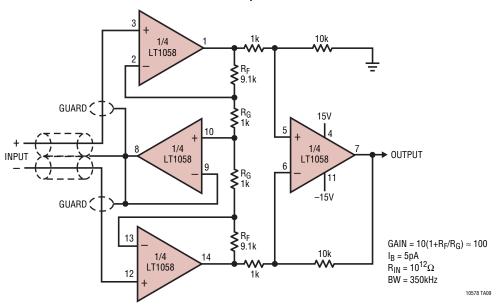


12-Bit A/D Converter

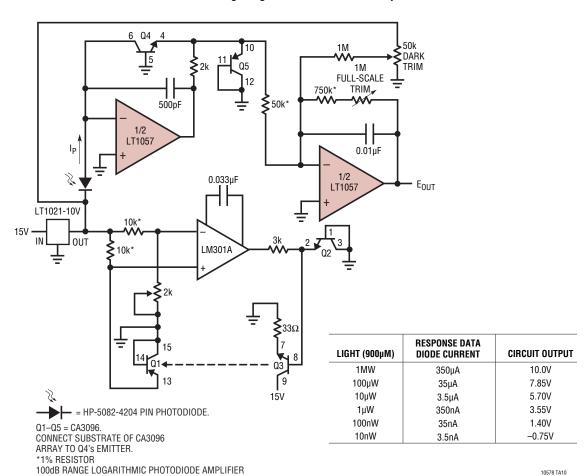


LINEAR

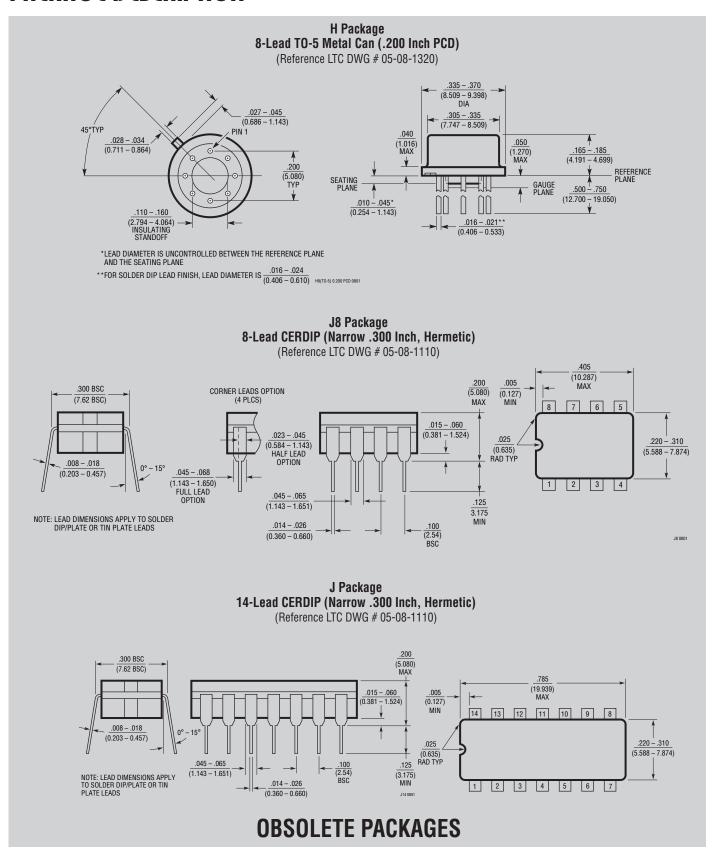
Instrumentation Amplifier with Shield Driver



100dB Range Logarithmic Photodiode Amplifier



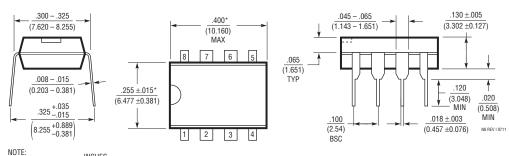
PACKAGE DESCRIPTION



PACKAGE DESCRIPTION

N Package 8-Lead PDIP (Narrow .300 Inch)

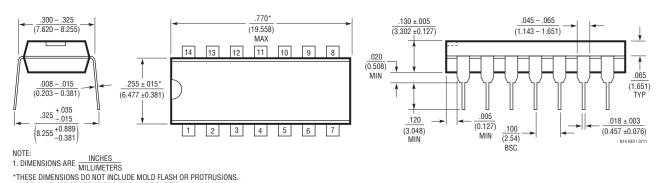
(Reference LTC DWG # 05-08-1510 Rev I)



1. DIMENSIONS ARE INCHES MILLIMETERS

N Package 14-Lead PDIP (Narrow .300 Inch)

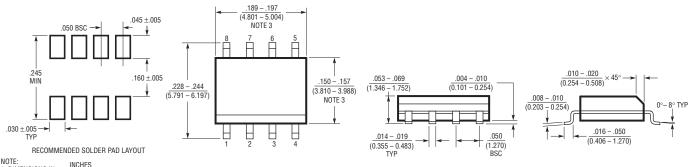
(Reference LTC DWG # 05-08-1510 Rev I)



MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1610 Rev G)



NOTE: 1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$ 2. DRAWING NOT TO SCALE

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

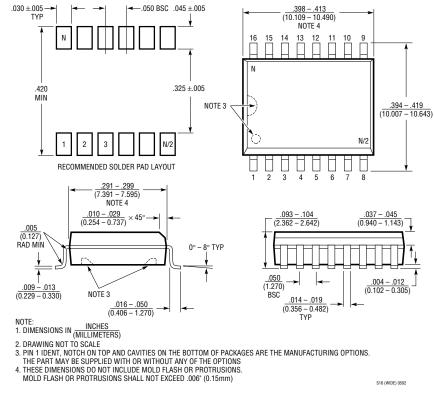
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE



^{*}THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

SW Package 16-Lead Plastic Small Outline (Wide .300 Inch)

(Reference LTC DWG # 05-08-1620)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1055/6	Precision, High Speed, JFET Input Operational Amplifiers	12V/µs Slew Rate, 5.5MHz Bandwidth
LT1880	SOT-23, Rail-to-Rail Output, Picoamp Input Precision Op Amps	150μV Max Offset Voltage, 900pA Max Input Bias Current
LT1881/2	Dual and Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps	50μV Max Offset Voltage, 200pA Max Input Bias Current
LT1884/5	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps	50μV Max Offset Voltage, 400pA Max Input Bias Current
LT6010	135µA, 14nV/rtHz, Rail-to-Rail Output, Precision Low Power Op Amp with Shutdown	35μV Max Offset Voltage, 300pA Max Input Bias Current
LT6011/12	Dual/Quad 135µA, 14nV/rtHz, Rail-to-Rail Output Precision Low Power Op Amp	60μV Max Offset Voltage, 300pA Max Input Bias Current
LTC6078/9	Micropower Precision, Dual/Quad CMOS Rail-to-Rail Input/Output Amplifiers	Maximum Offset Drift: 0.7μV/°C
LTC6241/2	Dual/Quad 18MHz, Low Noise, Rail-to-Rail CMOS Op Amps	O.1Hz to 10Hz Noise: 550n Vpp

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