

LB1945H

Allowable Operating Ranges at $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V_{BB}		10 to 28	V
Logic supply voltage	V_{CC}		4.75 to 5.25	V
Reference voltage	V_{REF}		1.5 to 5.0	V

Electrical Characteristics at $T_a = 25^{\circ}\text{C}$, $V_{BB} = 24\text{V}$, $V_{CC} = 5\text{V}$, $V_{REF} = 5.0\text{V}$

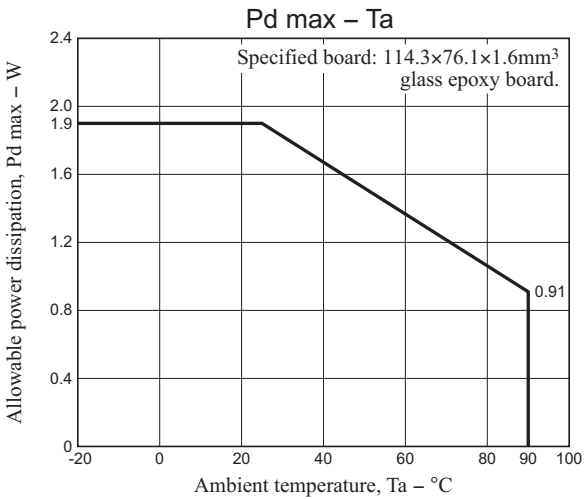
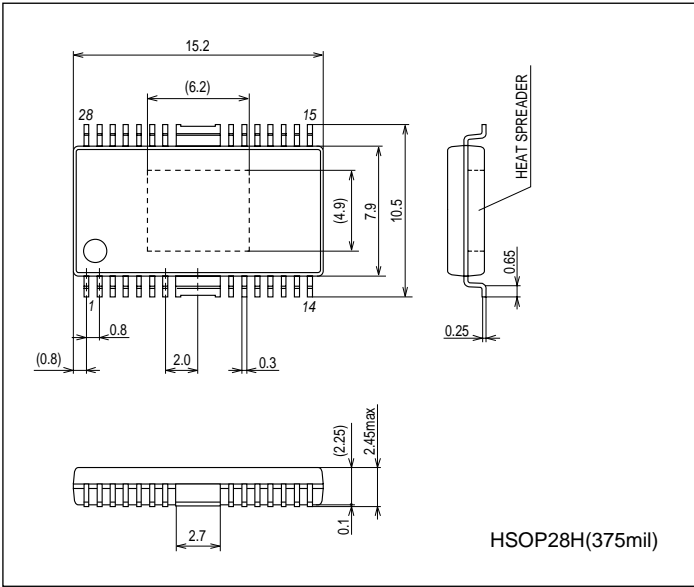
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output Block						
Output stage supply current	I _{BB} ON	I ₁ = 0.8V, I ₂ = 0.8V, ENABLE = 0.8V	0.5	1.0	2.0	mA
	I _{BB} OFF	ENABLE = 3.2V			0.2	mA
Output saturation voltage	V _{Osat1}	I _O = +0.5A, sink		0.3	0.5	V
	V _{Osat2}	I _O = +0.8A, sink		0.5	0.7	V
	V _{Osat3}	I _O = -0.5A, source		1.6	1.8	V
	V _{Osat4}	I _O = -0.8A, source		1.8	2.0	V
Output leakage current	I _{O1} (leak)	V _O = V _{BB} , sink			50	μA
	I _{O2} (leak)	V _O = 0V, source	-50			μA
Output sustain voltage	V _{SUS}	L = 3.9mH, I _O = 1.0A, Design guarantee value *	30			V
Logic Block						
Logic supply current	I _{CC} ON	I ₁ = 0.8V, I ₂ = 0.8V, ENABLE = 0.8V	50	70	92	mA
	I _{CC} OFF	ENABLE = 3.2V	7	10	13	mA
Input voltage	V _{IH}		3.2			V
	V _{IL}				0.8	V
Input current	I _{IH}	V _{IH} = 3.2V	35	50	65	μA
	I _{IL}	V _{IL} = 0.8V	7	10	13	μA
Set current control threshold value	V _{ref} /V _{sen}	I ₁ = 0.8V, I ₂ = 0.8V	9.5	10	10.5	
		I ₁ = 3.2V, I ₂ = 0.8V	13.5	15	16.5	
		I ₁ = 0.8V, I ₂ = 3.2V	25.5	30	34.5	
Reference current	I _{ref}	V _{ref} = 5.0V, I ₁ = 0.8V, I ₂ = 0.8V	17.5	25	32.5	μA
CR pin current	I _{CR}	CR = 1.0V	-1.0			mA
Thermal shutdown temperature	T-TSD	Design guarantee value *		170		°C
Temperature hysteresis width	T _s hys			40		°C

* Design guarantee value, Do not measurement.

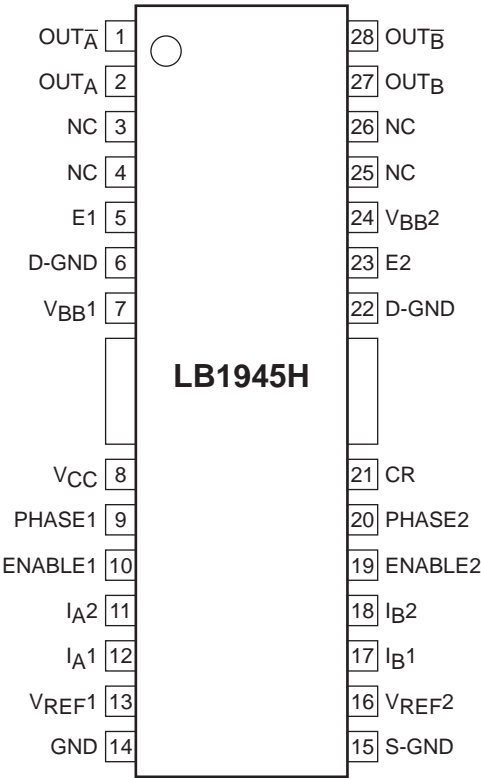
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Package Dimensions

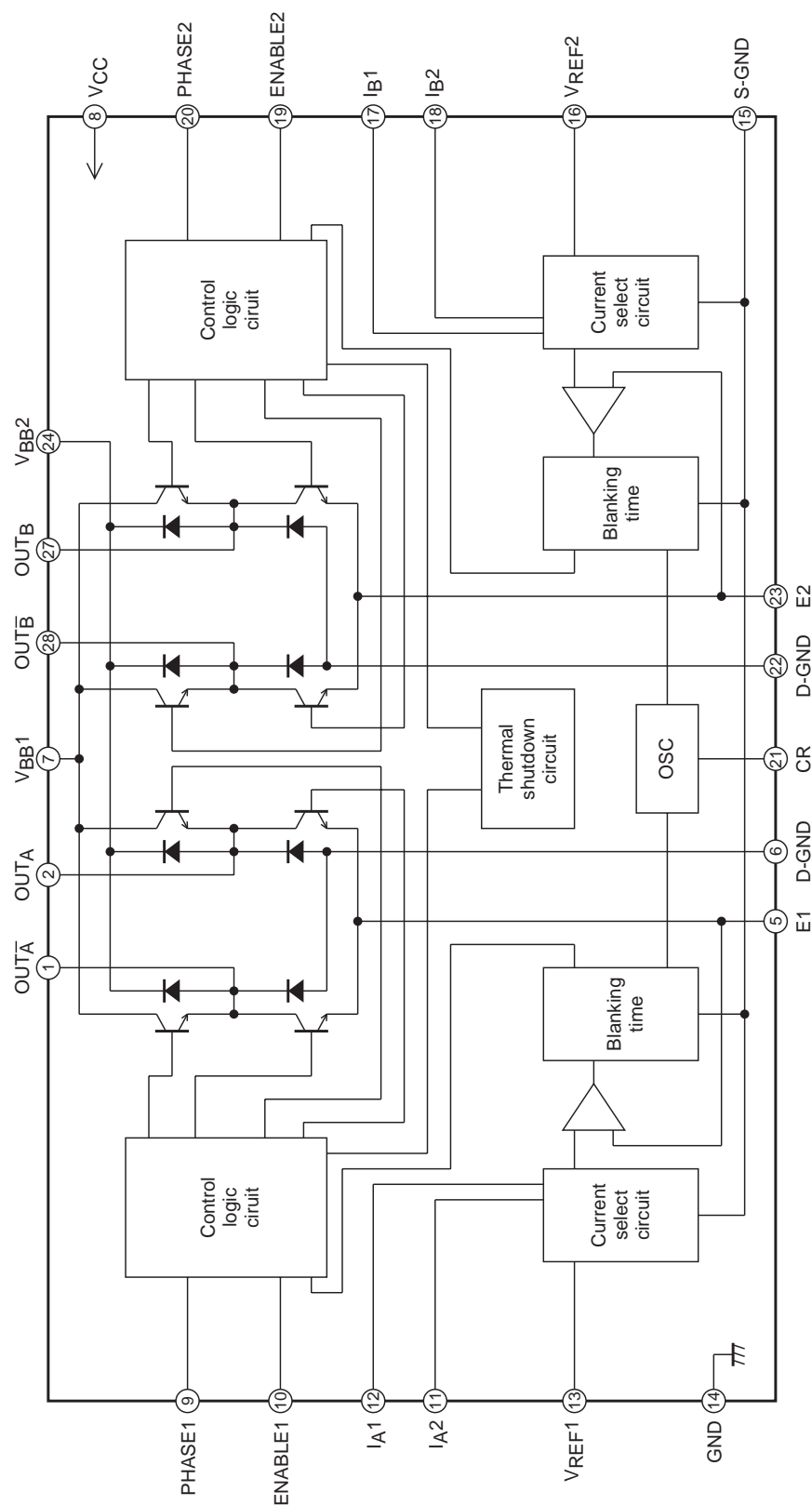
unit : mm (typ)
3233B



Pin Assignment



Block Diagram



Truth Table

ENABLE	PHASE	OUT _A	OUT _A [̄]
L	H	H	L
L	L	L	H
H	–	OFF	OFF

I ₁	I ₂	Output current
L	L	$V_{ref} / (10 \times RE) = I_{OUT}$
H	L	$V_{ref} / (15 \times RE) = I_{OUT} \times 2/3$
L	H	$V_{ref} / (30 \times RE) = I_{OUT} \times 1/3$
H	H	0

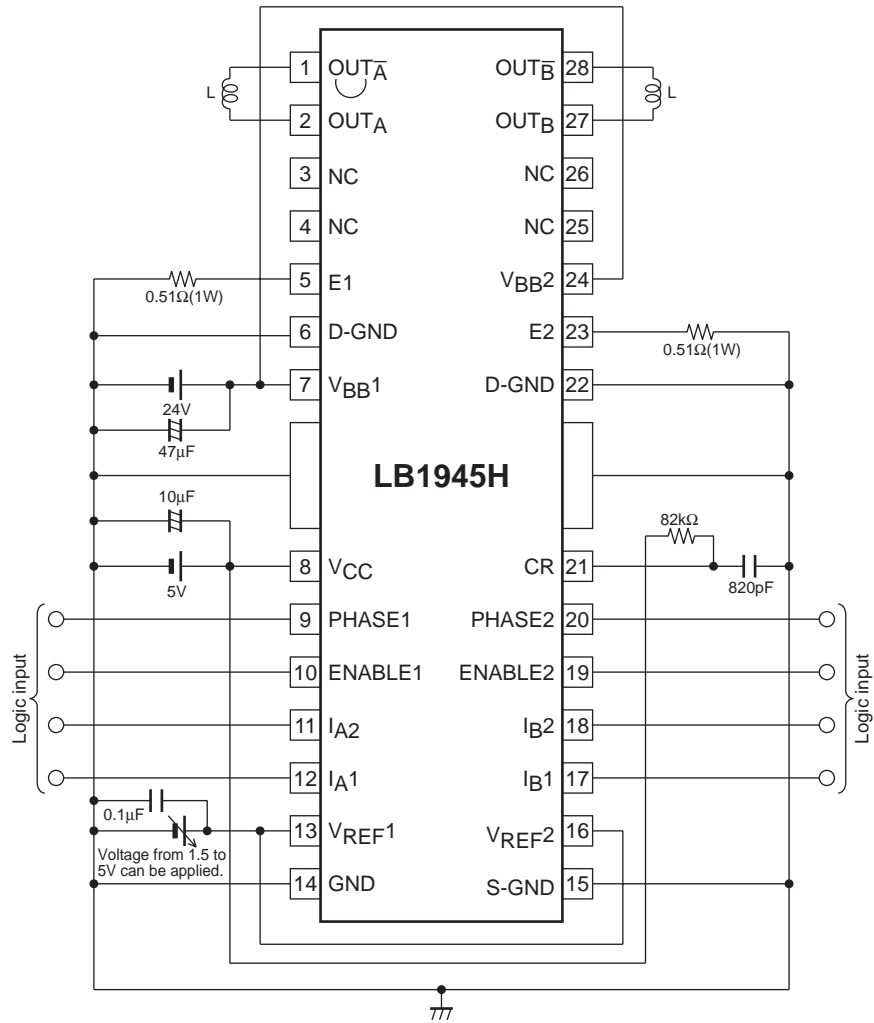
Note: Output is OFF when ENABLE = H or when I₁ = I₂ = H.

Pin Function

Pin No.	Pin name	Function
7	V _{BB} 1	Output stage power supply voltage pin.
24	V _{BB} 2	Cathode pin for the upper-side diodes.
5 23	E1 E2	Insert resistor RE between these pins and ground to control set current.
2 1 27 28	OUT _A OUT _A [̄] OUT _B OUT _B [̄]	Output pins.
14	GND	Ground pin.
15	S-GND	Sense ground pin.
6 22	D-GND D-GND	Lower-side internal diode ground (anode).
21	CR	Triangular wave chopping with CR constant setting. Triangular wave OFF time is noise cancel time.
13 16	V _{REF} 1 V _{REF} 2	Output current setting pins. (Output current is set by inputting a 1.5V to 7.5V voltage.)
9 20	PHASE1 PHASE2	Output phase select input pin. High input: OUT _A = H, OUT _A [̄] = L Low input: OUT _A = L, OUT _A [̄] = H
10 19	ENABLE1 ENABLE2	Output ON/OFF setting input pins. High input: output OFF Low input: output ON
12,11 17,18	I _A 1,I _A 2 I _B 1,I _B 2	Output current setting digital input pins. Current is set to 1/3, 2/3, 1 by High and Low combinations.
8	V _{CC}	Logic block power supply voltage pin.

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Application Circuit Example



The fin on the bottom of HSOP-28H package and the fins between pins 7 and 8 and 21 and 22 should be grounded.

Usage Notes**1. VREF pin**

Because the VREF pin is used as reference voltage input pin for the current setting, care must be taken to prevent noise from affecting the input.

2. GND pin

Because this IC switches large currents, the ground pattern must be designed with care. The fin on the bottom of the package and the fins between pins 7 and 8 and 21 and 22 should be grounded. Low-impedance patterns should be used in blocks where large currents flow, and these blocks should be separated from low-level signal blocks. In particular, the ground of the sense resistor RE at pin E should be located close to the IC ground. Pattern layout should be designed so that the capacitors between V_{CC} and ground and V_{BB} and ground are close to V_{CC} and V_{BB} .

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