Features

- The CENTAUR KS8695X featuring XceleRouter technology is a single-chip multi-port gateway-on-a-chip with all the key components integrated for a high-performance and low-cost broadband gateway.
- ARM922T High-Performance CPU Core
  - ARM922T core at 166MHz
  - 8KB I-cache and 8KB D-cache
  - Memory management unit (MMU) for Linux and WinCE®
  - 32-bit ARM and 16-bit thumb instruction sets for smaller memory footprints
- XceleRouter Technology
  - TCP/UDP/IP packet header checksum generation to offload CPU tasks
  - IPv4 packet filtering on checksum errors
  - Automatic error packet discard
- Integrated Ethernet Transceivers and Switch Engine
  - Five 10/100 transceivers and five MACs (1P for WAN interface, 4P for LAN switching)
  - 10BASE-T, 100BASE-TX, and 100BASE-FX modes (FX on the WAN port)
  - On-chip SRAM as frame buffer memory
  - Wire-speed switching
  - VLAN ID and 802.1p tag/untag options
  - Extensive MIB counter management support
  - IGMP snooping for multicast packet filtering
  - Port-based VLAN
  - QoS/CoS packet prioritization support: per port, 802.1p and DiffServ-based
  - 802.1D Spanning Tree Protocol support
  - Dedicated 1K entry look-up engine
  - Automatic MDI/MDI-X crossover on all ports
  - Port mirroring/monitoring/sniffing
  - Broadcast storm protection with % control
  - Full- and half-duplex flow control
- Memory and External I/O Interfaces
  - 8/16/32-bit wide shared data path for SDRAM, ROM/SRAM/Flash and external I/O
  - Total memory space up to 64MB
  - Intel®/AMD®-type Flash support
- WAN and LAN DMA Engines and FIFO
  - DMA engine with burst mode support for efficient WAN and LAN data transfers
  - FIFOs for back-to-back packet transfers
- Peripheral Support
  - 8/16/32-bit external I/O interface supporting PCMCIA or generic CPU/DSP host I/F
  - Eight general-purpose input/output (GPIO)
  - Two 32-bit timer counters (one watchdog)
  - Interrupt controller
  - ARM922T JTAG debug interface
- Power Management
  - Reduced CPU and system clock speeds
- System Design
  - Up to 166MHz CPU and 125MHz bus speed
- Reference HW/SW Evaluation Kit
  - Hardware evaluation board (passes class B EMI)
  - Board support package including firmware source codes, linux kernel, and software stacks
  - Documentation for design and programming
- Commercial Temperature Range: 0°C to +70°C
- Available in 208-Pin PQFP

Applications

- Multi-port broadband gateway
- Multi-port firewall and VPN appliances
- Combination wireless and wireline gateway
- Multi-port VoIP gateway
- Fiber-to-the-home managed CPE

Ordering Information

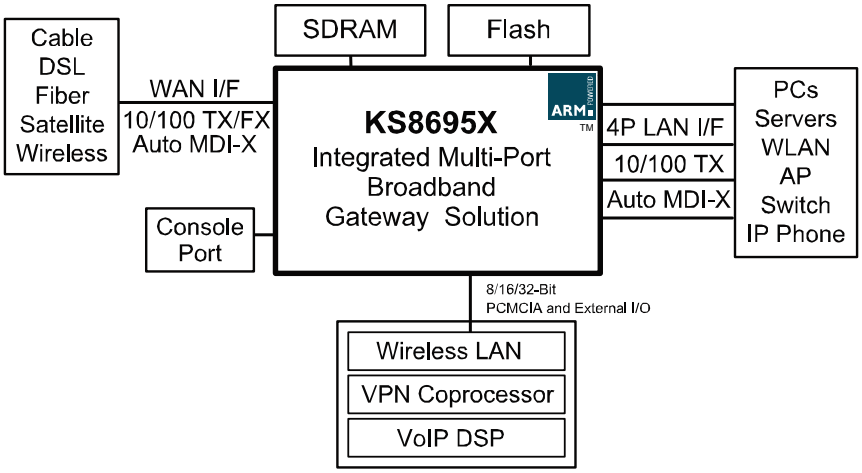
Part Number		Temperature Range	Package
Standard	**Pb (lead)-Free**		
KS8695X	KSZ8695X	0° to +70°C	208-Pin PQFP

Revision History

Revision	Date	Summary of Changes
1.00	05/24/04	Created.
1.01	06/17/04	Updated System Clock.
1.02	10/26/04	Updated Timing Diagrams: SRAM Read and Write, SDRAM Read and Write, and External I/O Read/Write Cycles.
1.03	06/01/06	Added pb-free option.

Contents

System Level Applications



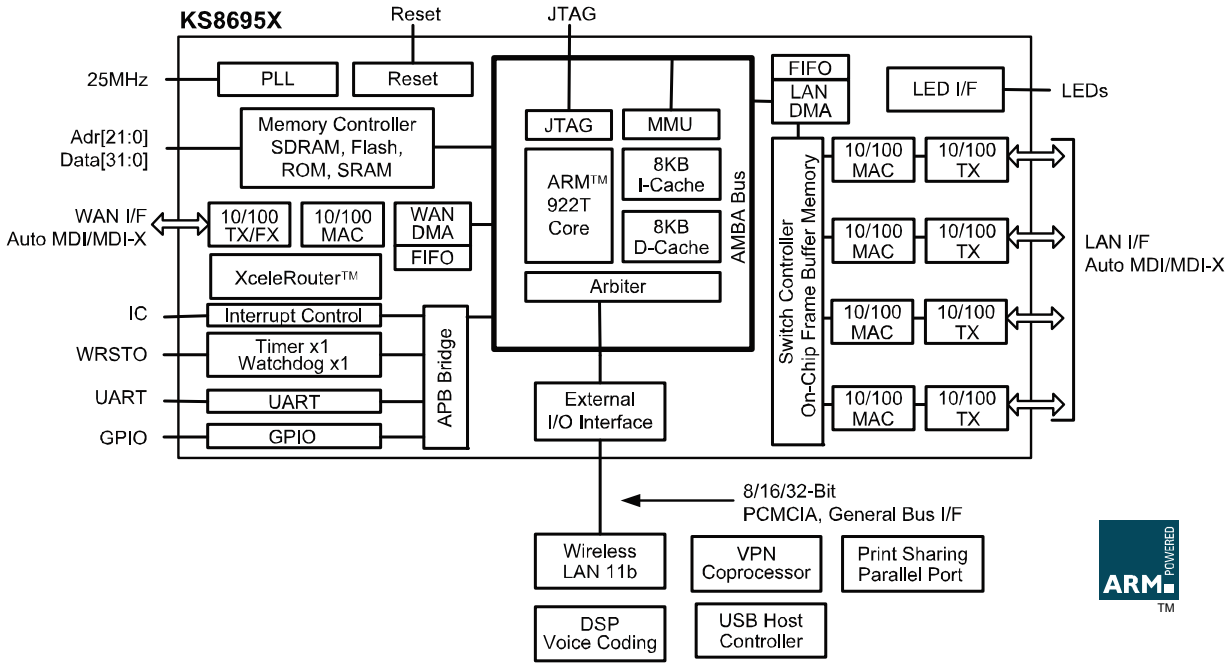


Figure 1. KS8695X Applications

Pin Description

Pin Number	Pin Name	Type[1]	Pin Function
1	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
2	VSS-IO	Gnd	Digital I/O V_{SS}.
3	ADDR10	O	Address Bit.
4	ADDR9	O	Address Bit.
5	ADDR8	O	Address Bit.
6	ADDR7	O	Address Bit.
7	ADDR6	O	Address Bit.
8	ADDR5	O	Address Bit.
9	ADDR4	O	Address Bit.
10	ADDR3	O	Address Bit.
11	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
12	VSS-IO	Gnd	Digital I/O V_{SS}.
13	ADDR2	O	Address Bit.
14	ADDR1	O	Address Bit.
15	ADDR0	O	Address Bit.
16	SDCSN1	O	SDRAM Chip Select. Active Low Chip Select Pins for SDRAM.
17	SDCSN0	O	SDRAM Chip Select. Active Low Chip Select Pins for SDRAM.
18	SDRASN	O	SDRAM Row Address Strobe. Active Low.
19	SDCASN	O	SDRAM Column Address Strobe. Active Low.
20	SDWEN	O	SDRAM Write Enable. Active Low.
21	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
22	VSS-IO	Gnd	Digital I/O V_{SS}.
23	SDOCLK	O	System/SDRAM Clock Out.
24	SDICLK	I	SDRAM Clock In.
25	VDD-CORE	P	1.8V Digital Core V_{DD}.
26	VSS-CORE	Gnd	Digital Core V_{SS}.
27	SDQM3	O	SDRAM Data Input/Output Mask.
28	SDQM2	O	SDRAM Data Input/Output Mask.
29	SDQM1	O	SDRAM Data Input/Output Mask.
30	SDQM0	O	SDRAM Data Input/Output Mask.
31	DATA31	I/O	External Data Bit.
32	DATA30	I/O	External Data Bit.

Note:

1. Gnd = Ground.
   P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.

Pin Number	Pin Name	Type[1]	Pin Function
33	DATA29	I/O	External Data Bit.
34	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
35	VSS-IO	Gnd	Digital I/O V_{SS}.
36	DATA28	I/O	External Data Bit.
37	DATA27	I/O	External Data Bit.
38	DATA26	I/O	External Data Bit.
39	DATA25	I/O	External Data Bit.
40	DATA24	I/O	External Data Bit.
41	DATA23	I/O	External Data Bit.
42	DATA22	I/O	External Data Bit.
43	VDD-CORE	P	1.8V Digital Core V_{DD}.
44	VSS-CORE	Gnd	Digital Core V_{SS}.
45	DATA21	I/O	External Data Bit.
46	DATA20	I/O	External Data Bit.
47	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
48	VSS-IO	Gnd	Digital I/O V_{SS}.
49	DATA19	I/O	External Data Bit.
50	DATA18	I/O	External Data Bit.
51	DATA17	I/O	External Data Bit.
52	DATA16	I/O	External Data Bit.
53	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
54	VSS-IO	Gnd	Digital I/O V_{SS}.
55	DATA15	I/O	External Data Bit.
56	DATA14	I/O	External Data Bit.
57	DATA13	I/O	External Data Bit.
58	DATA12	I/O	External Data Bit.
59	DATA11	I/O	External Data Bit.
60	DATA10	I/O	External Data Bit.
61	DATA9	I/O	External Data Bit.
62	DATA8	I/O	External Data Bit.
63	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
64	VSS-IO	Gnd	Digital I/O V_{SS}.
65	DATA7	I/O	External Data Bit.

Note:

1. Gnd = Ground.
   P = Power supply.
   I/O = Bidirectional.

Pin Number	Pin Name	Type(1)	Pin Function
66	DATA6	I/O	External Data Bit.
67	DATA5	I/O	External Data Bit.
68	DATA4	I/O	External Data Bit.
69	DATA3	I/O	External Data Bit.
70	DATA2	I/O	External Data Bit.
71	DATA1	I/O	External Data Bit.
72	DATA0	I/O	External Data Bit.
73	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
74	VSS-IO	Gnd	Digital I/O V_{SS}.
75	ECSN2	O	External I/O Device Chip Select. Active Low.
76	ECSN1	O	External I/O Device Chip Select. Active Low.
77	ECSN0	O	External I/O Device Chip Select. Active Low.
78	EWAITN	I	External Wait. Active Low.
79	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
80	VSS-IO	Gnd	Digital I/O V_{SS}.
81	RCSN1	O	ROM/SRAM/FLASH Chip Select. Active Low.
82	RCSN0	O	ROM/SRAM/FLASH Chip Select. Active Low.
83	WRSTO	O	Watchdog Timer Reset Output.
84	TEST3	NC	This pin must be left as no connect.
85	EROEN/ WRSTPLS	O/I	ROM/SRAM/FLASH and External I/O Output Enable. Active Low. /WRSTO Polarity Select.
86	ERWEN3/ TICTESTENN	O	External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.
87	ERWEN2/ TESTREQA	O	External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.
88	ERWEN1/ TESTREQB	O	External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.
89	ERWEN0/ TESTACK	O	External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.
90	VDD-CORE	P	1.8V Digital Core V_{DD}.
91	VSS-CORE	Gnd	Digital Core V_{SS}.
92	URXD	I	UART Receive Data.
93	UDTRN/ DBGENN	O	UART Data Terminal Ready. Active Low. /Debug Enable (factory test signal).
94	UTXD	O	UART Transmit Data.

Note:

1. Gnd = Ground.
   P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   O/I = Output in normal mode; input pin during reset.
   NC = No connect.

Pin Number	Pin Name	Type(1)	Pin Function
95	UDSRN	I	UART Data Set Ready. Active Low.
96	URTSN/ CPUCLKSEL	O/I	UART Request to Send/CPU Clock Select.
97	UCTSN/ BISTEN	I	UART Data Set Ready. Active Low. /BIST Enable (factory test signal).
98	UDCDN/ SCANEN	I	UART Data Carrier Detect. /Scan Enable (factory test signal).
99	URIN/ TSTRST	I	UART Ring Indicator/Chip Test Reset (factory test signal).
100	GPIO7	I/O	General Purpose I/O Pin.
101	GPIO6	I/O	General Purpose I/O Pin.
102	GPIO5/ TOUT1	I/O	General Purpose I/O Pin/Timer 1 Output Pin.
103	VDD-IO	P	3.3V Digital I/O Circuitry V_{DD}.
104	VSS-IO	Gnd	Digital I/O V_{SS}.
105	GPIO4/ TOUT0	I/O	General Purpose I/O Pin/Timer 0 Output Pin.
106	GPIO3/ EINT3	I/O	General Purpose I/O Pin/External Interrupt Request Pin.
107	GPIO2/ EINT2	I/O	General Purpose I/O Pin/External Interrupt Request Pin.
108	GPIO1/ EINT1	I/O	General Purpose I/O Pin/External Interrupt Request Pin.
109	GPIO0/ EINT0	I/O	General Purpose I/O Pin/External Interrupt Request Pin.
110	TCK	I	JTAG Test Clock.
111	TMS	I	JTAG Test Mode Select.
112	TDI	I	JTAG Test Data In.
113	TDO	O	JTAG Test Data Out.
114	TRSTN	I	JTAG Test Reset. Active Low.
115	VDD-CORE	P	1.8V Digital Core V_{DD}.
116	VSS-CORE	Gnd	Digital Core V_{SS}.
117	TESTEN	I	Chip Test Enable (factory test signal).
118	WLED1/ B0SIZE1	O/I	WAN LED Programmable Indicator 1/Bank 0 Size Bit 1.
119	WLED0/ B0SIZE0	O/I	WAN LED Programmable Indicator 0/Bank 0 Size Bit 0.

Note:

1. Gnd = Ground.
   P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   O/I = Output in normal mode; input pin during reset.

Pin Number	Pin Name	Type[1]	Pin Function
120	L4LED1/ DBGAD7	O	LAN Port 4 LED Programmable Indicator 1.
121	L4LED0/ DBGAD6	O	LAN Port 4 LED Programmable Indicator 0.
122	L3LED1/ DBGAD5	O	LAN Port 3 LED Programmable Indicator 1.
123	L3LED0/ DBGAD4	O	LAN Port 3 LED Programmable Indicator 0.
124	L2LED1/ DBGAD3	O	LAN Port 2 LED Programmable Indicator 0.
125	L2LED0/ DBGAD2	O	LAN Port 2 LED Programmable Indicator 0.
126	L1LED1/ DBGAD1	O	LAN Port 1 LED Programmable Indicator 1.
127	L1LED0/ DBGAD0	O	LAN Port 1 LED Programmable Indicator 0.
128	VDD-CORE	P	1.8V Digital Core V_{DD}.
129	VSS-CORE	Gnd	Digital Core V_{SS}.
130	TEST4	NC	This pin must be left as no connect.
131	TEST5	NC	This pin must be left as no connect.
132	TEST6	NC	This pin must be left as no connect.
133	TEST7	NC	This pin must be left as no connect.
134	TEST8	NC	This pin must be left as no connect.
135	TEST9	NC	This pin must be left as no connect.
136	TEST10	NC	This pin must be left as no connect.
137	VDD-IO	P	3.3V digital I/O Circuitry V_{DD}.
138	VSS-IO	Gnd	Digital I/O V_{SS}.
139	TEST11	NC	This pin must be left as no connect.
140	TEST12	NC	This pin must be left as no connect.
141	TEST13	NC	This pin must be left as no connect.
142	TEST14	NC	This pin must be left as no connect.
143	TEST15	NC	This pin must be left as no connect.
144	TEST16	NC	This pin must be left as no connect.
145	TEST17	NC	This pin must be left as no connect.
146	TEST18	NC	This pin must be left as no connect.

Note:

1. Gnd = Ground.
   P = Power supply.
   O = Output.
   NC = No connect.

Pin Number	Pin Name	Type(1)	Pin Function
147	TEST19	NC	This pin must be left as no connect.
148	RESETN	I	KS8695X Chip Reset. Active Low.
149	TEST2	I	PHY Test Pin (factory test signal).
150	XCLK1	I	External Clock In.
151	XCLK2	I	External Clock In (negative polarity).
152	VDDA-PLL	P	1.8V Analog V_{DD} for PLL.
153	GNDA	Gnd	Analog Ground.
154	VDDAR	P	1.8V Analog $V_{DD.}$
155	GNDA	Gnd	Analog Ground.
156	GNDA	Gnd	Analog Ground.
157	VDDAR	P	1.8V Analog $V_{DD.}$
158	WANFXSD/ DOUT	I/O	WAN Fiber Signal Detect/DOUT:Factory Analog Test Mode.
159	WANRXP	I	WAN PHY Receive Signal + (differential).
160	WANRXM	I	WAN PHY Receive Signal – (differential).
161	GNDA	Gnd	Analog Ground.
162	WANTXM	O	WAN PHY Transmit Signal – (differential).
163	WANTXP	O	WAN PHY Transmit Signal + (differential).
164	GNDA	Gnd	Analog Ground.
165	LANRXP1	I	LAN Port 1 PHY Receive Signal + (differential).
166	LANRXM1	I	LAN Port 1 PHY Receive Signal – (differential).
167	GNDA	Gnd	Analog Ground.
168	LANTXM1	O	LAN Port 1 PHY Transmit Signal – (differential).
169	LANTXP1	O	LAN Port 1 PHY Transmit Signal + (differential).
170	VDDAR	P	1.8V Analog $V_{DD.}$
171	GNDA	Gnd	Analog Ground.
172	ISET	I	Set PHY Transmit Output Current. Connect to Ground with 3.01kΩ 1% Resistor.
173	VDDAT	P	2.5/3.3V Analog $V_{DD.}$
174	LANRXP2	I	LAN Port 2 PHY Receive Signal + (differential).
175	LANRXM2	I	LAN Port 2 PHY Receive Signal – (differential).
176	GNDA	Gnd	Analog Ground.
177	LANTXM2	O	LAN Port 2 PHY Transmit Signal – (differential).
178	LANTXP2	O	LAN Port 2 PHY Transmit Signal + (differential).

Note:

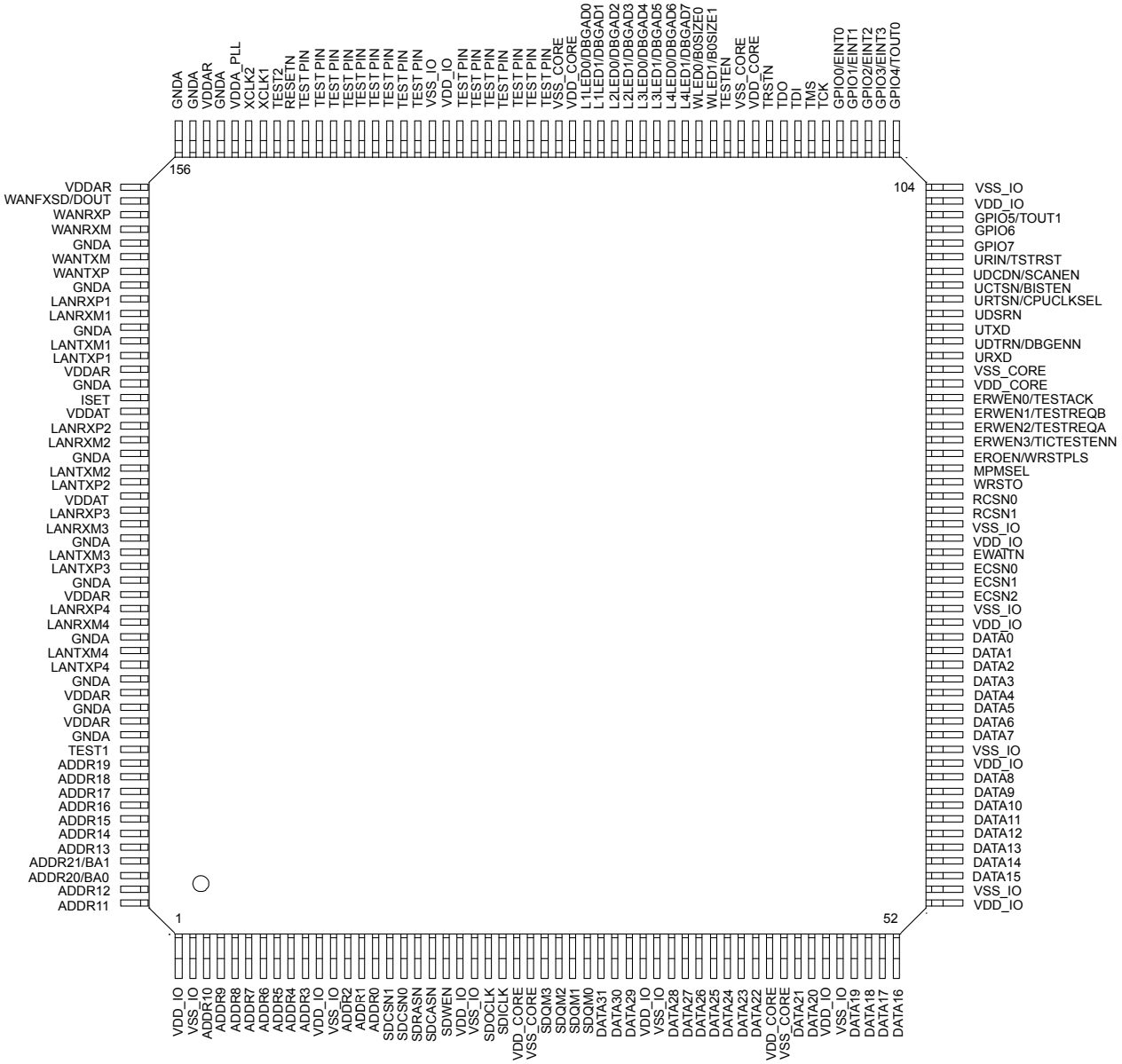
1. Gnd = Ground.
   P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   NC = No connect.

Pin Number	Pin Name	Type[1]	Pin Function
179	VDDAT	P	2.5V/3.3V Analog V_{DD}.
180	LANRXP3	I	LAN Port 3 PHY Receive Signal + (differential).
181	LANRXM3	I	LAN Port 3 PHY Receive Signal – (differential).
182	GNDA	Gnd	Analog Ground.
183	LANTXM3	O	LAN Port 3 PHY Transmit Signal – (differential).
184	LANTXP3	O	LAN Port 3 PHY Transmit Signal + (differential).
185	GNDA	Gnd	Analog Ground.
186	VDDAR	P	1.8V Analog V_{DD}.
187	LANRXP4	I	LAN Port 4 PHY Receive Signal + (differential).
188	LANRXM4	I	LAN Port 4 PHY Receive Signal – (differential).
189	GNDA	Gnd	Analog Ground.
190	LANTXM4	O	LAN Port 4 PHY Transmit Signal – (differential).
191	LANTXP4	O	LAN Port 4 PHY Transmit Signal + (differential).
192	GNDA	Gnd	Analog Ground.
193	VDDAR	P	1.8V Analog V_{DD}.
194	GNDA	Gnd	Analog Ground.
195	VDDAR	P	1.8V Analog V_{DD}.
196	GNDA	Gnd	Analog Ground.
197	TEST1	I	PHY Test Pin (factory test signal).
198	ADDR19	O	Address Bit.
199	ADDR18	O	Address Bit.
200	ADDR17	O	Address Bit.
201	ADDR16	O	Address Bit.
202	ADDR15	O	Address Bit.
203	ADDR14	O	Address Bit.
204	ADDR13	O	Address Bit.
205	ADDR21/BA1	O	Address Bit/Bank Address bit 1 for SDRAM Interface.
206	ADDR20/BA0	O	Address Bit/Bank Address bit 0 for SDRAM Interface.
207	ADDR12	O	Address Bit.
208	ADDR11	O	Address Bit.

Note:

1. Gnd = Ground.
   P = Power supply.
   I = Input.
   O = Output.

Pin Configuration



208-Pin PQFP (PQ)

Functional Description

Introduction

The CENTAUR KS8695X is a cost-effective, high-performance router-on-a-chip solution for Ethernet-based systems. It integrates a powerful processor with a 5-port switch that consists of five MAC units, five physical layer transceivers (PHYs), DMA engines, and hardware protocol engines for CPU off loading.

The KS8695X is built around the 16/32-bit ARM922T RISC processor. The ARM922T is a scalable, high-performance, microprocessor developed for highly integrated system-on-a-chip applications. The KS8695X offers an 8KB I-cache and an 8KB D-cache to reduce memory access latency for high-performance applications. There are also SDRAM, SRAM, and ROM interfaces with configurable bus speeds and data width. The KS8695X provides external I/O interfaces, a UART interface, ageneral purpose I/O, a JTAG debugging port, an internal interrupt controller, and internal timers.

The KS8695X contains independent DMA engines for the WAN and LAN. Each of the independent DMA engines supports burst mode as well as little-endian byte ordering for memory buffers and descriptors. Each DMA engine contains one 3KB receive FIFO and one 3KB transmit FIFO to ensure back-to-back packet reception and no under-runs on packet transmission.

An integrated switch provides hardware support for some of the most desirable Layer 2 features such as port-based VLAN, QoS/CoS packet prioritization, IGMP snooping, and Spanning Tree Protocol. The switch contains a 16Kx32 SRAM on-chip memory for frame buffering. The embedded frame buffer memory is designed with a 1.4Gbps on-chip memory bus. This allows the KS8695X to perform full non-blocking frame switching and/or routing.

There are five MAC units in the KS8695X: four are for LAN and one is for the WAN.

Connected to the LAN and WAN MACs are five 10/100 PHYs. These PHYs use Micrel's patented low-power analog PHY technology to achieve increased performance. The PHY units also support the auto MDI/MDI-X feature. The LAN PHYs support 10BASE-T and 100BASE-TX operation as per the IEEE802.3 standard. The WAN PHY supports 10BASE-T, 100BASE-TX, and 100BASE-FX operation.

The KS8695X combines proven PHY, MAC, and switch technology with protocol and DMA engines, and the powerful ARM922T processor to create a solution that saves BOM costs, board real-estate, and design time while providing outstanding performance for a variety of router applications.

CPU Features

- 166MHz ARM922T RISC processor core
- On-chip AMBA bus 2.0 interfaces
- 16-bit thumb programming to relax memory requirement
- 8KB I-cache and 8KB D-cache
- Little-endian mode supported
- Configurable memory management unit
- Supports reduced CPU and system clock speed for power saving

Advanced Memory Controller Features

- Supports glueless connection to two banks of ROM/SRAM/FLASH memory with programmable 8/16/32 bit data bus and programmable access timing
- Supports glueless connection to two SDRAM banks with programmable 8/16/32 bit data bus and programmable RAS/CAS latency
- Supports three external I/O banks with programmable 8/16/32 bit data bus and programmable access timing
- Programmable system clock speed for power management

Direct Memory Access (DMA) Engines

- Independent MAC DMA engine with programmable burst mode for WAN port
- Independent MAC DMA engine with programmable burst mode for LAN ports
- Supports little-endian byte ordering for memory buffers and descriptors
- Contains large independent receive and transmit FIFOs (3KB receive/3KB transmit) for back-to-back packet receive, and guaranteed no under-run packet transmit
- Data alignment logic and scatter gather capability

XceleRouter Technology

- Supports IPv4 IP header/TCP/UDP Packet checksum generation for host CPU off loading
- Supports IPv4 packet filtering based on checksum errors

Switch Engine

- 5-port 10/100 Integrated switch with one WAN and four LAN physical layer transceivers
- 16Kx32 on-chip SRAM for frame buffering
- 1.4Gbps on-chip memory bandwidth for wire-speed frame switching
- 10Mbps, 100Mbps modes of operations for both full and half duplex
- Supports port-based VLAN
- Support DiffServ priority, IEEE 802.1p-based priority or port-based priority
- Integrated address look-up engine, supports 1K absolute MAC addresses
- Automatic address learning, address aging, and address migration
- Broadcast storm protection
- Full-duplex IEEE 802.3x flow control
- Half-duplex back pressure flow control
- Supports IGMP snooping
- Spanning Tree Protocol support

Network Interface

- Features five MAC units and five PHY units
- Supports 10BASE-T and 100BASE-TX on all LAN ports and WAN port. Also supports 100BASE-FX on WAN port
- Supports automatic CRC generation and checking
- Supports automatic error packet discard
- Supports IEEE 802.3 auto-negotiation algorithm of full-duplex and half-duplex operation for 10Mbps and 100Mbps
- Supports full-/half-duplex operation on PHY interfaces
- Fully compliant with IEEE 802.3 Ethernet standards
- IEEE 802.3 full-duplex flow control and half-duplex backpressure collision flow control
- Supports MDI/MDI-X auto-crossover

Peripherals

- Twenty-eight interrupt sources, including four external interrupt sources
- Normal or fast interrupt mode (IRQ, FIQ) supported
- Prioritized interrupt handling
- Eight programmable general purpose I/O. Pins individually configurable to input, output, or I/O mode for dedicated signals
- Two programmable 32-bit timers with watchdog timer capability
- High-speed UART interface up to 115kbps

Other Features

- Integrated PLL to generate CPU and system clocks
- JTAG development interface for ICE connection
- 208-pin PQFP

Signal Description

System Level Hardware Interfaces

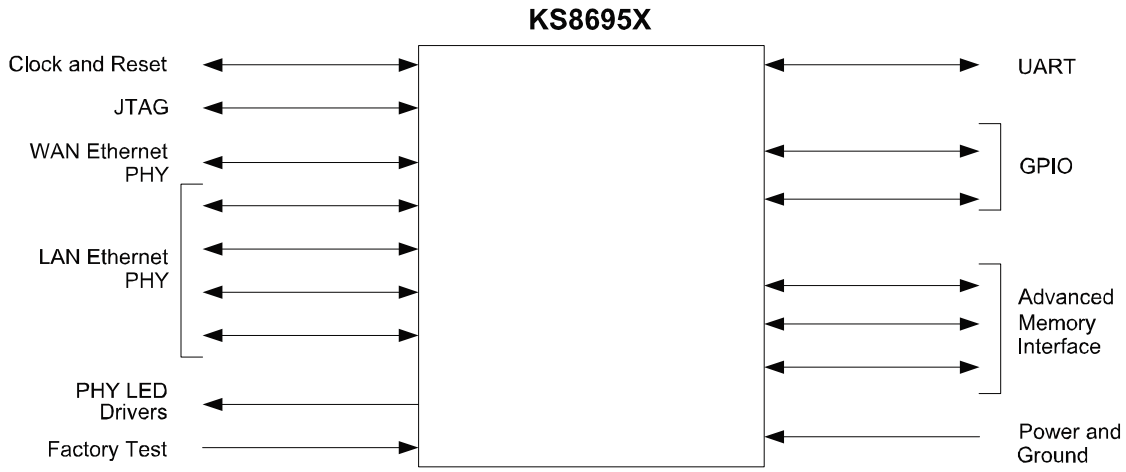


Figure 2. System Level Interfaces

At the system level the KS8695X features the following interfaces:

- Clock interface for crystal or external oscillator
- JTAG development interface
- One WAN Ethernet physical interface
- Four LAN Ethernet physical interfaces
- PHY LED drivers
- One high-speed UART interface
- Eight GPIO pins
- Advanced memory interface
  - Programmable synchronous bus rate
  - Programmable asynchronous interface timing
  - Independently programmable data bus width for static and synchronous memory
  - Glueless connection to SDRAM
  - Glueless connection to flash memory or ROM
- Factory test
- Power and ground

Configuration Pins

The following pins are sampled as input during reset.

Configuration	Pin Name	Pin #	Setting
Bank0 Flash Data Width	B0SIZE[1:0]	118, 119	‘00’= reserved ‘01’ = byte wide ‘10’ = half word wide (16 bits) ‘11’ = word wide (32 bits)
WRSTO Polarity	EROEN/WRSTPLS	85	‘0’ = active high ‘1’ = active low
CPU Clock Select	URTSN/CPUCLKSEL	96	‘0’ = normal mode (PLL) '1’ = bypass internal PLL

Table 1. Configuration Pins

Reset

The KS8695X has a single reset input that can be driven by a system reset circuit or a simple power on reset circuit. The KS8695X also features a reset output (WRSTO) that can be used to reset other devices in the system. WRSTO can be configured as either an active high reset or an active low reset through a strap-in option on pin 85 as shown in Table 1. The KS8695X also has a built in watchdog timer. Once the user programs the watchdog timer and the timer setting expires, the KS8695X will reset itself and also assert WRSTO to reset the other devices in the system. Figure 3 shows a typical system that uses the KS8695X WRSTO as the system reset.

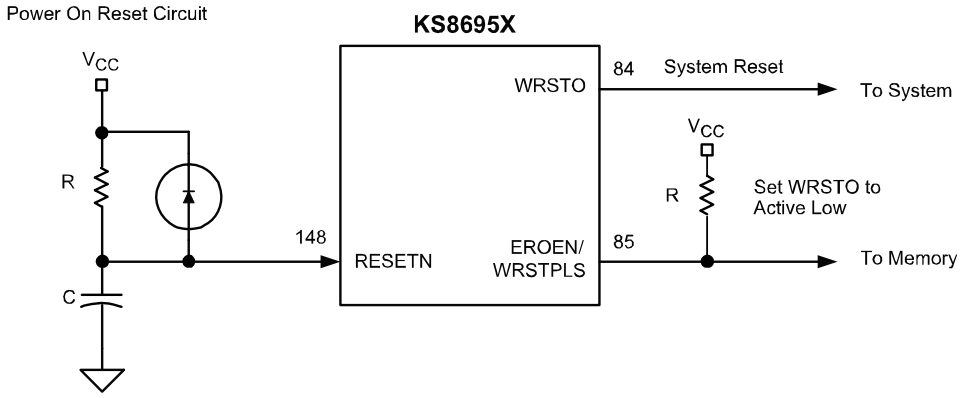


Figure 3. Example of a Reset Circuit

System Clock

The clock to the KS8695X can be supplied by either a 25MHz ±50ppm crystal or by an oscillator. If an oscillator is used it shall be connected to the X1 input (pin 150) on the KS8695X. If a crystal is used, it shall be connected with a circuit like the one shown below. The 25MHz input clock is used by an internal PLL to generate the programmable SDOCLK. SDOCLK is the system clock, and can be programmed from 25MHz to 125MHz using system clock and bus control register at offset 0x0004. The CPUCLKSEL strap-in option on pin 96 needs to be pulled low for normal operation.

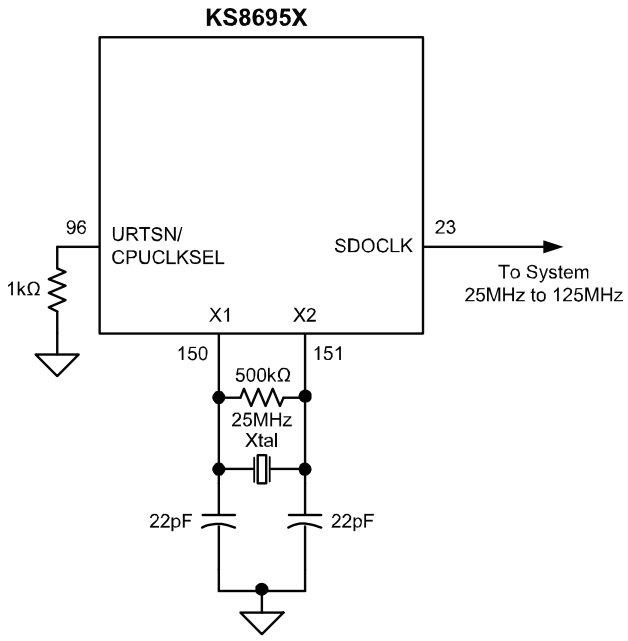


Figure 4. Typical Clock Circuit

Signal Descriptions by Group

Clock and Reset Pins

Pin	Name	I/O Type[1]	Description
150	XCLK1/ CPUCLK	I	External Clock In. This signal is used as the source clock for the transmit clock of the internal MAC and PHY. The clock frequency should be 25MHz ±50ppm. The XCLK1 signal is also used as the reference clock signal for the internal PLL togenerate the 125MHz internal system clock. CPUCLK: factory clock test input when the internal PLL is disabled (factory test signal).
151	XCLK2	I	External Clock In. Used with XCLK1 pin when another polarity of crystal is needed. This is unused for a normal clock input.
96	URTSN/ CPUCLKSEL	O/I	Normal Mode: UART request to send. Active low output. During reset: CPU clock select. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source. CPUCLKSEL=1 (factory test signal): the external clock to the CPUCLK pin is used as the internal CPU clock source.
148	RESETN	I	KS8695X chip reset. Active low input asserted for at least 256 system clock (40ns) cycles to reset the KS8695X. When in the reset state, all the output pins are tri-stated and all open drain signals are floating.
83	WRSTO	O	Watchdog timer reset output. This signal is asserted for at least 200ms if RESETN is asserted or when the internal watchdog timer expires.
85	EROEN/ WRSTPLS	O/I	Normal Mode: ROM/SRAM/FLASH and External I/O output enable. Active low. When asserted, this signal controls the output enable port of the specified device. During reset: Watchdog timer reset polarity setting. WRSTPLS=0, Active high; WRSTPLS=1, Active low. No default.

JTAG Interface Pins

Pin	Name	I/O Type[1]	Description
110	TCK	I	JTAG test clock.
111	TMS	I	JTAG test mode select.
112	TDI	I	JTAG test data in.
113	TDO	O	JTAG test data out.
114	TRSTN	I	JTAG test reset. Active low.

WAN Ethernet Physical Interface Pins

Pin	Name	I/O Type[1]	Description
159	WANRXP	I	WAN PHY receive signal + (differential).
160	WANRXM	I	WAN PHY receive signal – (differential).
162	WANTXM	O	WAN PHY transmit signal – (differential).
163	WANTXP	O	WAN PHY transmit signal + (differential).
158	WANFXSD/ DOUT	I/O	WAN fiber signal detect. Signal detect input when the WAN port is operated in 100BASE-FX 100Mb fiber mode. DOUT:factory analog test mode.

Note:

1. I = Input.
   O = Output.
   I/O = Bidirectional.
   O/I = Output in normal mode; input pin during reset.

LAN Ethernet Physical Interface Pins

Pin	Name	I/O Type[1]	Description
187 180 174 165	LANRXP[4:1]	I	LAN Port[4:1] PHY receive signal + (differential).
188 181 175 166	LANRXM[4:1]	I	LAN Port[4:1] PHY receive signal - (differential).
191 184 178 169	LANTXP[4:1]	O	LAN Port[4:1] PHY transmit signal + (differential).
190 183 177 168	LANTXM[4:1]	O	LAN Port[4:1] PHY transmit signal - (differential).
172	ISET	I	Set PHY transmit output current. Connect to ground through a 3.01kΩ 1% resistor.

PHY LED Drivers

Pin	Name	I/O Type[1]	Description
119	WLED0/ B0SIZE0	O/I	Normal Mode: WAN LED indicator 0. Programmable via WAN misc. Control register bits [2:0]. ‘000’ = Speed; ‘001’ = Link; ‘010’ = Full/half duplex; ‘011’ = Collision; ‘100’ = TX/RX activity; ‘101’ = Full-duplex collision; ‘110’ = Link/Activity. During reset: Bank 0 Data Access Size. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: ‘01’ = one byte, ‘10’ = half-word, ‘11’ = one word, and ‘00’ = reserved.
118	WLED1/ B0SIZE1	O/I	Normal Mode: WAN LED indicator 1. Programmable via WAN Misc. Control register bits [6:4]. ‘000’ = Speed; ‘001’= Link; ‘010’ = Full/half duplex; ‘011’ = Collision; ‘100’ = TX/RX activity; ‘101’ = Full-duplex collision; ‘110’ = Link/Activity. During reset: Bank 0 data access size. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: ‘01’= one byte, ‘10’ = half-word, ‘11’ = one word, and ‘00’ = reserved.
121 123 125 127	L[4:1]LED0	O	LAN Port[4:1] LED indicator 0. Programmable via switch control 0 register bits [27:25]. ‘000’ = Speed; ‘001’ = Link; ‘010’ = Full/half duplex; ‘011’ = Collision; ‘100’ = TX/RX activity; ‘101’ = Full-duplex collision; ‘110’ = Link/Activity.
120 122 124 126	L[4:1]LED1	O	LAN Port[4:1] LED indicator 1. Programmable via switch control 0 register bits [24:22]. ‘000’ = Speed; ‘001’ = Link; ‘010’ = Full/half duplex; ‘011’ = Collision; ‘100’ = TX/RX activity; ‘101’ = Full-duplex collision; ‘110’ = Link/Activity.

Note:

1. I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.

UART Pins

Pin	Name	I/O Type[1]	Description
92	URXD	I	UART receive data.
94	UTXD	O	UART transmit data.
93	UDTRN/ DBGENN	O	UART data terminal ready. Active low. Debug enable (factory test signal).
95	UDSRN	I	UART data set ready. Active low.
96	URTSN/ CPUCLKSEL	O/I	Normal mode: UART request to send. Active low output. During reset: CPU clock select. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source. CPUCLKSEL=1 (factory test signal), the external clock to the CPUCLK pin is used as the internal CPU clock source.
97	UCTSN/ BISTEN	I	UART clear to send. BIST enable (factory test signal).
98	UDCDN/ SCANEN	I	UART data carrier detect. Scan enable (factory test signal).
99	URIN/ TSTRST	I	UART ring indicator. Chip test reset (factory test signal).

General Purpose I/O Pins

Pin	Name	I/O Type[1]	Description
109	GPIO0/ EINT0	I/O	General purpose I/O pin/external interrupt request pin.
108	GPIO1/ EINT1	I/O	General purpose I/O pin/external interrupt request pin.
107	GPIO2/ EINT2	I/O	General purpose I/O pin/external interrupt request pin.
106	GPIO3/ EINT3	I/O	General purpose I/O pin/external interrupt request pin.
105	GPIO4/ TOUT0	I/O	General purpose I/O pin/timer 0 output pin.
102	GPIO5/ TOUT1	I/O	General purpose I/O pin/timer 1 output pin.
101	GPIO6	I/O	General purpose I/O pin.
100	GPIO7	I/O	General purpose I/O pin.

Note:

1. I = Input.
   O = Output.
   I/O = Bidirectional.
   O/I = Output in normal mode; input pin during reset.

Resered Pins

Pin	Name	I/O Type[1]	Description
84	TEST3	NC	The **Reserved Pins** serve as no connect in order to ensure correct operation of the device. **DO NOT** connect any signal to these pins.
130	TEST4	NC	No connect.
131	TEST5	NC	No connect.
132	TEST6	NC	No connect.
133	TEST7	NC	No connect.
134	TEST8	NC	No connect.
135	TEST9	NC	No connect.
136	TEST10	NC	No connect.
139	TEST11	NC	No connect.
140	TEST12	NC	No connect.
141	TEST13	NC	No connect.
142	TEST14	NC	No connect.
143	TEST15	NC	No connect.
144	TEST16	NC	No connect.
145	TEST17	NC	No connect.
146	TEST18	NC	No connect.
147	TEST19	NC	No connect.

Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O)

Pin	Name	I/O Type[1]	Description
24	SDICLK	I	SDRAM Clock In: SDRAM clock input for the SDRAM memory controller interface.
23	SDOCLK	O	System/SDRAM Clock Out: Output of the internal system clock, it is also used as the clock signal for SDRAM interface.
205	ADDR21/BA1	O	Address Bit 21/Bank Address Input 1: Address bit 21 for asynchronous accesses. Bank Address Input bit 1 for SDRAM accesses.
206	ADDR20/BA0	O	Address Bit 20/Bank Address Input 0: Address bit 20 for asynchronous accesses. Bank Address Input bit 0 for SDRAM accesses.
198 199 200 201 202 203 204 207 208 3 4 5 6 7 8 9 10 13 14 15	ADDR[19] ADDR[18] ADDR[17] ADDR[16] ADDR[15] ADDR[14] ADDR[13] ADDR[12] ADDR[11] ADDR[10] ADDR[9] ADDR[8] ADDR[7] ADDR[6] ADDR[5] ADDR[4] ADDR[3] ADDR[2] ADDR[1] ADDR[0]	O	Address Bus: The 22-bit address bus (including ADDR[21:20] above) covers 4M word memory space shared by ROM/SRAM/FLASH, SDRAM, and external I/O banks. During the SDRAM cycles, the internal address bus is used to generate RAS and CAS addresses for the SDRAM. The number of column address bits in the SDRAM banks can be programmed from 8 to 11 bits via the SDRAM control registers. ADDR[12:0] are the SDRAM address, and ADDR[21:20] are the SDRAM bank address. During other cycles, the ADDR[21:0] is the byte address of the data transfer. Note: The address pinout non-sequential by design. It is optimized for board level connections to SDRAM. For SDRAM and ROM/SRAM/Flash, connect ADDR[0] to A0 on the memory, ADDR[1] to A1 on the memory, and so forth. Address bit mapping for 8-bit, 16-bit, 32-bit access. For external I/O devices, the system designer must connect address lines conventionally for 8-bit, 16-bit, and 32-bit access.

Note:
1. I = Input.
   O = Output.
   NC = No connect.

Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O) (continued)

Pin	Name	I/O Type[1]	Description
31 32 33 36 37 38 39 40 41 42 45 46 49 50 51 52 55 56 57 58 59 60 61 62 65 66 67 68 69 70 71 72	DATA[31] DATA[30] DATA[29] DATA[28] DATA[27] DATA[26] DATA[25] DATA[24] DATA[23] DATA[22] DATA[21] DATA[20] DATA[19] DATA[18] DATA[17] DATA[16] DATA[15] DATA[14] DATA[13] DATA[12] DATA[11] DATA[10] DATA[9] DATA[8] DATA[7] DATA[6] DATA[5] DATA[4] DATA[3] DATA[2] DATA[1] DATA[0]	I/O	External DATA Bus. 32-bit bidirectional data bus for data transfer. KS8695X also supports 8- and 16-bit data bus widths.
16 17	SDCSN[1] SDCSN[0]	O	SDRAM Chip Select: Active low chip select pins for SDRAM. The KS8695X supports up to two SDRAM banks. One SDCSN output is provided for each bank.
18	SDRASN	O	SDRAM Row Address Strobe: Active low. The row address strobe pin for SDRAM.
19	SDCASN	O	SDRAM Column Address Strobe: Active low. The column address strobe pin for SDRAM.
20	SDWEN	O	SDRAM Write Enable: Active low. The write enable signal for SDRAM.
27 28 29 30	SDQM[3] SDQM[2] SDQM[1] SDQM[0]	O	SDRAM Data Input/Output Mask: Data input/output mask signals for SDRAM. The SDQM is sampled high and is an output mask signal for write accesses and an output enable signal for read accesses. Input data are masked during a write cycle. The SDQM0/1/2/3 correspond to XDATA[7:0], XDATA[15:8], XDATA[23:16] and XDATA[31:24], respectively.
75 76 77	ECSN[2] ECSN[1] ECSN[0]	O	External I/O Device Chip Select: Active low. Three external I/O banks are provided for external memory mapped I/O operations. Each I/O bank stores up to 16KB. The ECSNx signals indicate which of the three I/O banks is selected.

Note:
1. O = Output.
   I/O = Bidirectional.

Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O) (continued)

Pin	Name	I/O Type[1]	Description
78	EWAITN	I	External wait: Active low. This signal is asserted when an external I/O device or a ROM/SRAM/FLASH bank needs more access cycles than those defined in the corresponding control register.
81 82	RCSN[1] RCSN[0]	O	ROM/SRAM/FLASH chip select: Active low. The KS8695X can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
85	EROEN/ WRSTPLS	O/I	Normal mode: External I/O and ROM/SRAM/FLASH output enable:Active low. When asserted, this signal controls the output enable port of the specified memory device. During reset: Watchdog timer reset polarity setting. WRSTPLS=0, Active low; WRSTPLS = 1, active high. No default.
89	ERWEN0/ TESTACK	O	External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory test signal).
88	ERWEN1/ TESTREQB	O	External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory test signal).
87	ERWEN2/ TESTREQA	O	External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device except SDRAM). ARM CPU test signal (factory test signal).
86	ERWEN3/ TICTESTENN	O	External I/O and ROM/SRAM/FLASH write byte enable. Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory test signal).
119	WLED0/ B0SIZE0	O/I	Normal mode: WAN LED indicator 0:Programmable via WAN misc. Control register bits [2:0]. 000 = Speed; 001 = Link; 010 = Full/half duplex; 011 = Collision; 100 = TX/RX activity; 101 = Full-duplex collision; 110 = Link/Activity. During reset: Bank 0 data access size. Bank 0 is used for the boot program. B0SiZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved.
118	WLED1/ B0SIZE1	O/I	Normal mode: WAN LED indicator 1:Programmable via WAN Misc. Control register bits [6:4]. 000 = Speed; 001 = Link; 010 = Full/half duplex; 011 = Collision; 100 = TX/RX activity; 101 = Full-duplex collision; 110 = Link/Activity. During reset: Bank 0 data access size. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved.

Factory Test Pins

Pin	Name	I/O Type[1]	Description
117	TESTEN	I	Chip test enable: (factory test signal), pull down if not used.
197	TEST1	I	PHY test pin: (factory test signal).
149	TEST2	I	PHY test pin: (factory test signal).

Note:

1. I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.

Power and Ground Pins

Pin	Name	I/O Type[1]	Description
152	VDDA-PLL	P	1.8V analog V_{DD} for PLL.
173 179	VDDAT	P	2.5V/3.3V analog V_{DD}. These pins can use voltage of either 2.5V or 3.3V.
154 157 170 186 193 195	VDDAR	P	1.8V analog V_{DD}.
25 43 90 115 128	VDD-CORE	P	1.8V digital core V_{DD}.
1 11 21 34 47 53 63 73 79 103 137	VDD-IO	P	3.3V digital I/O circuitry V_{DD}.
26 44 91 116 129	VSS-CORE	Gnd	Digital core V_{SS}.
2 12 22 35 48 54 64 74 80 104 138	VSS-IO	Gnd	Digital I/O V_{SS}.

Note:
1. P = Power supply.
   Gnd = Ground.

Power and Ground Pins (continued)

Pin	Name	I/O Type[1]	Description
153 155 156 161 164 167 171 176 182 185 189 192 194 196	GNDA	Gnd	Analog Ground.

Note:
1. Gnd = Ground.

Address Map and Register Description

Memory Map

Upon power up, the KS8695X memory map is configured as shown below.

Address Range	Region	Description
0x03FF0000-0x03FFFFFF	64KB	KS8695PX System Configuration Register Space
0x02000000-0x03FEFFFF	32MB	Not Configured
0x00000000-0x01FFFFFF	32MB	Flash Bank 0

Memory Map Example

The default base address for the KS8695X system configuration registers is 0x03ff0000. After power up, the user is free to remap the memory for their specific application. The following is an example of the memory space remapped for operation.

Address Range	Region	Description
0x03FF0000-0x03FFFFFF	64KB	KS8695PX System Configuration Register Space
0x02900000-0x03FEFFFF	23MB	Spare (External I/O)
0x02100000-0x028FFFFF	8MB	FLASH
0x00100000-0x020FFFFF	32MB	SDRAM
0x00000000-0x0007FFFF	512KB	SRAM

Register Description

The KS8695X system configuration registers (SCRs) are located in a block of 64KB in the host memory address space. After power up and initialization, the user can remap the SCRs to a desired offset. The SCRs are 32 bits wide. They are 32 bit word-aligned and must be accessed using word instructions. A description of the KS8695X system configuration registers follows. For bit definitions, please see the detailed "Register Description" section.

Address	Description	Mode	Size
System Registers			
0x0000	System Configuration Register	R/W	[31:0]
0x0004	System Clock and Bus Control Register	R/W	[31:0]
Memory Controller Interface Registers			
0x4000	External I/O Access Control Register 0	R/W	[31:0]
0x4004	External I/O Access Control Register 1	R/W	[31:0]
0x4008	External I/O Access Control Register 2	R/W	[31:0]
0x4010	ROM/SRAM/FLASH Control Register 0	R/W	[31:0]
0x4014	ROM/SRAM/FLASH Control Register 1	R/W	[31:0]
0x4020	ROM/SRAM/FLASH General Register	R/W	[31:0]
0x4030	SDRAM Control Register 0	R/W	[31:0]
0x4034	SDRAM Control Register 1	R/W	[31:0]
0x4038	SDRAM General Control Register	R/W	[31:0]
0x403C	SDRAM Buffer Control Register	R/W	[31:0]
0x4040	SDRAM Refresh Timer Register	R/W	[31:0]

Address	Description	Mode	Size
WAN DMA Registers			
0x6000	WAN MAC DMA Transmit Control Register	R/W	[31:0]
0x6004	WAN MAC DMA Receive Control Register	R/W	[31:0]
0x6008	WAN MAC DMA Transmit Start Command Register	R/W	[31:0]
0x600C	WAN MAC DMA Receive Start Command Register	R/W	[31:0]
0x6010	WAN Transmit Descriptor List Base Address Register	R/W	[31:0]
0x6014	WAN Receive Descriptor List Base Address Register	R/W	[31:0]
0x6018	WAN MAC Station Address Low Register	R/W	[31:0]
0x601C	WAN MAC Station Address High Register	R/W	[31:0]
0x6080	WAN MAC Additional Station Address Low Register 0	R/W	[31:0]
0x6084	WAN MAC Additional Station Address High Register 0	R/W	[31:0]
0x6088	WAN MAC Additional Station Address Low Register 1	R/W	[31:0]
0x608C	WAN MAC Additional Station Address High Register 1	R/W	[31:0]
0x6090	WAN MAC Additional Station Address Low Register 2	R/W	[31:0]
0x6094	WAN MAC Additional Station Address High Register 2	R/W	[31:0]
0x6098	WAN MAC Additional Station Address Low Register 3	R/W	[31:0]
0x609C	WAN MAC Additional Station Address High Register 3	R/W	[31:0]
0x60A0	WAN MAC Additional Station Address Low Register 4	R/W	[31:0]
0x60A4	WAN MAC Additional Station Address High Register 4	R/W	[31:0]
0x60A8	WAN MAC Additional Station Address Low Register 5	R/W	[31:0]
0x60AC	WAN MAC Additional Station Address High Register 5	R/W	[31:0]
0x60B0	WAN MAC Additional Station Address Low Register 6	R/W	[31:0]
0x60B4	WAN MAC Additional Station Address High Register 6	R/W	[31:0]
0x60B8	WAN MAC Additional Station Address Low Register 7	R/W	[31:0]
0x60BC	WAN MAC Additional Station Address High Register 7	R/W	[31:0]
0x60C0	WAN MAC Additional Station Address Low Register 8	R/W	[31:0]
0x60C4	WAN MAC Additional Station Address High Register 8	R/W	[31:0]
0x60C8	WAN MAC Additional Station Address Low Register 9	R/W	[31:0]
0x60CC	WAN MAC Additional Station Address High Register 9	R/W	[31:0]
0x60D0	WAN MAC Additional Station Address Low Register 10	R/W	[31:0]
0x60D4	WAN MAC Additional Station Address High Register 10	R/W	[31:0]
0x60D8	WAN MAC Additional Station Address Low Register 11	R/W	[31:0]
0x60DC	WAN MAC Additional Station Address High Register 11	R/W	[31:0]
0x60E0	WAN MAC Additional Station Address Low Register 12	R/W	[31:0]
0x60E4	WAN MAC Additional Station Address High Register 12	R/W	[31:0]
0x60E8	WAN MAC Additional Station Address Low Register 13	R/W	[31:0]
0x60EC	WAN MAC Additional Station Address High Register 13	R/W	[31:0]
0x60F0	WAN MAC Additional Station Address Low Register 14	R/W	[31:0]
0x60F4	WAN MAC Additional Station Address High Register 14	R/W	[31:0]
0x60F8	WAN MAC Additional Station Address Low Register 15	R/W	[31:0]
0x60FC	WAN MAC Additional Station Address High Register 15	R/W	[31:0]

Address	Description	Mode	Size
LAN DMA Registers			
0x8000	LAN MAC DMA Transmit Control Register	R/W	[31:0]
0x8004	LAN MAC DMA Receive Control Register	R/W	[31:0]
0x8008	LAN MAC DMA Transmit Start Command Register	R/W	[31:0]
0x8010	LAN Transmit Descriptor List Base Address	R/W	[31:0]
0x8014	LAN Receive Descriptor List Base Address	R/W	[31:0]
0x8018	LAN MAC Station Address Low Register	R/W	[31:0]
0x801C	LAN MAC Station Address High Register	R/W	[31:0]
0x8080	LAN MAC Additional Station Address Register Low 0	R/W	[31:0]
0x8084	LAN MAC Additional Station Address Register High 0	R/W	[31:0]
0x8088	LAN MAC Additional Station Address Register Low 1	R/W	[31:0]
0x808C	LAN MAC Additional Station Address Register High 1	R/W	[31:0]
0x8090	LAN MAC Additional Station Address Register Low 2	R/W	[31:0]
0x8094	LAN MAC Additional Station Address Register High 2	R/W	[31:0]
0x8098	LAN MAC Additional Station Address Register Low 3	R/W	[31:0]
0x809C	LAN MAC Additional Station Address Register High 3	R/W	[31:0]
0x80A0	LAN MAC Additional Station Address Register Low 4	R/W	[31:0]
0x80A4	LAN MAC Additional Station Address Register High 4	R/W	[31:0]
0x80A8	LAN MAC Additional Station Address Register Low 5	R/W	[31:0]
0x80AC	LAN MAC Additional Station Address Register High 5	R/W	[31:0]
0x80B0	LAN MAC Additional Station Address Register Low 6	R/W	[31:0]
0x80B4	LAN MAC Additional Station Address Register High 6	R/W	[31:0]
0x80B8	LAN MAC Additional Station Address Register Low 7	R/W	[31:0]
0x80BC	LAN MAC Additional Station Address Register High 7	R/W	[31:0]
0x80C0	LAN MAC Additional Station Address Register Low 8	R/W	[31:0]
0x80C4	LAN MAC Additional Station Address Register High 8	R/W	[31:0]
0x80C8	LAN MAC Additional Station Address Register Low 9	R/W	[31:0]
0x80CC	LAN MAC Additional Station Address Register High 9	R/W	[31:0]
0x80D0	LAN MAC Additional Station Address Register Low 10	R/W	[31:0]
0x80D4	LAN MAC Additional Station Address Register High 10	R/W	[31:0]
0x80D8	LAN MAC Additional Station Address Register Low 11	R/W	[31:0]
0x80DC	LAN MAC Additional Station Address Register High 11	R/W	[31:0]
0x80E0	LAN MAC Additional Station Address Register Low 12	R/W	[31:0]
0x80E4	LAN MAC Additional Station Address Register High 12	R/W	[31:0]
0x80E8	LAN MAC Additional Station Address Register Low 13	R/W	[31:0]
0x80EC	LAN MAC Additional Station Address Register High 13	R/W	[31:0]
0x80F0	LAN MAC Additional Station Address Register Low 14	R/W	[31:0]
0x80F4	LAN MAC Additional Station Address Register High 14	R/W	[31:0]
0x80F8	LAN MAC Additional Station Address Register Low 15	R/W	[31:0]
0x80FC	LAN MAC Additional Station Address Register High 15	R/W	[31:0]

Address	Description	Mode	Size
UART Registers			
0xE000	UART Receive Buffer Register	R/W	[31:0]
0xE004	UART Transmit Holding Register	R/W	[31:0]
0xE008	UART FIFO Control Register	R/W	[31:0]
0xE00C	UART Line Control Register	R/W	[31:0]
0xE010	UART Modem Control Register	R/W	[31:0]
0xE014	UART Line Status Register	R/W	[31:0]
0xE018	UART Modem Status Register	R/W	[31:0]
0xE01C	UART Baud Rate Divisor Register	R/W	[31:0]
0xE020	UART Status Register	R/W	[31:0]
Interrupt Controller Registers			
0xE200	Interrupt Mode Control Register	R/W	[31:0]
0xE204	Interrupt Enable Register	R/W	[31:0]
0xE208	Interrupt Status Register	R/W	[31:0]
0xE210	Not Used	NA	NA
0xE20C	Interrupt Priority Register for WAN MAC	R/W	[31:0]
0xE214	Interrupt Priority Register for LAN MAC	R/W	[31:0]
0xE218	Interrupt Priority Register for Timer	R/W	[31:0]
0xE21C	Interrupt Priority Register for UART	R/W	[31:0]
0xE220	Interrupt Priority Register for External Interrupt	R/W	[31:0]
0xE224	Interrupt Priority Register for Communications Channel	R/W	[31:0]
0xE228	Interrupt Bus Error Response Register	R/W	[31:0]
0xE22C	Interrupt Mask Status Register	R/W	[31:0]
0xE230	Interrupt Pending Highest Priority Register for FIQ	R/W	[31:0]
0xE234	Interrupt Pending Highest Priority Register for IRQ	R/W	[31:0]
Timer Registers			
0xE400	Timer Control Register	R/W	[31:0]
0xE404	Timer 1 Timeout Count Register	R/W	[31:0]
0xE408	Timer 0 Timeout Count Register	R/W	[31:0]
0xE40C	Timer 1 Pulse Count Register	R/W	[31:0]
0xE410	Timer 0 Pulse Count Register	R/W	[31:0]
General Purpose I/O Registers			
0xE600	I/O Port Mode Register	R/W	[31:0]
0xE604	I/O Port Control Register	R/W	[31:0]
0xE608	I/O Port Data Register	R/W	[31:0]

Address	Description	Mode	Size
Switch Engine Configuration Registers			
0xE800	Switch Engine Control 0 Register	R/W	[31:0]
0xE804	Switch Engine Control 1 Register	R/W	[31:0]
0xE808	Port 1 Configuration Register	R/W	[31:0]
0xE80C	Port 2 Configuration Register	R/W	[31:0]
0xE810	Port 3 Configuration Register	R/W	[31:0]
0xE814	Port 4 Configuration Register	R/W	[31:0]
0xE818	Port 5 Configuration Register	R/W	[31:0]
0xE81C	Ports 1 and 2 Auto Negotiation (AN) Register	R/W	[31:0]
0xE820	Ports 3 and 4 Auto Negotiation (AN) Register	R/W	[31:0]
0xE824	Look-up Engine (LUE) Control Register	R/W	[31:0]
0xE828	Look-up Engine (LUE) Indirect Register High	R/W	[31:0]
0xE82C	Look-up Engine (LUE) Indirect Register Low	R/W	[31:0]
0xE830	Advance Feature Control Register	R/W	[31:0]
0xE834	DSCP Register High	R/W	[31:0]
0xE838	DSCP Register Low	R/W	[31:0]
0xE83C	Switch Engine MAC Address Register High	R/W	[31:0]
0xE840	Switch Engine MAC Address Register Low	R/W	[31:0]
0xE844	Management Counter Indirect Access Register	R/W	[31:0]
0xE848	Management Counter Data Register	R/W	[31:0]
0xE84C	Ports 1 and 2 PHY Power Management	R/W	[31:0]
0xE850	Ports 3 and 4 PHY Power Management	R/W	[31:0]
Miscellaneous Registers			
0xEA00	Device ID Register	R/W	[31:0]
0xEA04	Revision ID Register	R/W	[31:0]
0xEA08	Not Used	NA	NA
0xEA0C	WAN Miscellaneous Control Register	R/W	[31:0]
0xEA10	WAN PHY Power Management Register	R/W	[31:0]

Absolute Maximum Ratings[1]

Supply Voltage
(V_{DDAR},V_{DDA_PLL},V_{DD_CORE}) ..... –0.5V to +2.4V
(V_{DDAT},V_{DD_IO}) ..... –0.5V to +4.0V
Input Voltage (all inputs) ..... –0.5V to +4.0V
Output Voltage (all outputs) ..... –0.5V to +4.0V
Lead Temperature (soldering, 10sec.) ..... 270°C
Pb (Lead) Free Temperature (soldering, 10sec.) ..... 260°C
Storage Temperature (T_s) ..... –55°C to +150°C

Operating Ratings[2]

Supply voltage
(V_{DDAR},V_{DDA_PLL},V_{DD_CORE}) ..... +1.7V to +1.9V
(V_{DDAT})[3] ..... +2.4V to +2.6V
(V_{DDAT})[3] ..... +3.135V to +3.456V
(V_{DD_IO}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –0°C to +70°C
Junction Temperature (T_J) ..... 150°C
Package Thermal Resistance[4]
PQFP (θ_{JA}) No Air Flow ..... 39.1°C/W

Electrical Characteristics[5]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Total Supply Current (including TX output driver current) 100BASE-TX Operation: All ports 100% Utilization, SDOCLK = 125MHz						
I_{DX}	100BASE-TX (Analog I/O)	V_{DDAT} = +2.5V or +3.3V		0.220		A
I_{RX}, I_{DDC}	100BASE-TX (Analog RX, Digital Core)	V_{DDA_PLL}, V_{DDAR}, V_{DD_CORE} = +1.8V		0.223		A
I_{DDIO}	100BASE-T (Digital I/O)	V_{DD_IO} = +3.3V		0.164		A
10BASE-TX Operation: All ports 100% Utilization, SDOCLK = 125MHz						
I_{DX}	10BASE-TX (Analog I/O)	V_{DDAT} = +2.5V or +3.3V		0.165		A
I_{RX}, I_{DDC}	10BASE-TX (Analog RX, Digital Core)	V_{DDA_PLL}, V_{DDAR}, V_{DD_CORE} = +1.8V		0.333		A
I_{DDIO}	10BASE-T (Digital I/O)	V_{DD_IO} = +3.3V		0.133		A
Auto-Negotiation Mode: SDOCLK = 125MHz						
I_{DX}	10BASE-TX (Analog I/O)	V_{DDAT} = +2.5V or +3.3V		0.033		A
I_{RX}, I_{DDC}	10BASE-TX (Analog RX Digital Core)	V_{DDA_PLL}, V_{DDAR}, V_{DD_CORE} = +1.8V		0.216		A
I_{DDIO}	10BASE-T (Digital I/O)	V_{DD_IO} = +3.3V		0.118		A
TTL Inputs						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current (Excluding pull-up/pull-down)	V_{IN} = GND = V_{DD_IO}	–10		10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –8mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			+0.4	V
I_{OZ}	Output Tri-state Leakage				10	µA
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination on the differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination on the differential output			2	%
t_r, t_t	Rise/Fall Time Rise/Fall Time Imbalance		3 0		5 0.5	ns ns
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			0.5		V
	Output Jitters	Peak-to-peak		0.7	1.4	ns

Symbol	Parameter	Condition	Min	Typ	Max	Units
10BASE-TX Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
10BASE-TX Transmit (measured differentially after 1:1 transformer) V_{DDAT} = 2.5V						
V_P	Peak Differential Output Voltage	100Ω termination on the differential output		2.3		V
	Jitters Added	100Ω termination on the differential output			±3.5	ns
	Rise/Fall Time			28	30	ns

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).
3. V_{DDAT} can operate from either a 2.5V or 3.3V supply.
4. No heat spreader in package.
5. Specification for packaged product only.

LDO Options

For a standalone SOHO system using the KS8695X, Micrel recommends the following low-cost LDO bundle:

- One MIC5209BM for the +1.8V digital supply (V_{DD_CORE})
- One MIC5209-3.3BS for the +3.3V digital I/O supply (V_{DD_IO}) and analog transmit supply (V_{DDAT})

Since each system may have a different power requirement, be sure to contact your Micrel sales representative or Field Application Engineer to help you find a cost-effective LDO solution for your project.

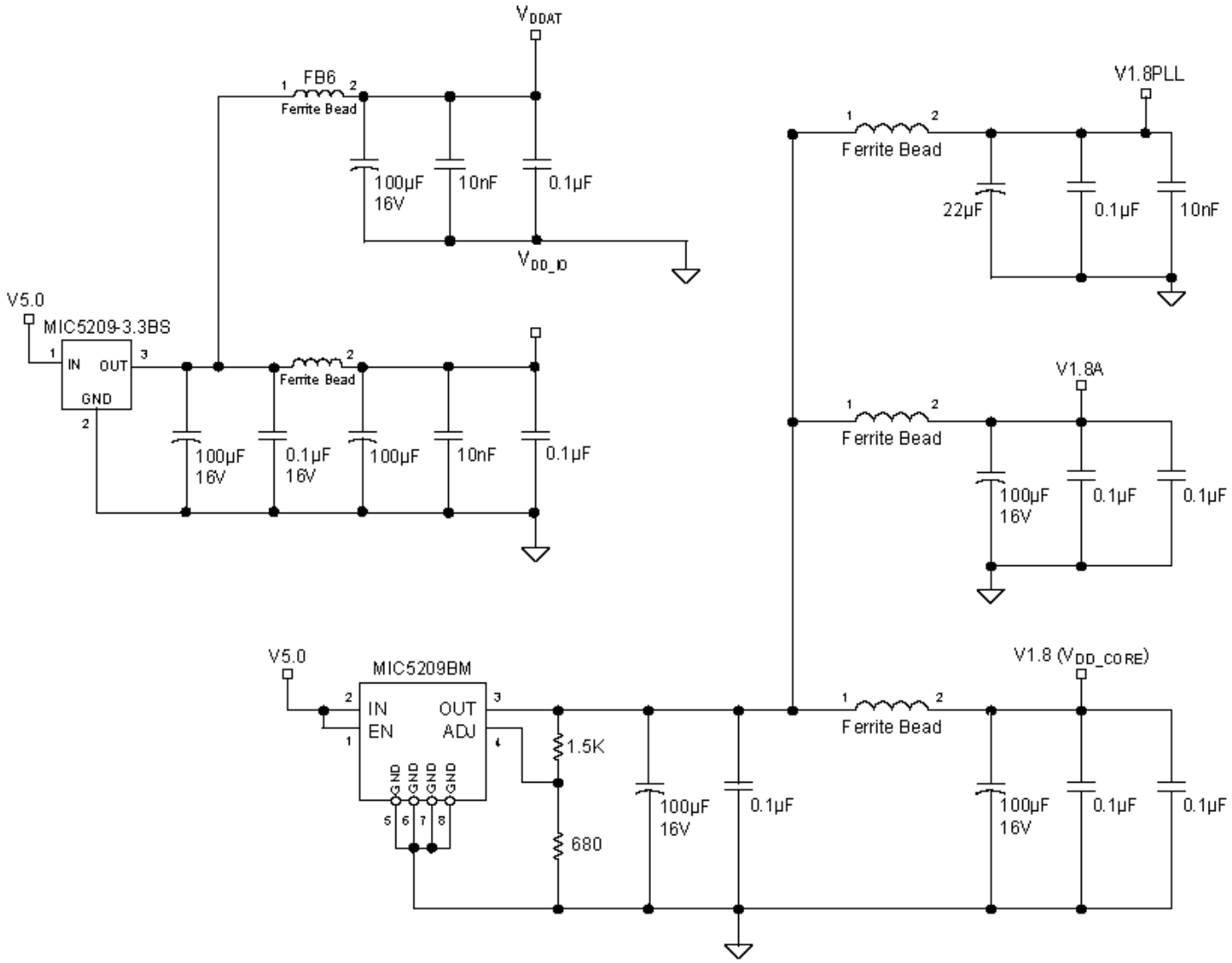


Figure 5. Low-Cost LDO Option

Timing Diagrams

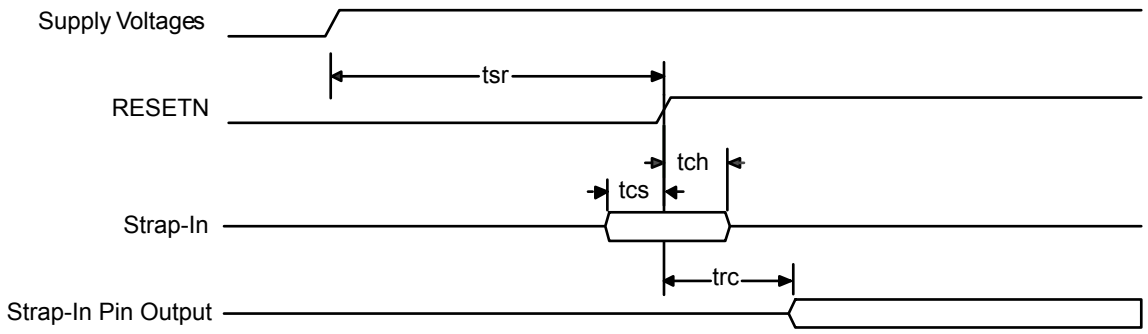


Figure 6. Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable supply voltages to reset high	10			ms
t_{CS}	Configuration set-up time	50			ns
t_{CH}	Configuration hold time	50			ns
t_{RC}	Reset to strap-in pin output	50			µs

Table 2. Reset Timing Parameters

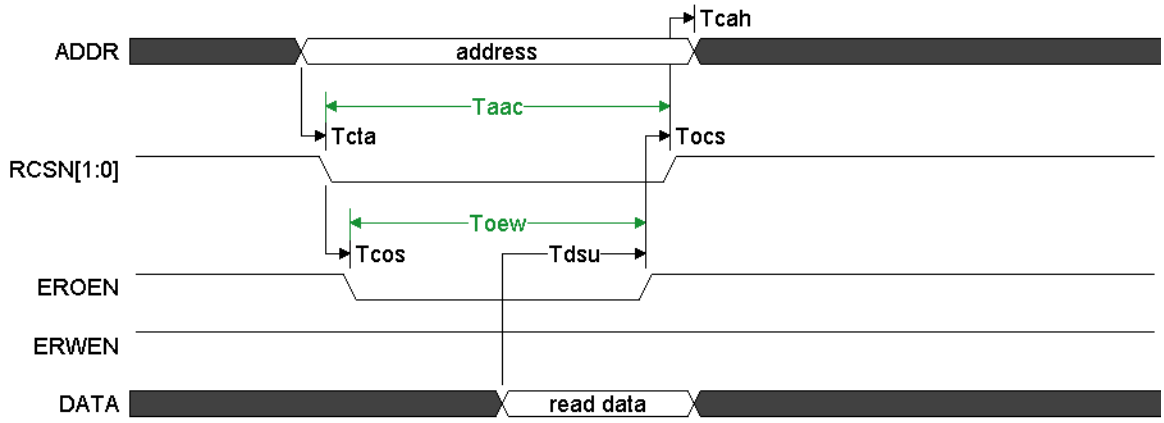


Figure 7. Static/Flash Memory Read Cycle

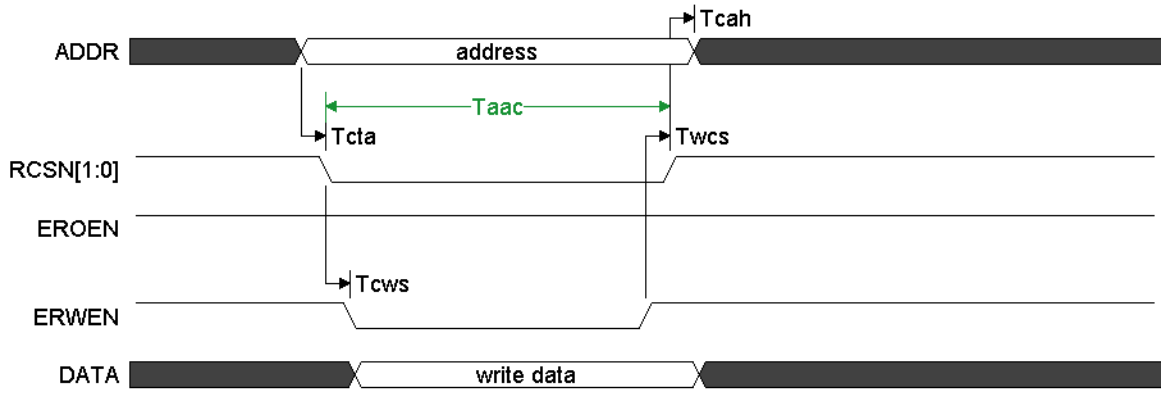


Figure 8. Static/Flash Memory Write Cycle

Symbol	Parameter	Min	Typ	Max	Units
T_{cta}	Valid address to CS setup time	0.8	1.1	1.3	ns
T_{cos}	OE valid to CS setup time	0.6	0.6	1.0	ns
T_{aac}	Address access time	RBiTACC	+1.0	RBiTACC	ns
T_{dsu}	Valid read data to OE setup time	2.0			ns
T_{cws}	CS valid to WE setup time	0.6	0.6	1.0	ns
T_{cah}	Address to CS hold time	1.0	1.0	1.4	ns
T_{ocs}	Rising edge OE to CS hold time	0			ns
T_{oew}	OE pulsewidth	RBiTACC	RBiTACC	RBiTACC	ns
T_{wcs}	Rising edge WE to OE hold time	0			ns

Table 3. Static/Flash Memory Timing Parameters

Symbol	Parameter[1]	Registers
RBiTACC	Programmable bank i access time	0x4010, 0x4014

Table 4. Programmable Static Memory Timing Parameters

Note:

1. "i" Refers to chip select parameters 0 and 1.

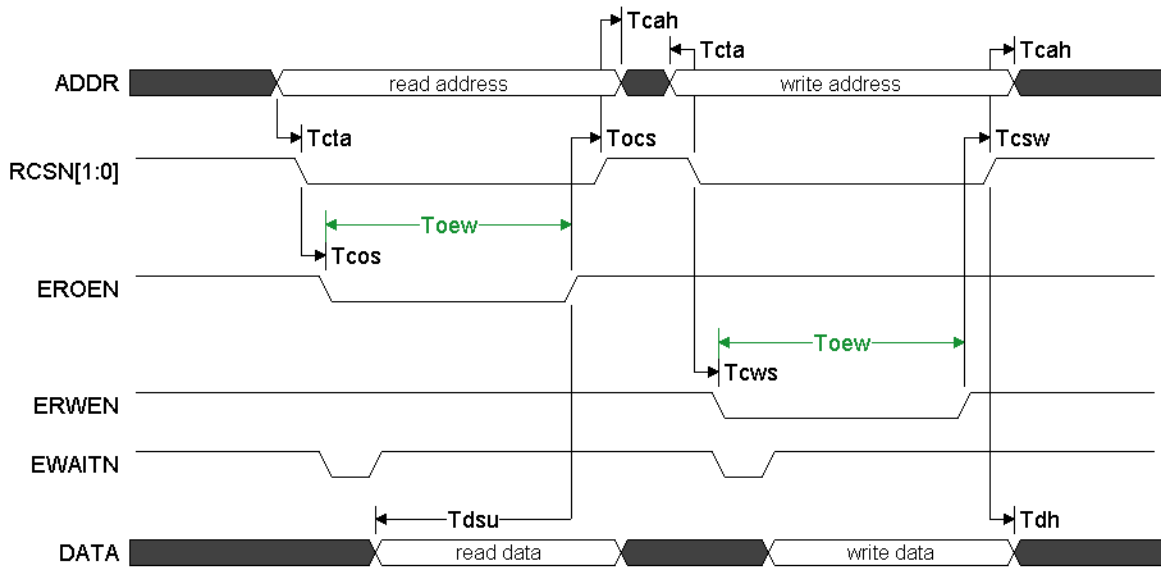


Figure 9. External I/O Read and Write Cycles

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Units
T_{cta}	Valid address to CS setup	EBiTACS +0.8	EBiTACS +1.1	EBiTACS +1.3	ns
T_{cos}	CS valid to OE setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dsu}	Valid read data to OE setup time	2.0			ns
T_{cws}	CS valid to WE setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dh}	CS to write data hold time	0			ns
T_{cah}	CS to ADDR hold time	EBiTCOH +1.0	EBiTCOH +1.0	EBiTCOH +1.4	ns
T_{oew}	OE/WE pulsewidth	EBiTACT		EBiTACT	ns
T_{ocs}, T_{csw}	Rising edge OE/WE to CS hold time	0			ns

Table 5. External I/O Memory Timing Parameters

Note:

1. Measurements for minimum were taken at 0°C, typical at 25°C, and maximum at 100°C.

Symbol	Parameter[1]	Registers
EBiTACS	Programmable bank i address setup time before chip select	0x4000, 0x4004, 0x4008
EBiTACT	Programmable bank i write enable/output enable access time	0x4000, 0x4004, 0x4008
EBiTCOS	Programmable bank i chip select setup time before OEN	0x4000, 0x4004, 0x4008
EBiTCOH	Programmable bank i chip select hold time	0x4000, 0x4004, 0x4008

Table 6. Programmable External I/O Timing Parameters

Note:

1. "i" Refers to chip select parameters 0, 1, or 2.

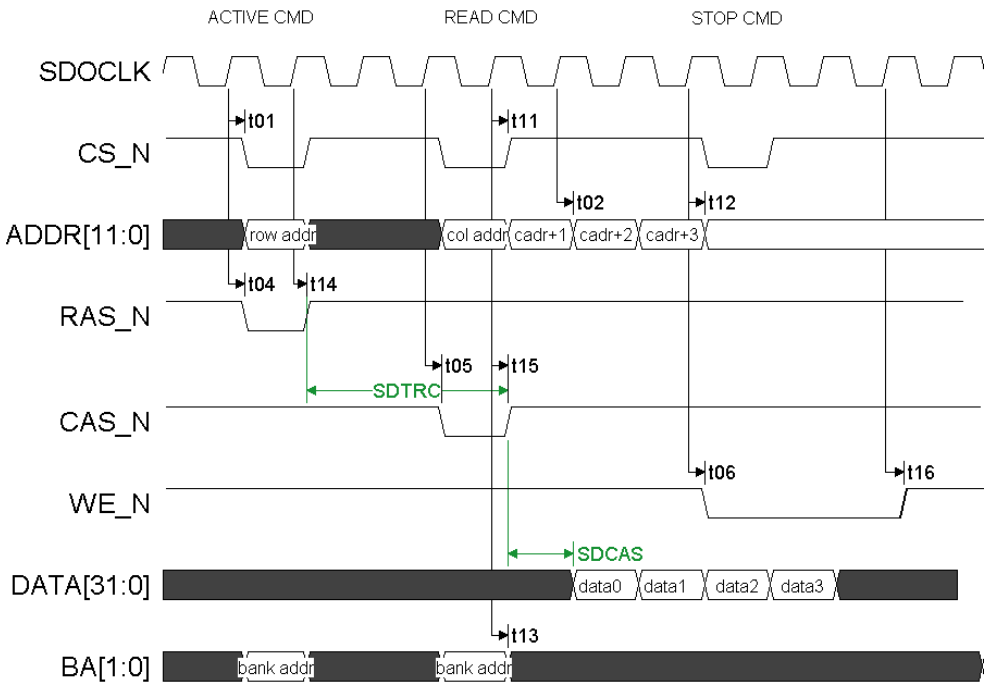


Figure 10. SDRAM Read Timing

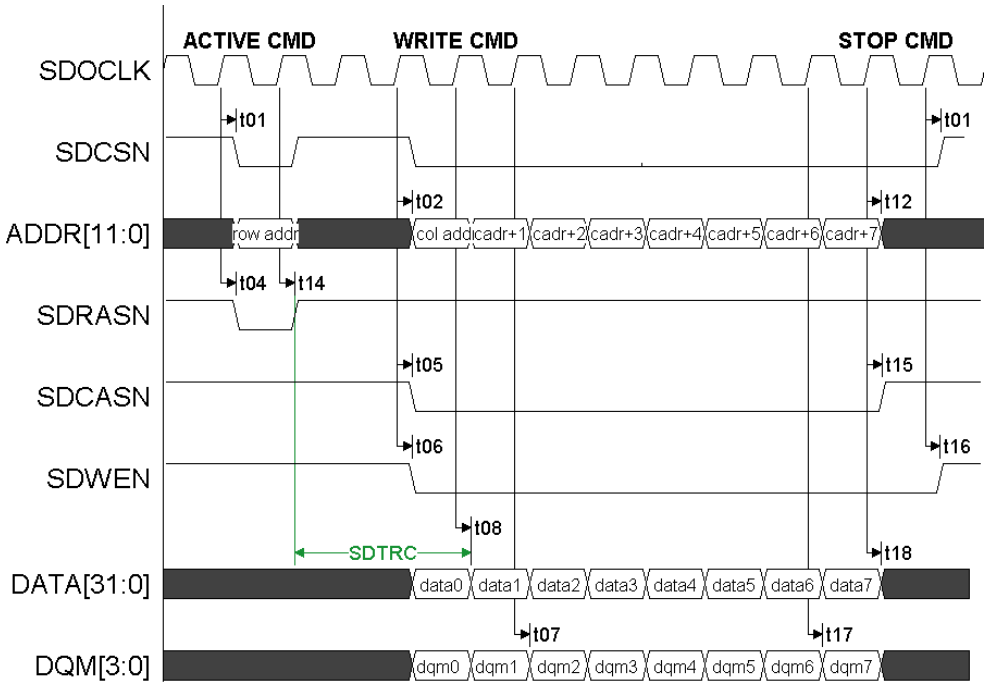


Figure 11. SDRAM Write Timing

Symbol	Parameter	Registers
SDTRC	Programmable SDRAM RAS to CAS latency	0x4038
SDCAS	Programmable SDRAM CAS latency	0x4038

Table 7. SDRAM Timing Parameters

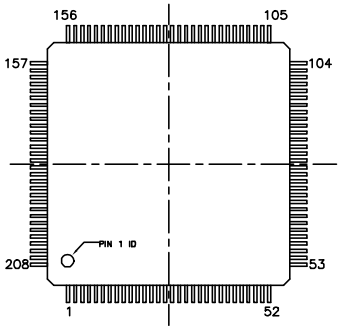
Symbol	Parameter	Min	Typ	Max	Units
SDRAM Signals Rise Time					
SDR	Clock rise time	4.2	4.0	4.8	ns
SDR	Address rise time	3.8	4.4	4.8	ns
SDR	Bank select rise time	3.6	4.2	4.4	ns
SDR	Data rise time				ns
SDR	Chip select rise time	3.0	3.0	3.7	ns
SDR	RAS rise time	3.4	3.6	3.8	ns
SDR	CAS rise time	3.0	3.5	3.4	ns
SDR	WE rise time	3.0	3.8	3.8	ns
SDR	DQM rise time	3.2	3.5	3.5	ns
SDRAM Signals Fall Time					
SDR	Clock fall time	5.0	6.0	6.4	ns
SDR	Address fall time	4.4	5.4	5.5	ns
SDR	Bank select fall time	5.2	5.5	6.0	ns
SDR	Data fall time				ns
SDR	Chip select fall time	3.6	3.6	4.2	ns
SDR	RAS fall time	3.8	3.8	4.4	ns
SDR	CAS fall time	4.0	3.8	4.8	ns
SDR	WE fall time	4.2	4.4	4.5	ns
SDR	DQM fall time	4.0	4.4	4.4	ns
SDRAM Timing Specifications					
t01	Clock-to-chip select output delay	0.7	0.7	0.9	ns
t11	Clock-to-chip select hold time	0.7	0.6	0.6	ns
t02	Clock-to-address high-to-low	1.2	1.6	1.7	ns
t12	Clock-to-address low-to-high	1.3	1.5	1.6	ns
t03	Clock-to-bank select high-to-low	1.9	1.8	1.9	ns
t13	Clock-to-bank select low-to-high	1.3	1.3	1.5	ns
t04	Clock-to-RAS output delay	1.1	1.1	1.5	ns
t14	Clock-to-RAS hold time	1.1	0.9	1.3	ns
t05	Clock-to-CAS output delay	1.3	1.1	1.5	ns
t15	Clock-to-CAS hold time	0.9	0.9	1.1	ns
t06	Clock-to-WE output delay	1.1	1.3	1.5	ns
t16	Clock-to-WE hold time	0.8	1.1	1.3	ns
t07	Clock-to-DQM output delay	0.7	1.1	1.1	ns
t17	Clock-to-DQM hold time	0.8	1.4	1.3	ns
t08	Clock-to-data output delay	0.4	0.6	0.8	ns
t18	Clock-to-data hold time	0.1	0.4	0.6	ns

Table 8. SDRAM Interface Timing

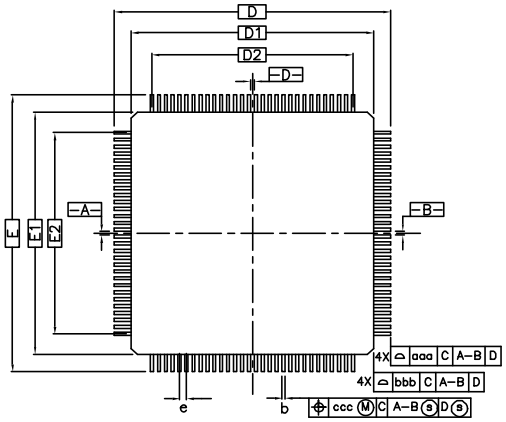
Symbol	Parameter	Registers
RBiTPACC	Programmable bank i access time	0x4010, 0x4014
RBiTPA	Programmable bank i page address access time	0x4010, 0x4014

Table 9. Static Memory Timing Parameters

Package Information



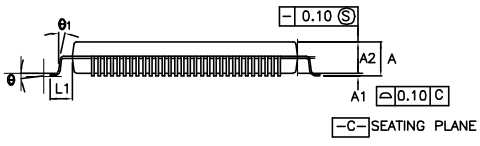
TOP VIEW



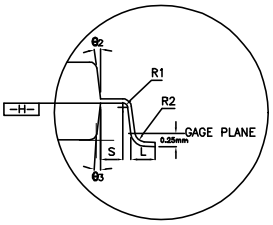
BOTTOM VIEW

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A1	0.25	—	—	0.010	—	—
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20 BASIC			1.228 BASIC		
D1	28.00 BASIC			1.102 BASIC		
E	31.20 BASIC			1.228 BASIC		
E1	28.00 BASIC			1.102 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	8° REF			8° REF		
θ3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	25.50			1.004		
E2	25.50			1.004		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.



SIDE VIEW



DETAILED VIEW

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.

208-Pin PQFP (PQ)

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