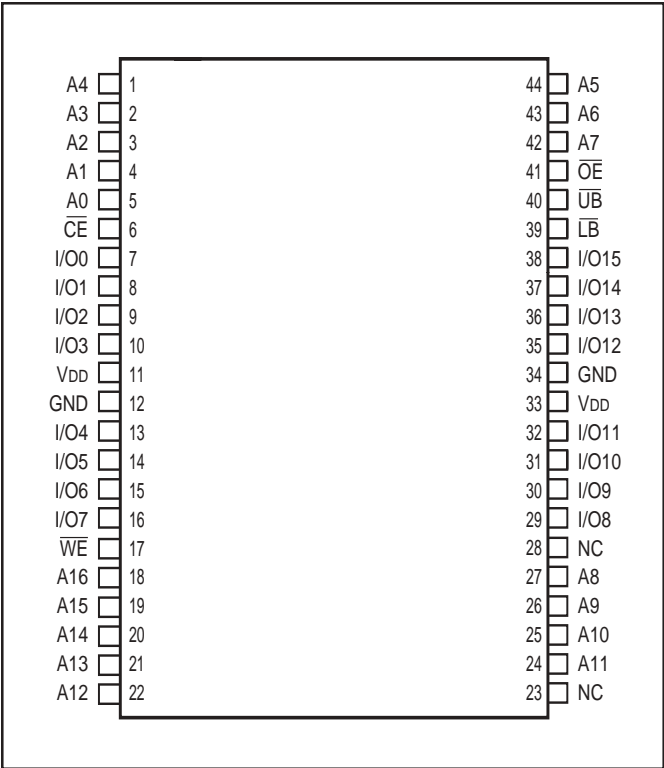## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	V_{DD} Current
						I/O PIN		
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

PIN CONFIGURATION
44-Pin TSOP (Type II) (T)

```
        ┌──────────────┐
  A4  ──┤ 1        44 ├── A5
  A3  ──┤ 2        43 ├── A6
  A2  ──┤ 3        42 ├── A7
  A1  ──┤ 4        41 ├── OE
  A0  ──┤ 5        40 ├── UB
  CE  ──┤ 6        39 ├── LB
 I/O0 ──┤ 7        38 ├── I/O15
 I/O1 ──┤ 8        37 ├── I/O14
 I/O2 ──┤ 9        36 ├── I/O13
 I/O3 ──┤ 10       35 ├── I/O12
 VDD  ──┤ 11       34 ├── GND
 GND  ──┤ 12       33 ├── VDD
 I/O4 ──┤ 13       32 ├── I/O11
 I/O5 ──┤ 14       31 ├── I/O10
 I/O6 ──┤ 15       30 ├── I/O9
 I/O7 ──┤ 16       29 ├── I/O8
  WE  ──┤ 17       28 ├── NC
  A16 ──┤ 18       27 ├── A8
  A15 ──┤ 19       26 ├── A9
  A14 ──┤ 20       25 ├── A10
  A13 ──┤ 21       24 ├── A11
  A12 ──┤ 22       23 ├── NC
        └──────────────┘
```

PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

PIN CONFIGURATION

48-Pin mini BGA (B)
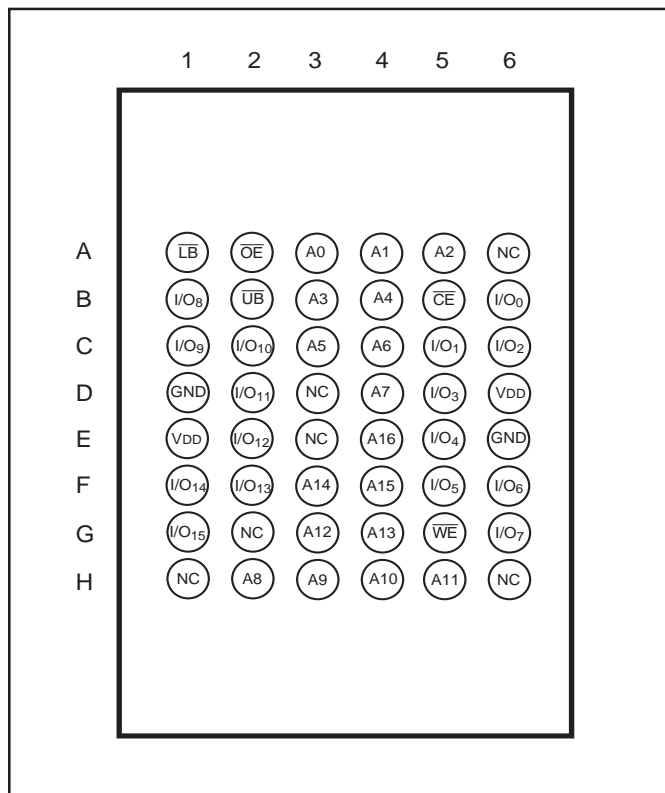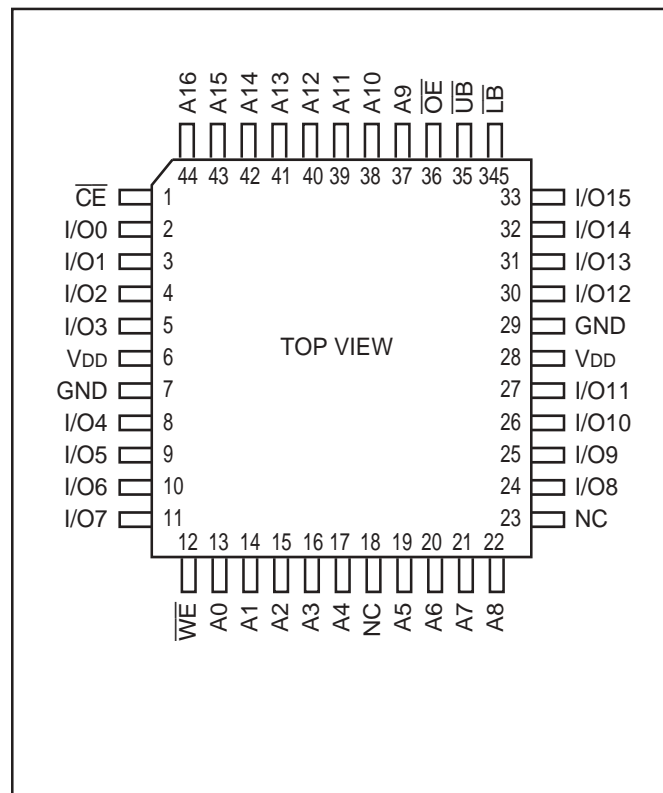
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O8	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	NC	A7	I/O3	VDD
E	VDD	I/O12	NC	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	$\overline{WE}$	I/O7
H	NC	A8	A9	A10	A11	NC

44-Pin LQFP (LQ)

Top pins (44-35): A16, A15, A14, A13, A12, A11, A10, A9, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$

Left pins:
- $\overline{CE}$ — 1
- I/O0 — 2
- I/O1 — 3
- I/O2 — 4
- I/O3 — 5
- VDD — 6
- GND — 7
- I/O4 — 8
- I/O5 — 9
- I/O6 — 10
- I/O7 — 11

TOP VIEW

Right pins:
- 33 — I/O15
- 32 — I/O14
- 31 — I/O13
- 30 — I/O12
- 29 — GND
- 28 — VDD
- 27 — I/O11
- 26 — I/O10
- 25 — I/O9
- 24 — I/O8
- 23 — NC

Bottom pins (12-22): $\overline{WE}$, A0, A1, A2, A3, A4, NC, A5, A6, A7, A8

PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage Relative to GND	−0.5 to 4.0V	V
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	−65 to + 150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V_{DD} (8 ns)	V_{DD} (10 ns)
Commercial	0°C to +70°C	3.3V + 10%, -5%	3.3V ± 10%
Industrial	−40°C to +85°C	3.3V + 10%, -5%	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = −4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		−0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	−1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	−1	1	µA

Note:
1. V_{IL} (min.) = −0.3V DC; V_{IL} (min.) = −2.0V AC (pulse width - 2.0 ns). Not 100% tested.
    V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width - 2.0 ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	Unit
I_{CC}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = Max.	Com. Ind. typ.[2]	— — —	65 70 50	— — —	60 65 50	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = max	Com. Ind.	— —	30 35	— —	25 30	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com. Ind. typ.[2]	— — —	3 4 700	— — —	3 4 700	mA mA μA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD}=3.3V, T_A=25°C. Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

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AC TEST CONDITIONS

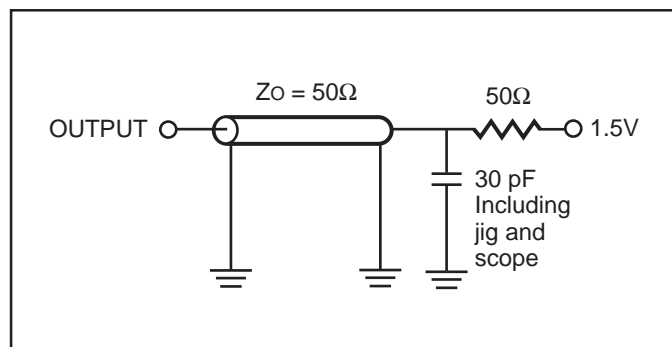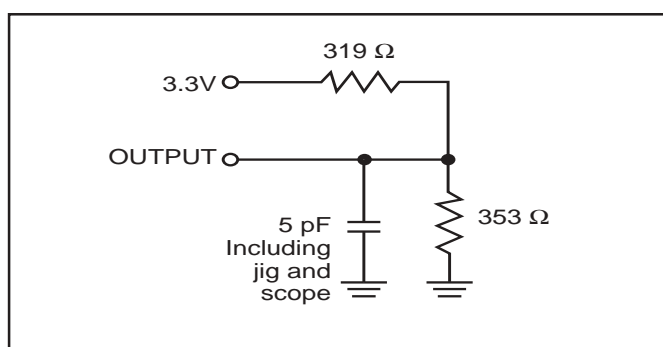| Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

Figure 1.

Figure 2.

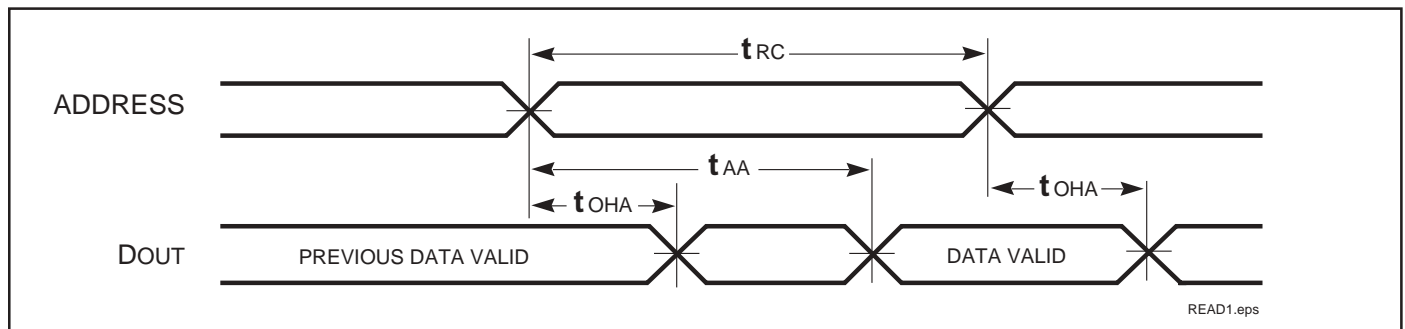## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol	Parameter	-8 ns Min.	-8 ns Max	-10 ns Min.	-10 ns Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	ns
t_{DOE}	$\overline{OE}$ Access Time	—	3.5	—	4	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	3.5	—	4	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	3.5	0	4	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3.5	—	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	3.5	—	4	ns
t_{HZB}[2]	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	3.5	0	4	ns
t_{LZB}[2]	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

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AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V$_{IL}$, $\overline{UB}$ or $\overline{LB}$ = V$_{IL}$)

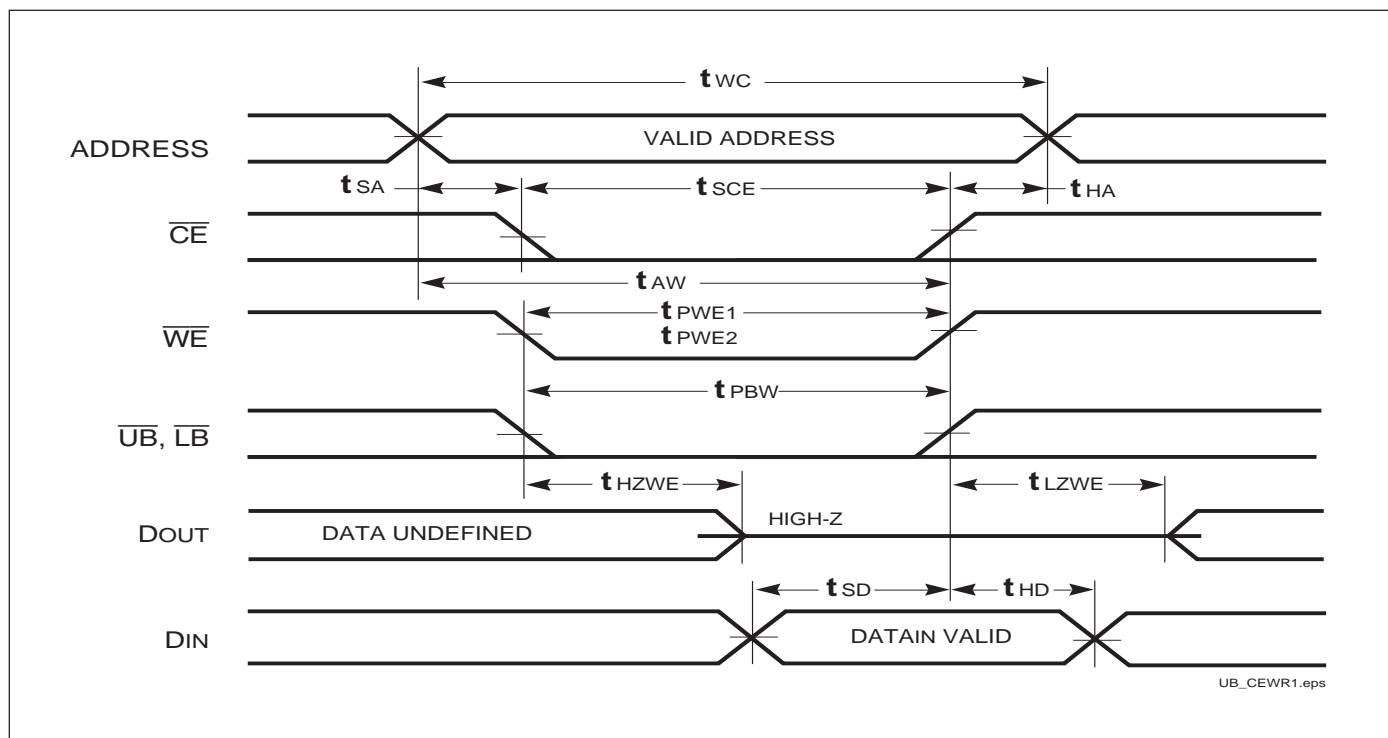READ1.eps

READ CYCLE NO. 2[1,3]

UB_CEDR2.eps
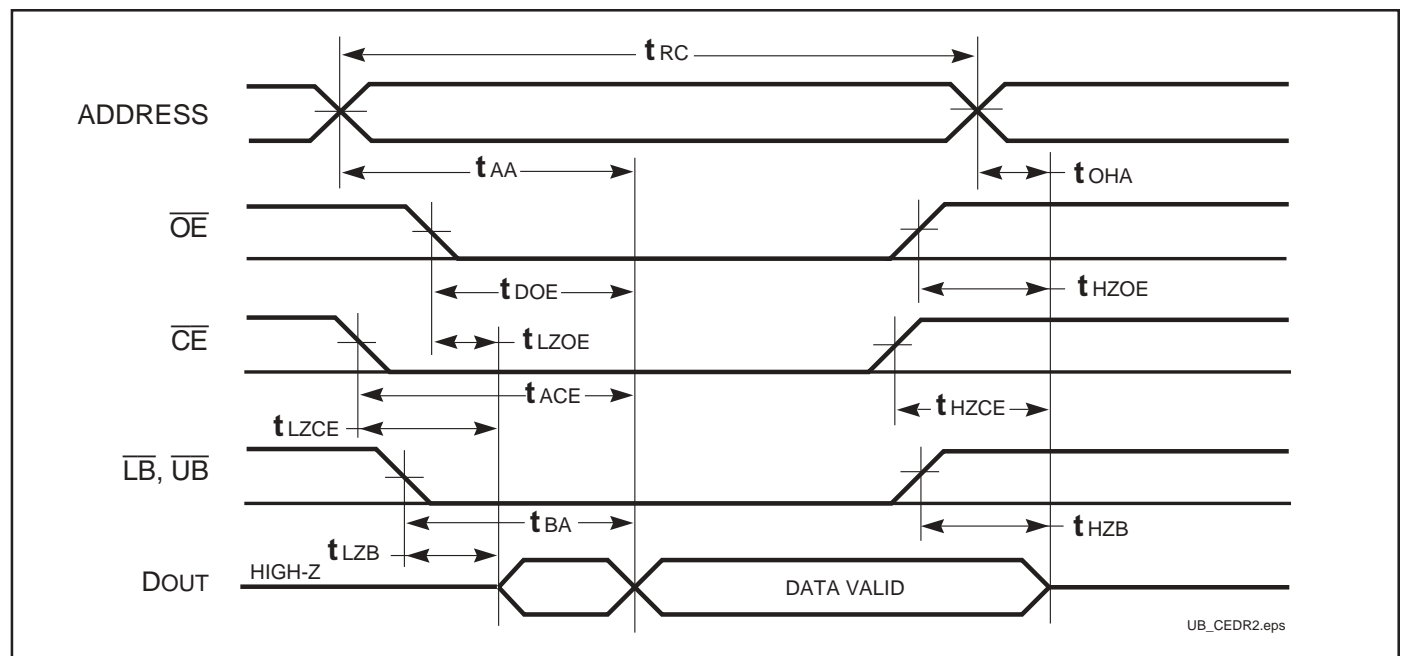
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V$_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

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10/27/05

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

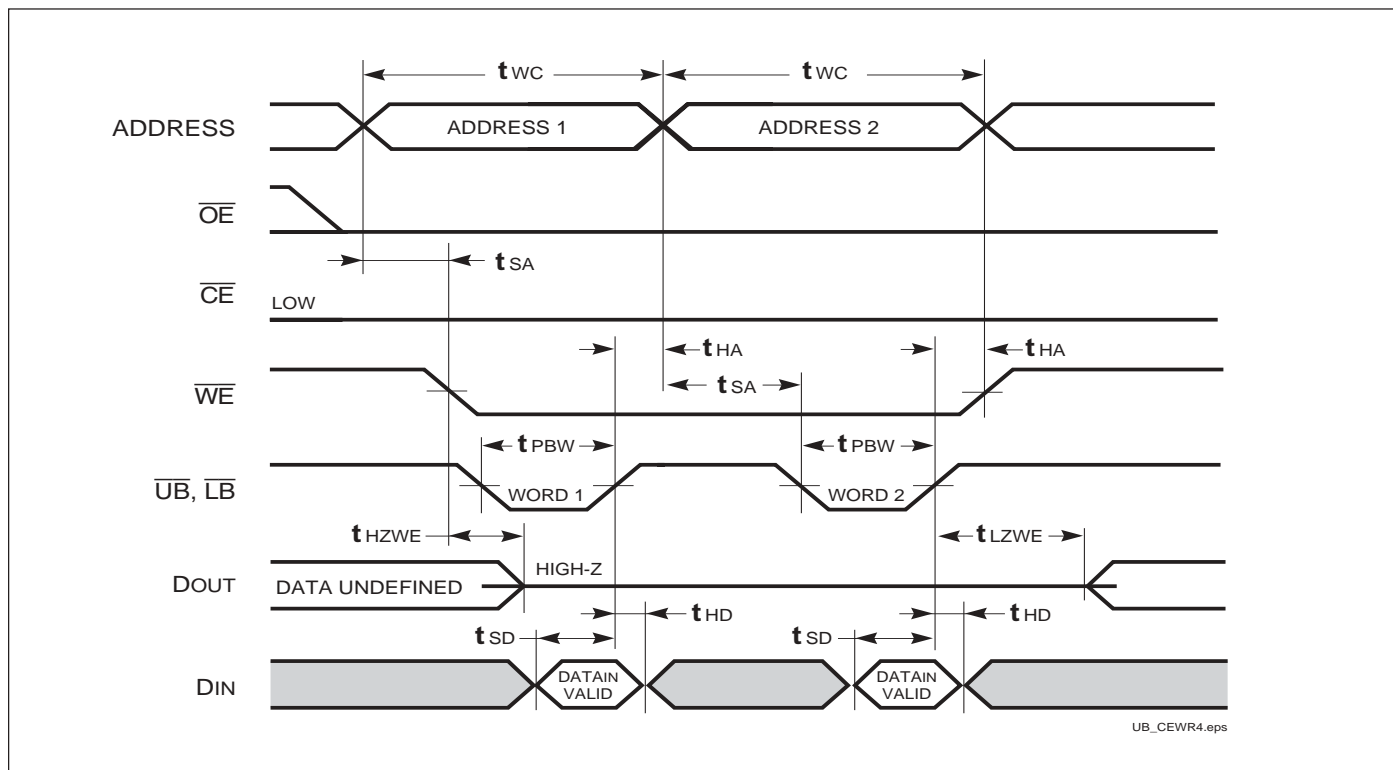| Symbol	Parameter	-8 ns Min.	Max	-10 ns Min.	Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	8	—	ns
t_{AW}	Address Setup Time to Write End	7	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PBW}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	6.5	—	8	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	6	—	7	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	6.5	—	8	—	ns
t_{SD}	Data Setup to Write End	4	—	5	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	3	—	4	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

ADDRESS — VALID ADDRESS

t_{WC}, t_{SA}, t_{SCE}, t_{HA}

$\overline{CE}$

t_{AW}

$\overline{WE}$ — t_{PWE1}, t_{PWE2}

t_{PBW}

$\overline{UB}$, $\overline{LB}$

t_{HZWE}, t_{LZWE}

DOUT — DATA UNDEFINED — HIGH-Z

t_{SD}, t_{HD}

DIN — DATAIN VALID

UB_CEWR1.eps

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WRITE CYCLE NO. 2[1] ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ = HIGH during Write Cycle)

ADDRESS — t_{WC} — VALID ADDRESS — t_{HA}

$\overline{\text{OE}}$

$\overline{\text{CE}}$ — LOW

$\overline{\text{WE}}$ — t_{AW} — t_{PWE1}

t_{SA} — t_{PBW}

$\overline{\text{UB}}, \overline{\text{LB}}$

t_{HZWE} — t_{LZWE}

D_{OUT} — DATA UNDEFINED — HIGH-Z

t_{SD} — t_{HD}

D_{IN} — DATA IN VALID

UB_CEWR2.eps
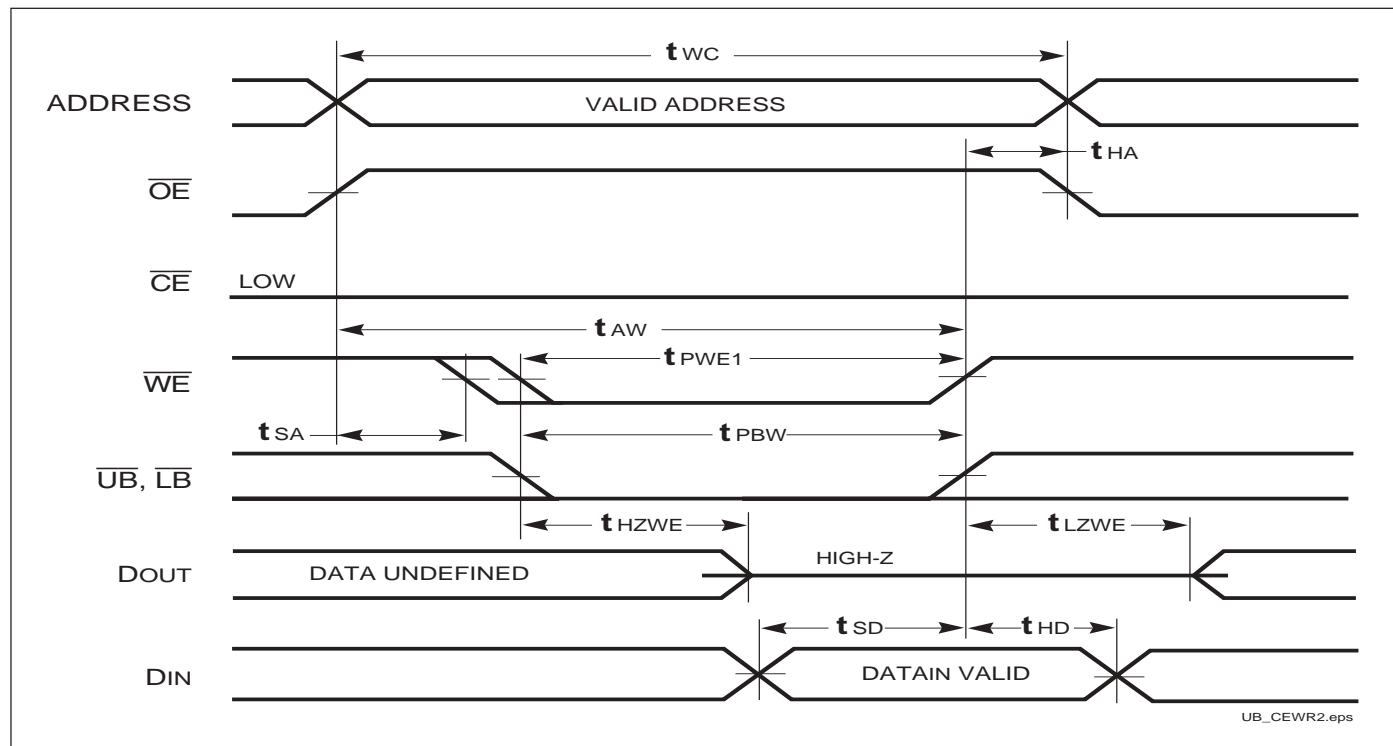
WRITE CYCLE NO. 3 ($\overline{\text{WE}}$ Controlled: $\overline{\text{OE}}$ is LOW During Write Cycle)

ADDRESS — t_{WC} — VALID ADDRESS — t_{HA}

$\overline{\text{OE}}$ — LOW

$\overline{\text{CE}}$ — LOW

$\overline{\text{WE}}$ — t_{AW} — t_{PWE2}

t_{SA} — t_{PBW}

$\overline{\text{UB}}, \overline{\text{LB}}$

t_{HZWE} — t_{LZWE}

D_{OUT} — DATA UNDEFINED — HIGH-Z

t_{SD} — t_{HD}

D_{IN} — DATA IN VALID

UB_CEWR3.eps

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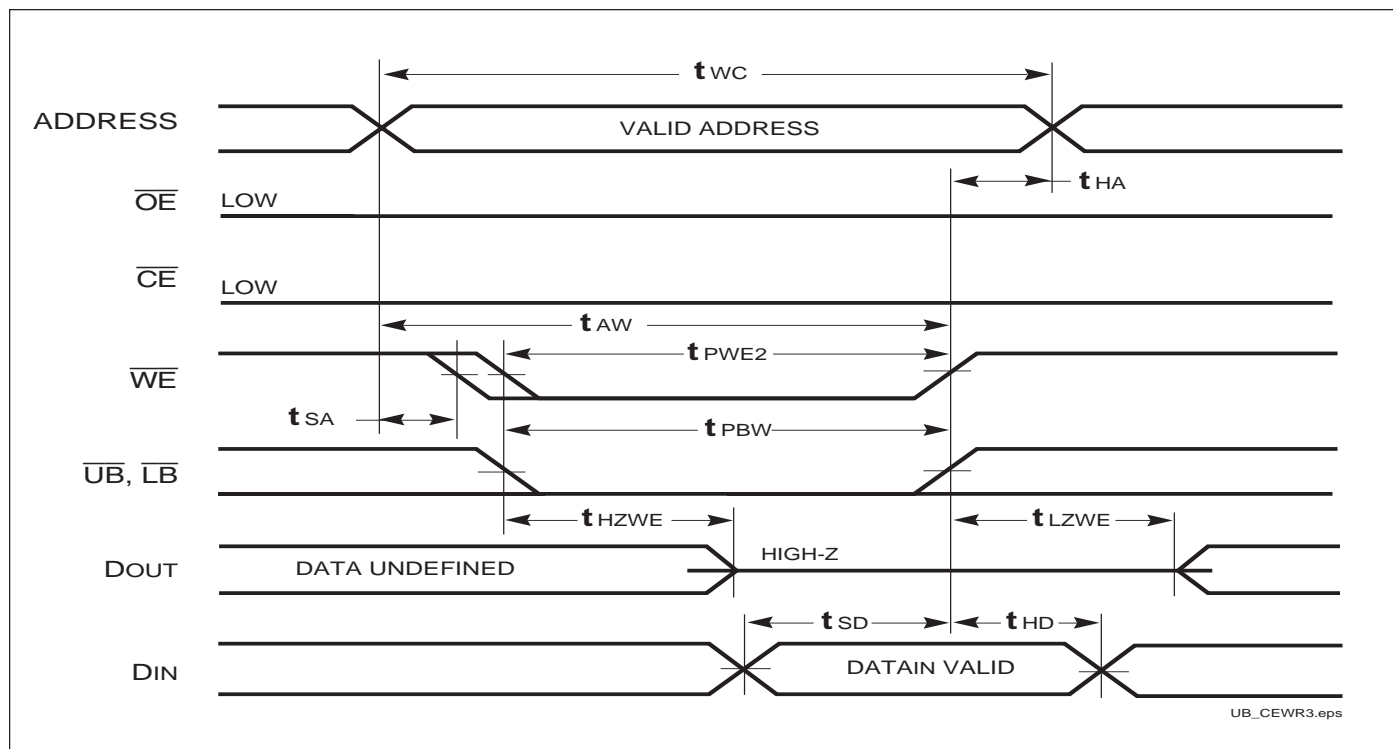
WRITE CYCLE NO. 4 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write) [1,3]

UB_CEWR4.eps

Notes:

1. The internal Write time is defined by the overlap of $\overline{\text{CE}}$ = LOW, $\overline{\text{UB}}$ and/or $\overline{\text{LB}}$ = LOW, and $\overline{\text{WE}}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with OE HIGH for a minimum of 4 ns before $\overline{\text{WE}}$ = LOW to place the I/O in a HIGH-Z state.
3. WE may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

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DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Options	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.7	3	mA
			Ind.	—	—	4	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = 3.3V$, $T_A = 25°C$. Not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

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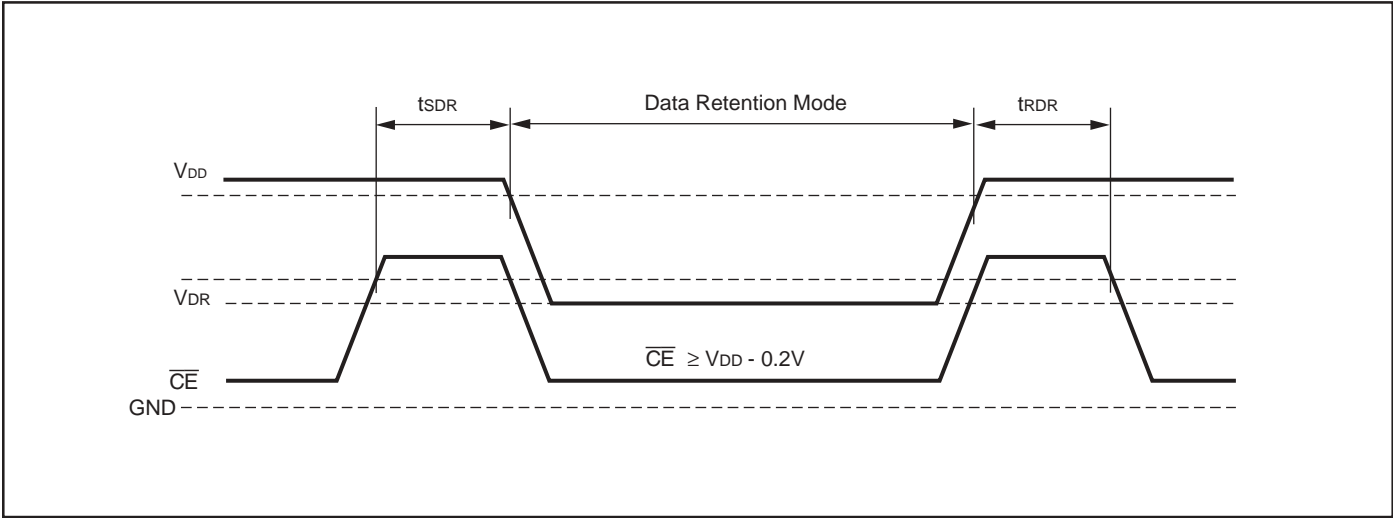
ORDERING INFORMATION:

Commercial Range: 0°C to +70°C

| Speed (ns)	Order Part No.	Package
8	IS61LV12816L-8T	Plastic TSOP (Type II)
	IS61LV12816L-8TL	Plastic TSOP (Type II), Lead-free
10	IS61LV12816L-10T	Plastic TSOP (Type II)
	IS61LV12816L-10TL	Plastic TSOP (Type II), Lead-free

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS61LV12816L-8BI	mini BGA (6mm x 8mm)
	IS61LV12816L-8TI	Plastic TSOP (Type II)
10	IS61LV12816L-10BI	mini BGA (6mm x 8mm)
	IS61LV12816L-10BLI	mini BGA (6mm x 8mm), Lead-free
	IS61LV12816L-10LQI	LQFP
	IS61LV12816L-10LQLI	LQFP, Lead-free
	IS61LV12816L-10TI	Plastic TSOP (Type II)
	IS61LV12816L-10TLI	Plastic TSOP (Type II), Lead-free

LQFP (Low Profile Quad Flat Pack)
Package Code: LQ (44-pin)

SEATING
PLANE
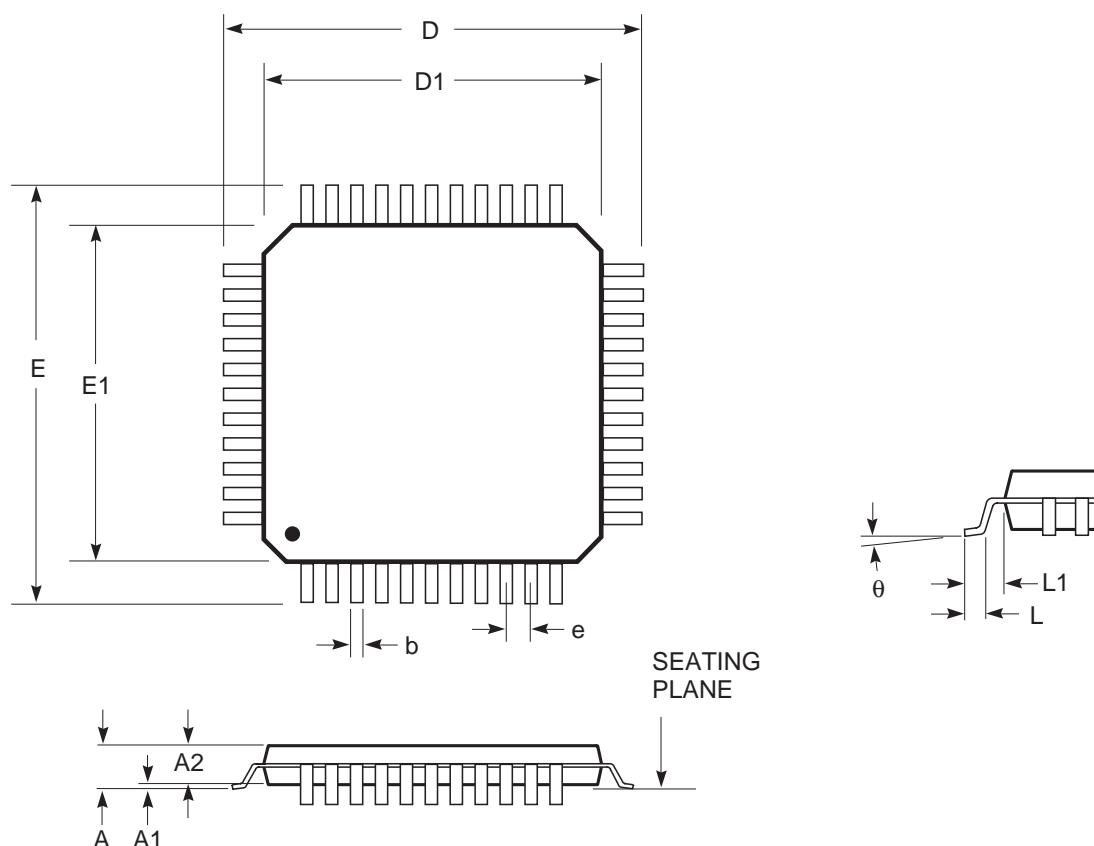
Low Profile Quad Flat Pack (LQ)				
Ref. Std.	MS-026			
No. Leads	44			
Symbol	**Millimeters**		**Inches**	
	Min	Max	Min	Max
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
C	0.09	0.20	0.004	0.008
D	12.00 BSC		0.472 BSC	
D1	10.00 BSC		0.394 BSC	
E	12.00 BSC		0.472 BSC	
E1	10.00 BSC		0.394 BSC	
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.	
θ	0º	7º	0º	7º

Notes:
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 include mold mismatch.
3. Controlling dimension: millimeters.
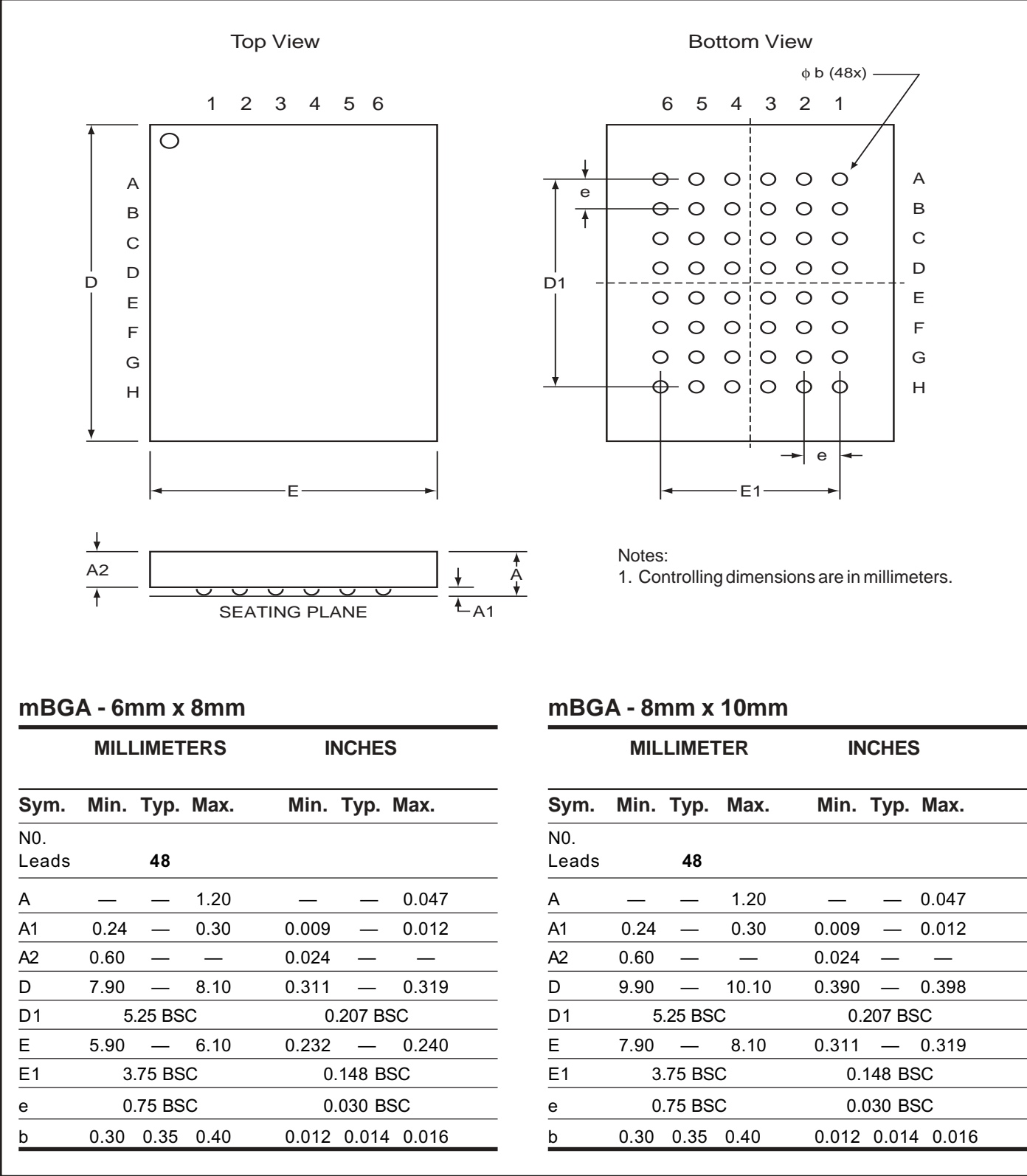
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05/30/03

PACKAGING INFORMATION

ISSI®

Mini Ball Grid Array
Package Code: B (48-pin)

Top View

Bottom View

φ b (48x)

Notes:
1. Controlling dimensions are in millimeters.

SEATING PLANE

mBGA - 6mm x 8mm

Sym.	MILLIMETERS			INCHES		
	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		48				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	7.90	—	8.10	0.311	—	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	—	6.10	0.232	—	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016

mBGA - 8mm x 10mm

Sym.	MILLIMETER			INCHES		
	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		48				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	9.90	—	10.10	0.390	—	0.398
D1	5.25 BSC			0.207 BSC		
E	7.90	—	8.10	0.311	—	0.319
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016

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Plastic TSOP
Package Code: T (Type II)
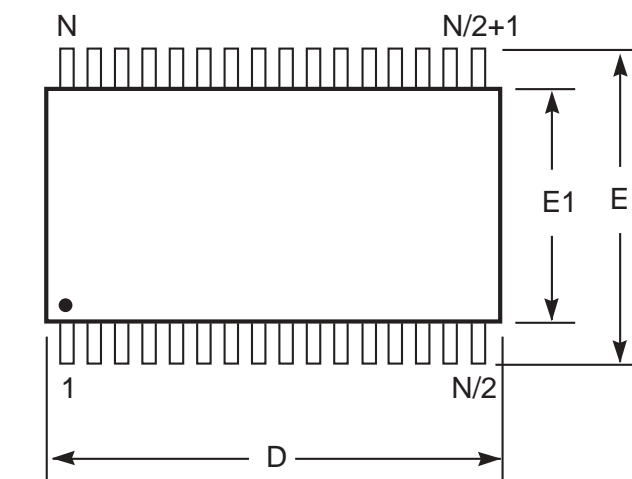
Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.
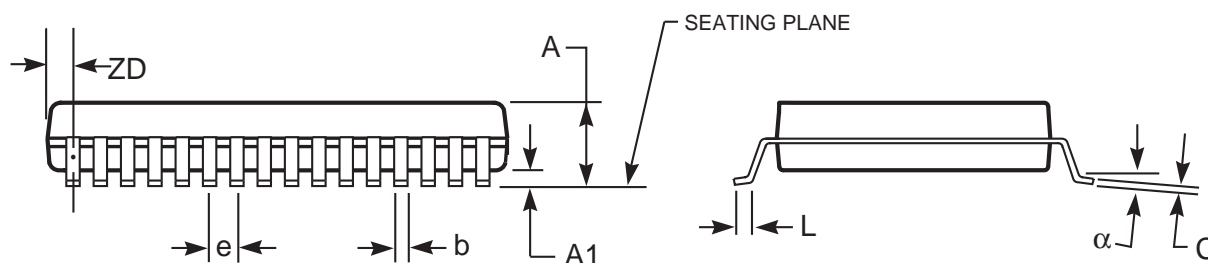
	Plastic TSOP (T - Type II)											
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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