

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	650	—	—	V	$V_{GE} = 0\text{V}$, $I_C = 100\mu\text{A}$ ③
$\Delta V_{(BR)CES}/\Delta$	Temperature Coeff. of Breakdown Voltage	—	505	—	mV/°C	$V_{GE} = 0\text{V}$, $I_C = 1\text{mA}$ (25°C-175°C)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.7	2.1	V	$I_C = 48\text{A}$, $V_{GE} = 15\text{V}$, $T_J = 25^\circ\text{C}$
		—	2.1	—		$I_C = 48\text{A}$, $V_{GE} = 15\text{V}$, $T_J = 175^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	5.5	—	7.7	V	$V_{CE} = V_{GE}$, $I_C = 1.4\text{mA}$
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage Temperature Coeff.	—	-23	—	mV/°C	$V_{CE} = V_{GE}$, $I_C = 1.4\text{mA}$ (25°C-175°C)
gfe	Forward Transconductance	—	31	—	S	$V_{CE} = 50\text{V}$, $I_C = 48\text{A}$, $PW = 20\mu\text{s}$
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	25	μA	$V_{GE} = 0\text{V}$, $V_{CE} = 650\text{V}$
		—	700	—		$V_{GE} = 0\text{V}$, $V_{CE} = 650\text{V}$, $T_J = 175^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	$V_{GE} = \pm 20\text{V}$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max④	Units	Conditions	
Q _g	Total Gate Charge (turn-on)	—	100	150	nC	I _C = 48A	
Q _{ge}	Gate-to-Emitter Charge (turn-on)	—	30	50		V _{GE} = 15V	
Q _{gc}	Gate-to-Collector Charge (turn-on)	—	40	60		V _{CC} = 600V	
E _{on}	Turn-On Switching Loss	—	1.7	2.6	mJ	I _C = 48A, V _{CC} = 400V, V _{GE} =15V R _G = 10Ω, L = 210μH, T _J = 25°C Energy losses include tail & diode reverse recovery ⑤⑥	
E _{off}	Turn-Off Switching Loss		1.0	1.9			
E _{total}	Total Switching Loss		2.7	4.5			
t _{d(on)}	Turn-On delay time	—	70	90	ns		
t _r	Rise time	—	60	80			
t _{d(off)}	Turn-Off delay time	—	140	160			
t _f	Fall time	—	30	50			
E _{on}	Turn-On Switching Loss	—	2.9	—	mJ		I _C = 48A, V _{CC} = 400V, V _{GE} =15V R _G = 10Ω, L = 210μH, T _J = 175°C Energy losses include tail & diode reverse recovery ⑤⑥
E _{off}	Turn-Off Switching Loss	—	1.4	—			
E _{total}	Total Switching Loss		4.3				
t _{d(on)}	Turn-On delay time	—	55	—	ns		
t _r	Rise time	—	60	—			
t _{d(off)}	Turn-Off delay time	—	145	—			
t _f	Fall time	—	65	—			
C _{ies}	Input Capacitance	—	3000	—	pF	V _{GE} = 0V	
C _{oes}	Output Capacitance	—	150	—		V _{CC} = 30V	
C _{res}	Reverse Transfer Capacitance	—	80	—		f = 1.0Mhz	
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T _J = 175°C, I _C = 192A V _{CC} = 520V, V _p ≤ 650V R _g = 10Ω, V _{GE} = +20V to 0V	
SCSOA	Short Circuit Safe Operating Area	5.5	—	—	μs	T _J = 150°C, V _{CC} = 400V, V _p ≤ 650V R _g = 10Ω, V _{GE} = +15V to 0V	

Notes:

- ① $V_{CC} = 80\%$ (V_{CES}), $V_{GE} = 20\text{V}$, $L = 50\mu\text{H}$, $R_G = 10\Omega$.
- ② R_θ is measured at T_J of approximately 90°C .
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ Maximum limits are based on statistical sample size characterization.
- ⑤ Pulse width limited by max. junction temperature.
- ⑥ Values influenced by parasitic L and C in measurement.

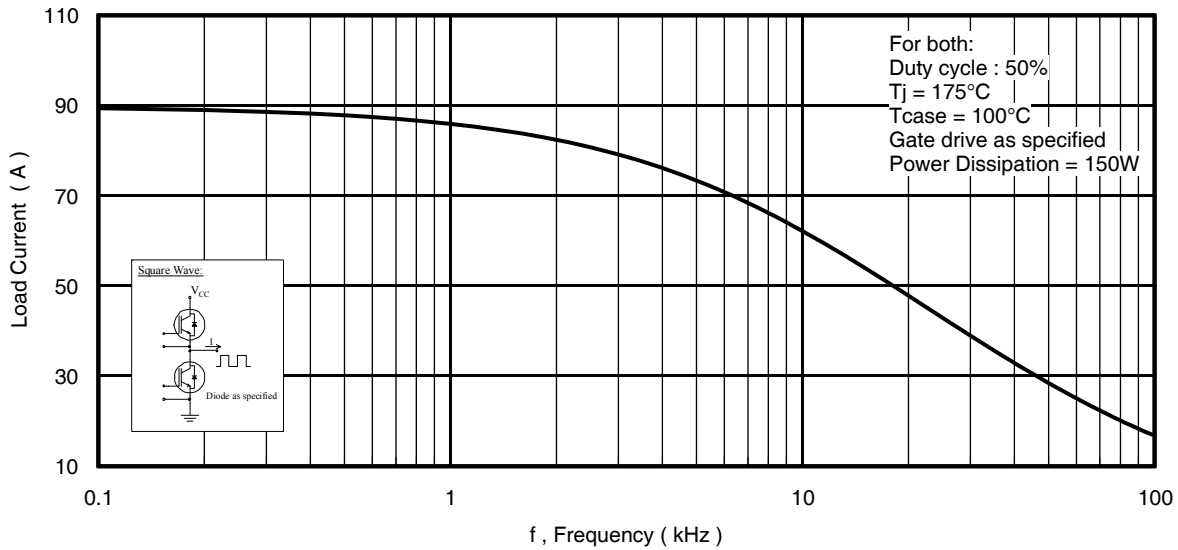


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

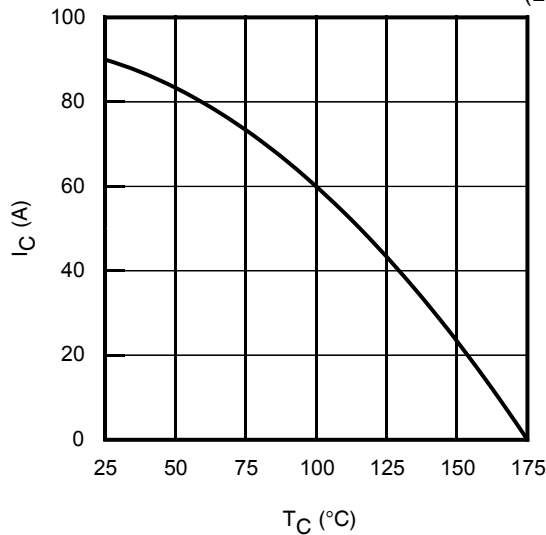


Fig. 2 - Maximum DC Collector Current vs. Case Temperature

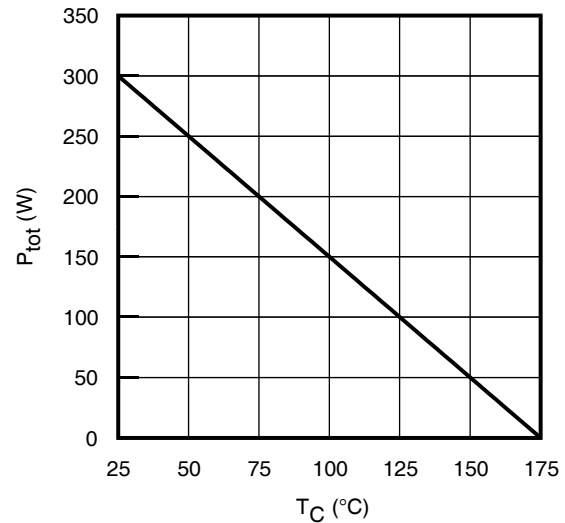


Fig. 3 - Power Dissipation vs. Case Temperature

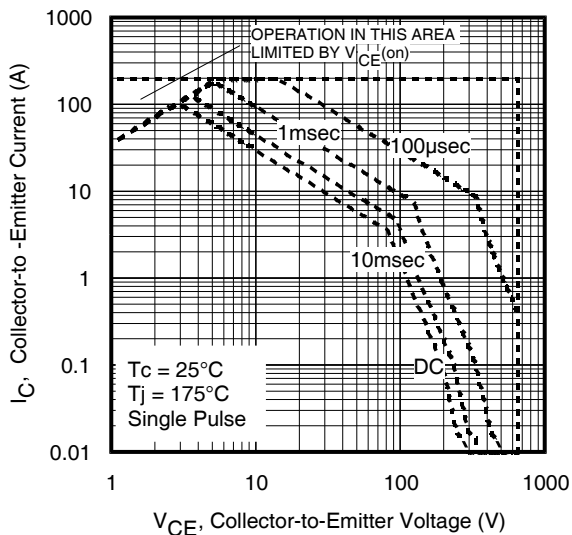


Fig. 4 - Forward SOA
 $T_c = 25^{\circ}\text{C}$, $T_j \leq 175^{\circ}\text{C}$, $V_{\text{GE}} = 15\text{V}$

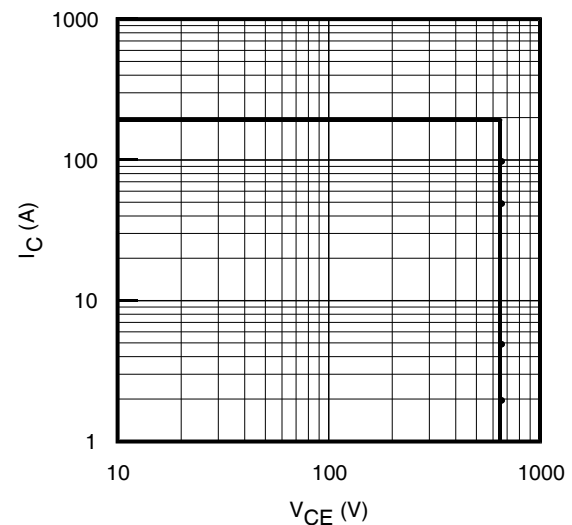


Fig. 5- Reverse Bias SOA
 $T_j = 175^{\circ}\text{C}$; $V_{\text{GE}} = 20\text{V}$

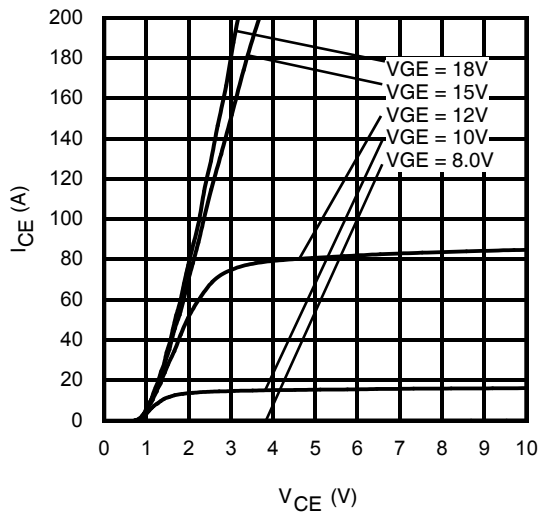


Fig. 6 - Typ. IGBT Output Characteristics
 $T_j = -40^\circ\text{C}$; $t_p = 20\mu\text{s}$

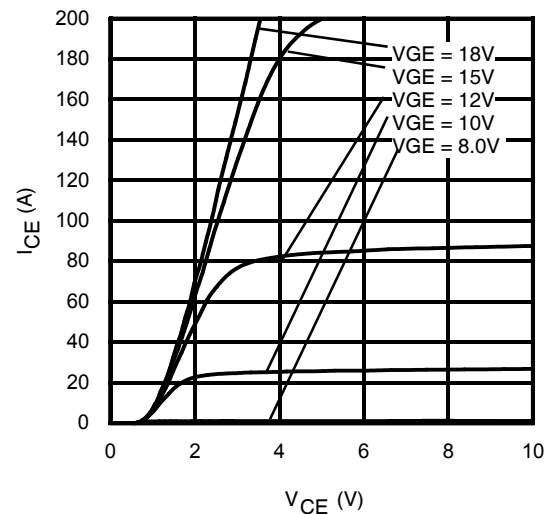


Fig. 7 - Typ. IGBT Output Characteristics
 $T_j = 25^\circ\text{C}$; $t_p = 20\mu\text{s}$

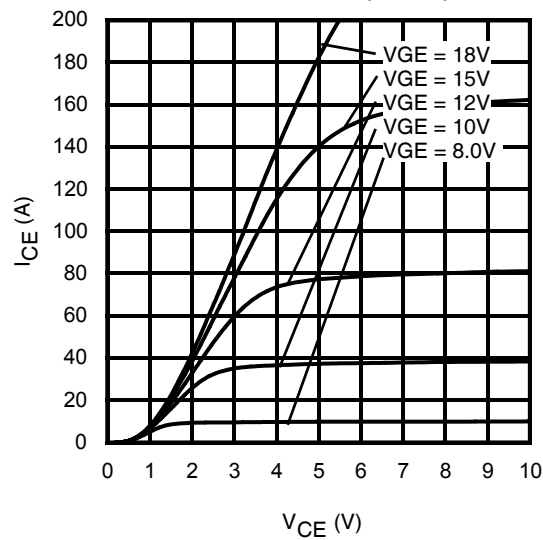


Fig. 8 - Typ. IGBT Output Characteristics
 $T_j = 175^\circ\text{C}$; $t_p = 20\mu\text{s}$

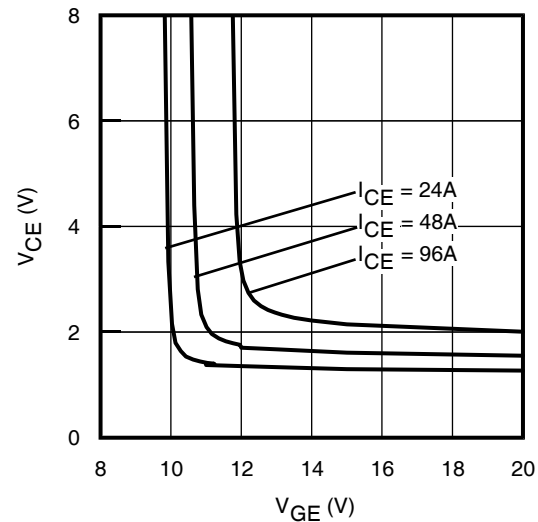


Fig. 9 - Typical V_{CE} vs. V_{GE}
 $T_j = -40^\circ\text{C}$

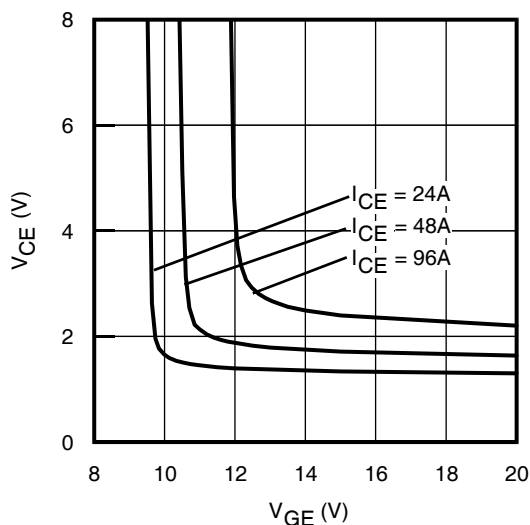


Fig. 10 - Typical V_{CE} vs. V_{GE}
 $T_j = 25^\circ\text{C}$

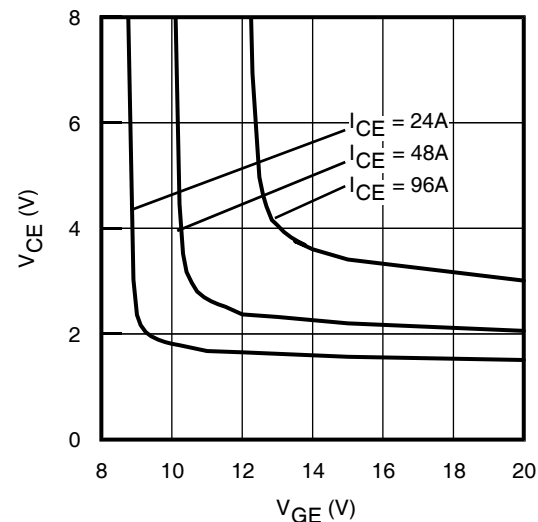


Fig. 11 - Typical V_{CE} vs. V_{GE}
 $T_j = 175^\circ\text{C}$

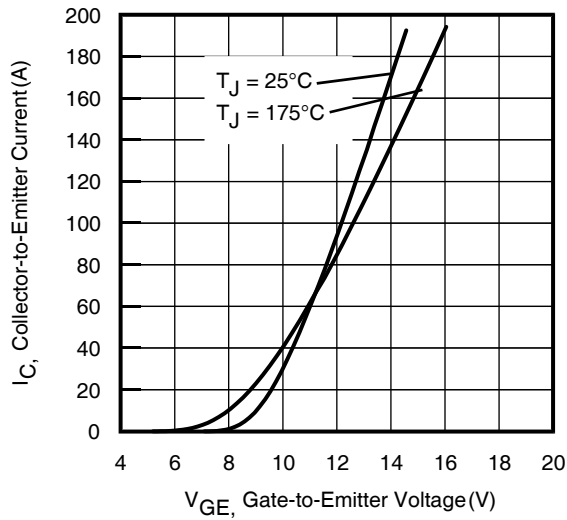


Fig. 12 - Typ. Transfer Characteristics
 $V_{CE} = 50V$; $t_p = 20\mu s$

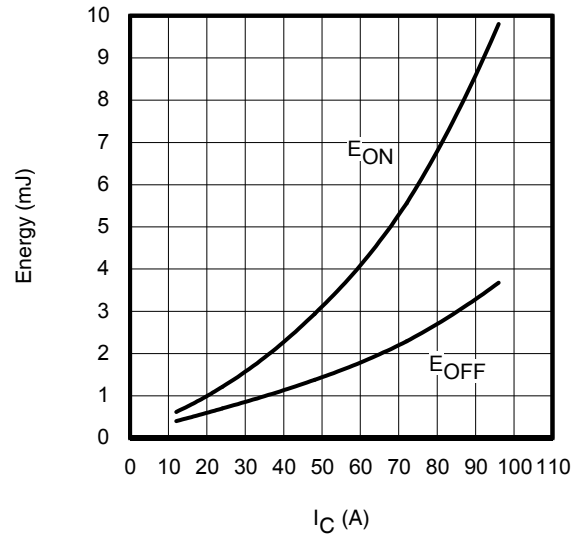


Fig. 13 - Typ. Energy Loss vs. I_C
 $T_J = 175^\circ C$; $L = 0.210mH$; $V_{CE} = 400V$, $R_G = 10\Omega$; $V_{GE} = 15V$

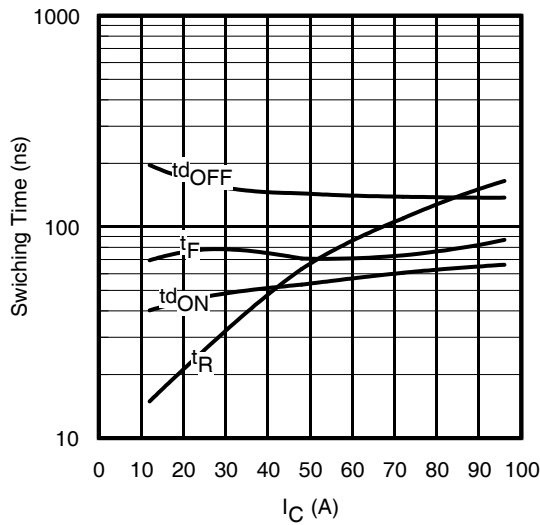


Fig. 14 - Typ. Switching Time vs. I_C
 $T_J = 175^\circ C$; $L = 0.210mH$; $V_{CE} = 400V$, $R_G = 10\Omega$; $V_{GE} = 15V$

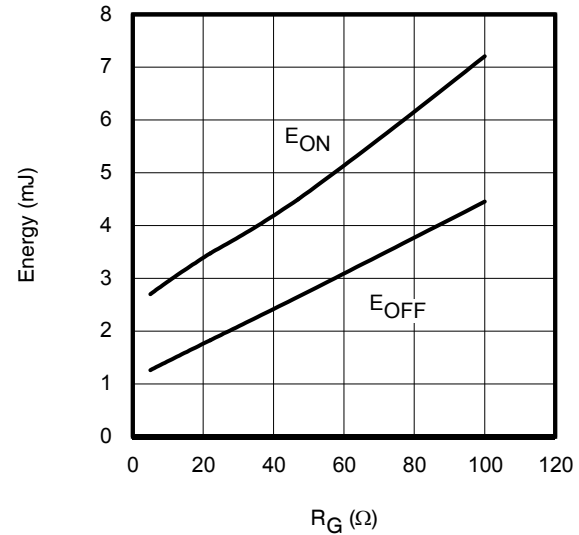


Fig. 15 - Typ. Energy Loss vs. R_G
 $T_J = 175^\circ C$; $L = 0.210mH$; $V_{CE} = 400V$, $I_{CE} = 48A$; $V_{GE} = 15V$

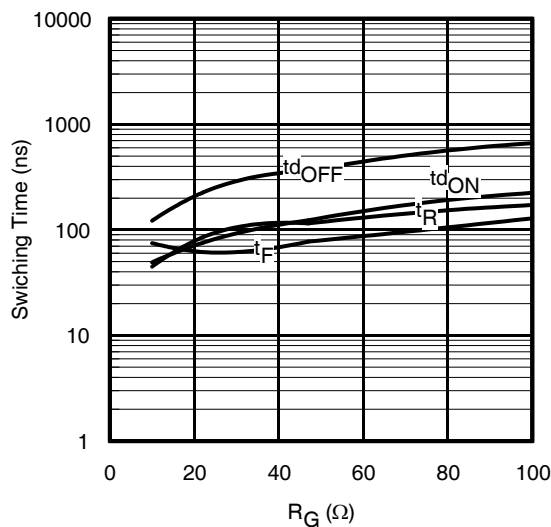


Fig. 16 - Typ. Switching Time vs. R_G
 $T_J = 175^\circ C$; $L = 0.210mH$; $V_{CE} = 400V$, $I_{CE} = 48A$; $V_{GE} = 15V$

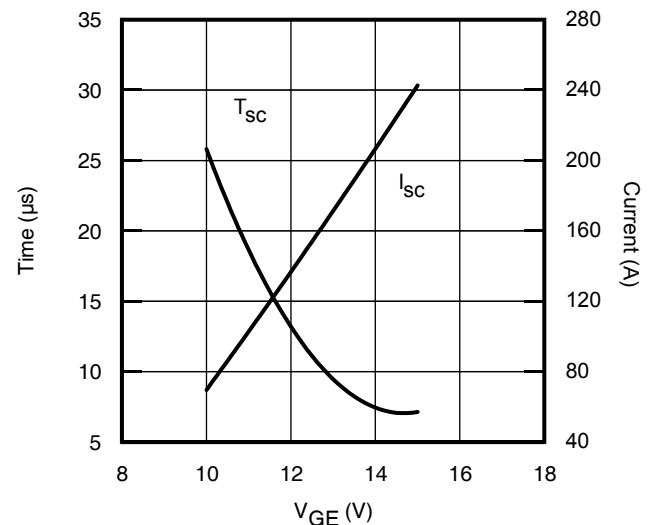


Fig. 17 - V_{CE} vs. Short Circuit Time
 $V_{CC} = 400V$; $T_C = 150^\circ C$

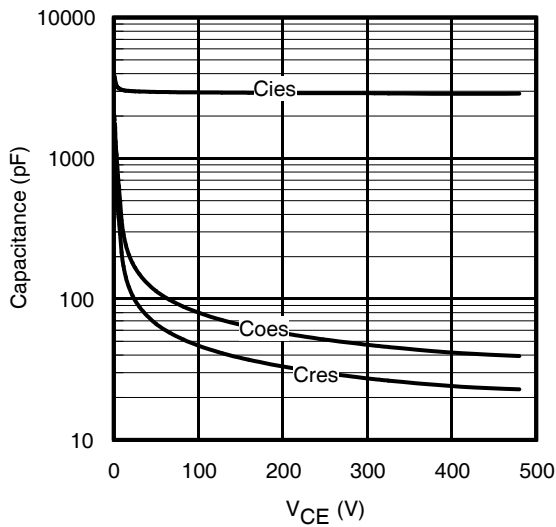


Fig. 18 - Typ. Capacitance vs. V_{CE}
 $V_{GE} = 0V$; $f = 1MHz$

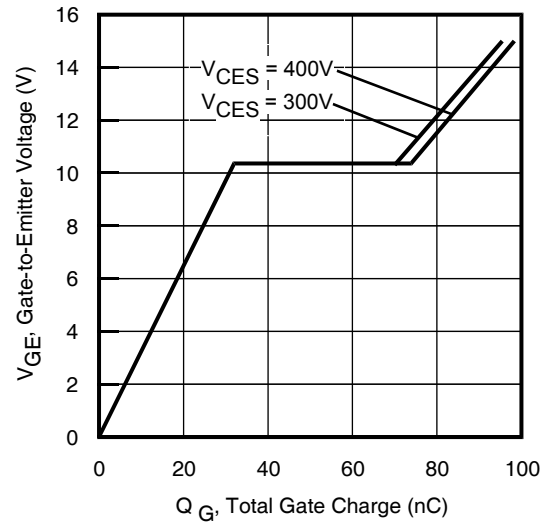


Fig. 19 - Typical Gate Charge vs. V_{GE}
 $I_{CE} = 48A$

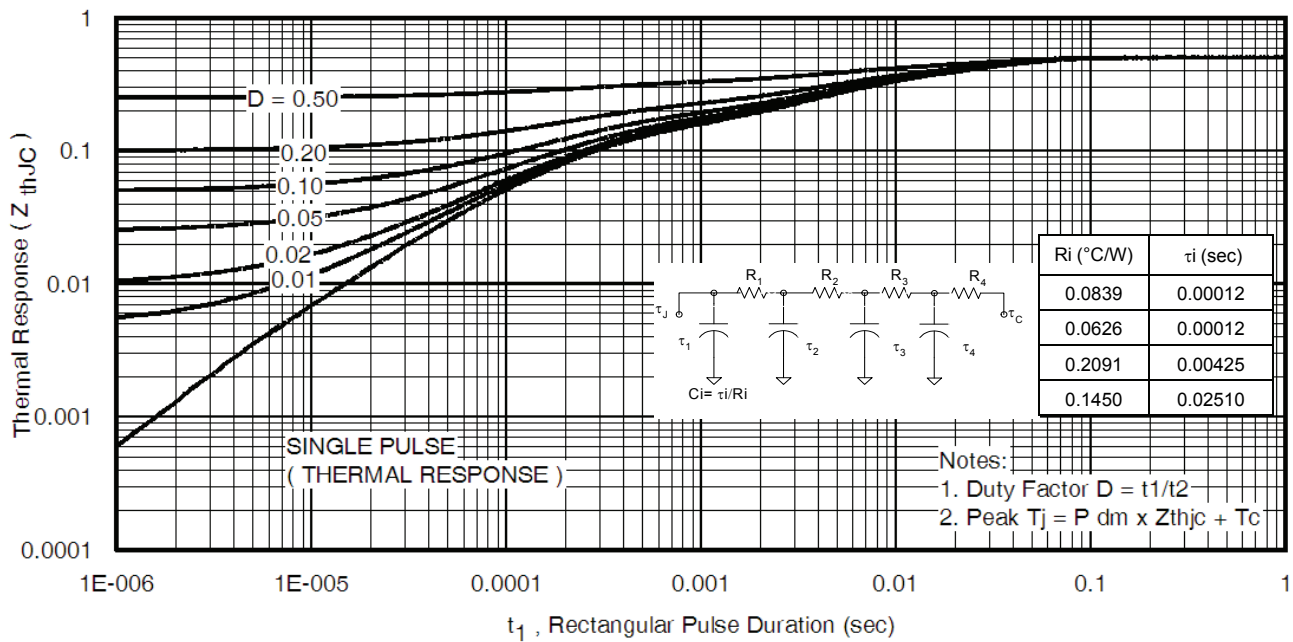


Fig. 20 Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

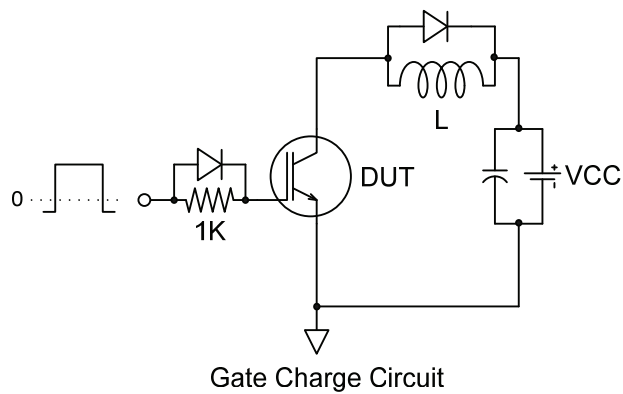


Fig.C.T.1 - Gate Charge Circuit (turn-off)

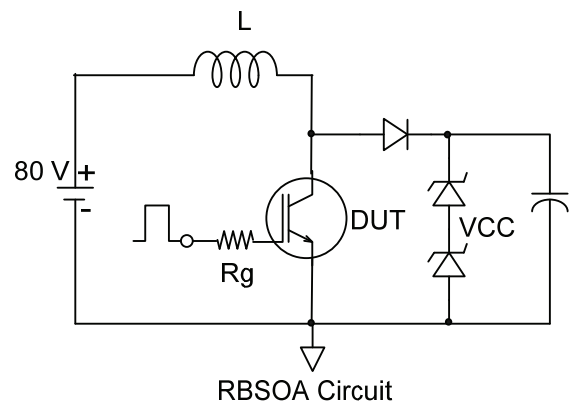


Fig.C.T.2 - RBSOA Circuit

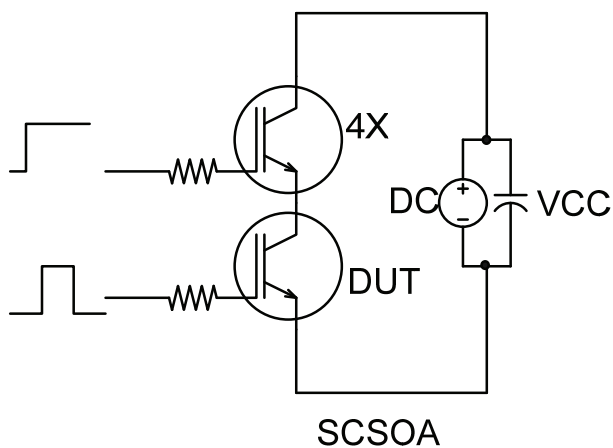


Fig.C.T.3 - Switching Loss Circuit

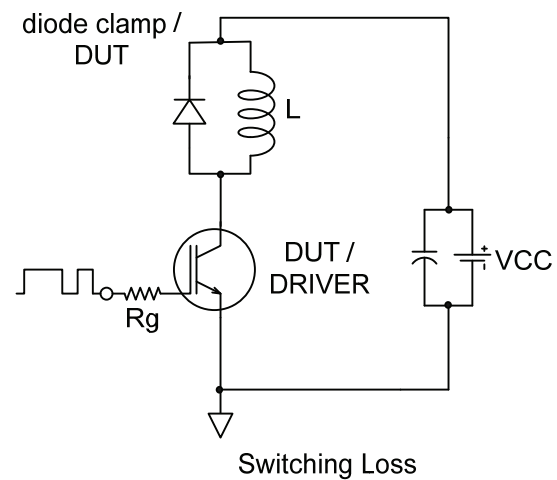


Fig.C.T.4 - Switching Loss Circuit

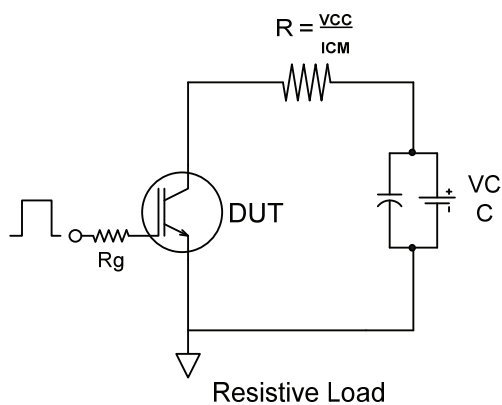


Fig.C.T.5 - Resistive Load Circuit

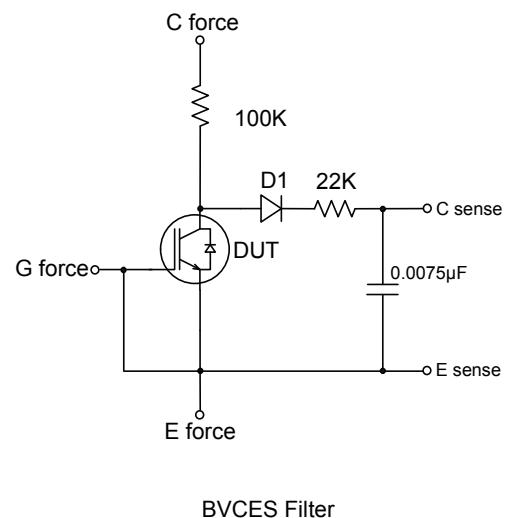


Fig.C.T.6 - BVCE Filter Circuit

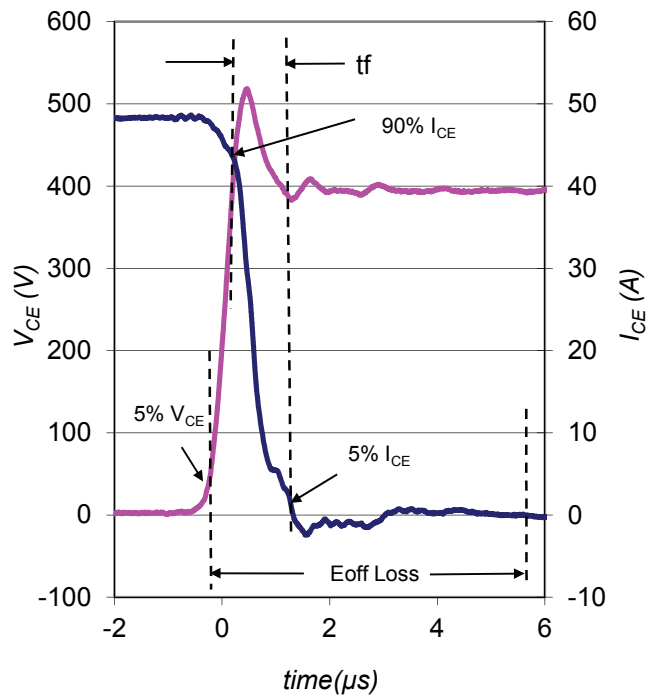


Fig. WF1 - Typ. Turn-off Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.4

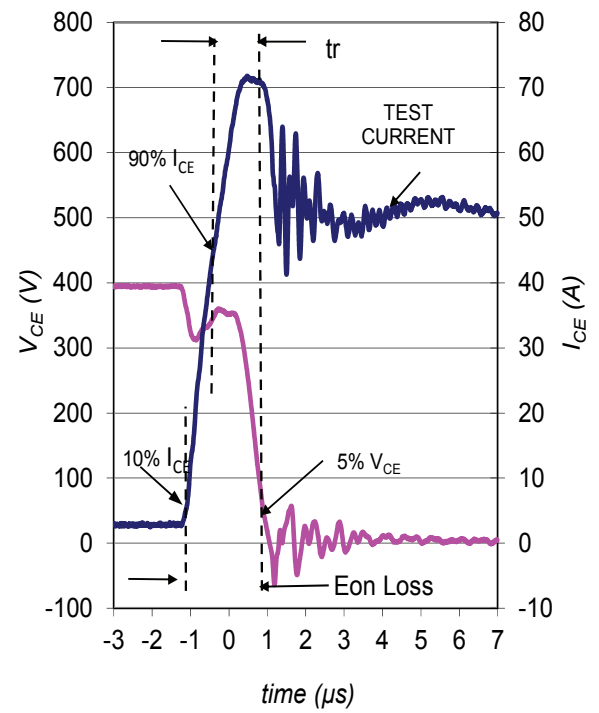


Fig. WF2 - Typ. Turn-on Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.4

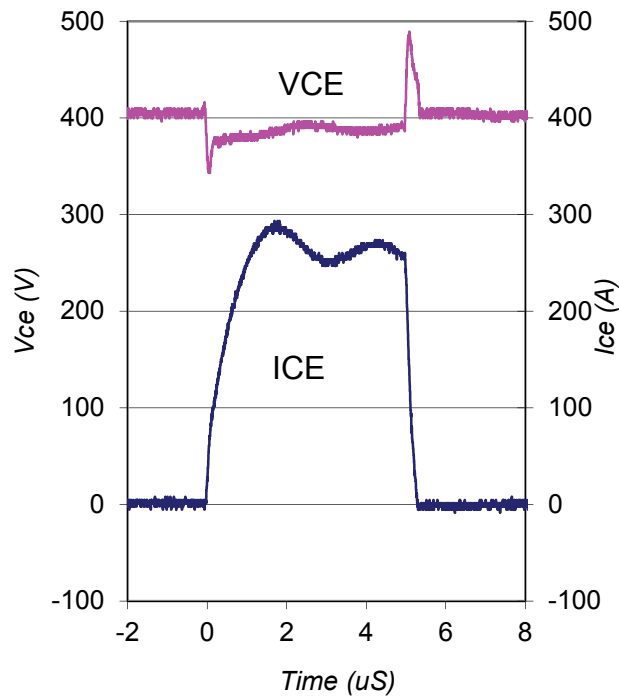
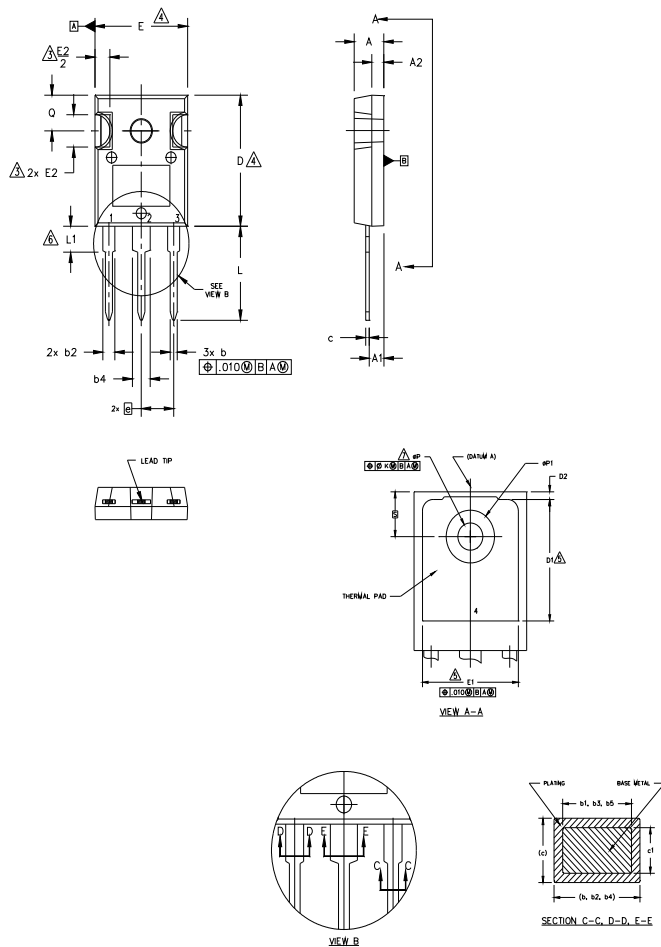


Fig. WF3 - Typ. S.C. Waveform
@ $T_J = 150^\circ\text{C}$ using Fig. CT.3

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

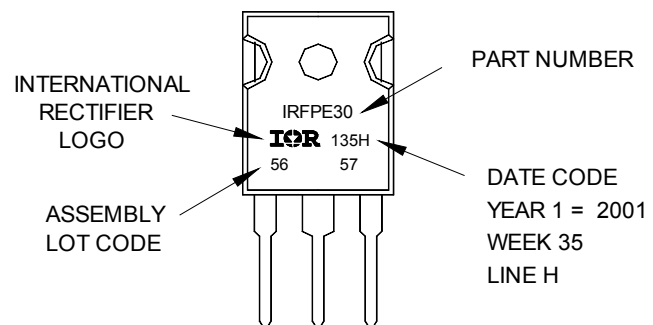
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"

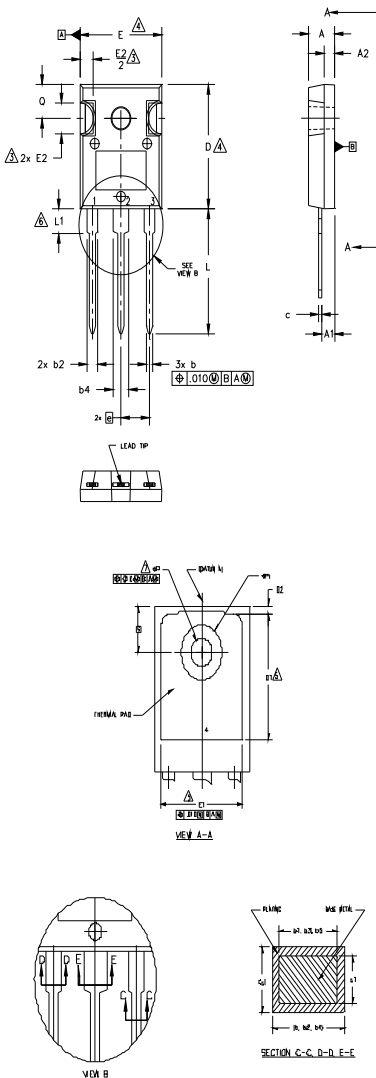


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

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HEXFET

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IGBTs, CoPACK

- 1.- GATE
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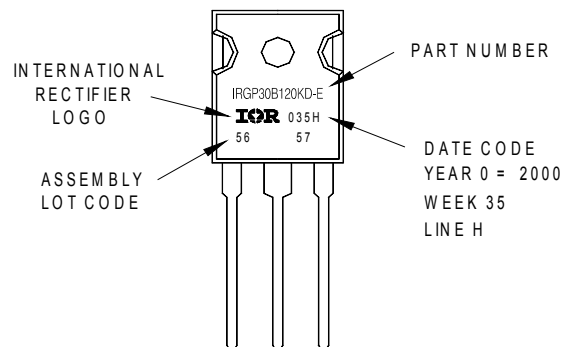
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-247AC	N/A
	TO-247AD	
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
8/21/2014	• Updated I_C vs. T_C graph Fig.2 to match page1 spec data on page 3.
	• Updated package outline on page9

International
 Rectifier

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