

IRFB/IRFS/IRFSL23N15D

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

International
IR Rectifier

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.090	Ω	$V_{GS} = 10V$, $I_D = 14A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 150V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	—	—	S	$V_{DS} = 25V$, $I_D = 14A$
Q_g	Total Gate Charge	—	37	56	nC	$I_D = 14A$
Q_{gs}	Gate-to-Source Charge	—	9.6	14		$V_{DS} = 120V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	19	29	ns	$V_{GS} = 10V$, ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—		$V_{DD} = 75V$
t_r	Rise Time	—	32	—		$I_D = 14A$
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		$R_G = 5.1\Omega$
t_f	Fall Time	—	8.4	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	1200	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	65	—		$f = 1.0MHz$ ⑥
C_{oss}	Output Capacitance	—	1520	—		$V_{GS} = 0V$, $V_{DS} = 1.0V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	120	—		$V_{GS} = 0V$, $V_{DS} = 120V$, $f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	210	—		$V_{GS} = 0V$, $V_{DS} = 0V$ to $120V$ ⑤

Avalanche Characteristics

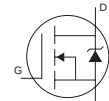
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	260	mJ
I_{AR}	Avalanche Current①	—	14	A
E_{AR}	Repetitive Avalanche Energy①	—	13.6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	92		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 14A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	150	220	ns	$T_J = 25^\circ\text{C}$, $I_F = 14A$
Q_{rr}	Reverse Recovery Charge	—	0.8	1.2	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				



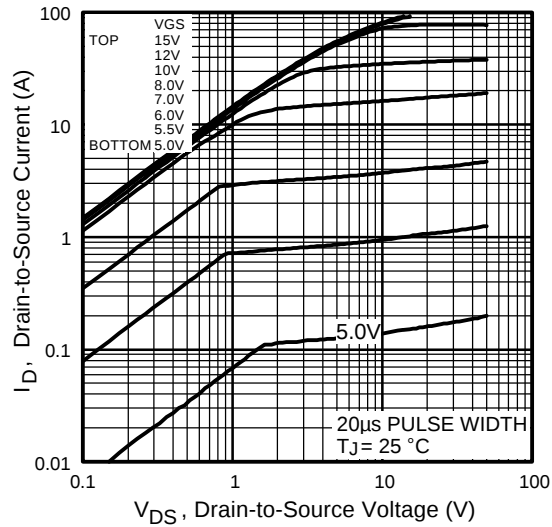


Fig 1. Typical Output Characteristics

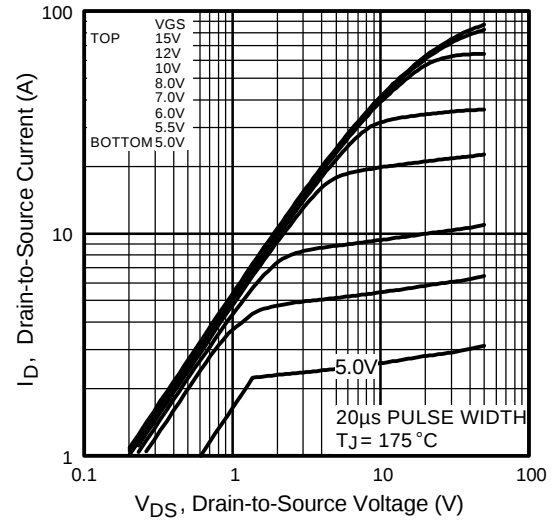


Fig 2. Typical Output Characteristics

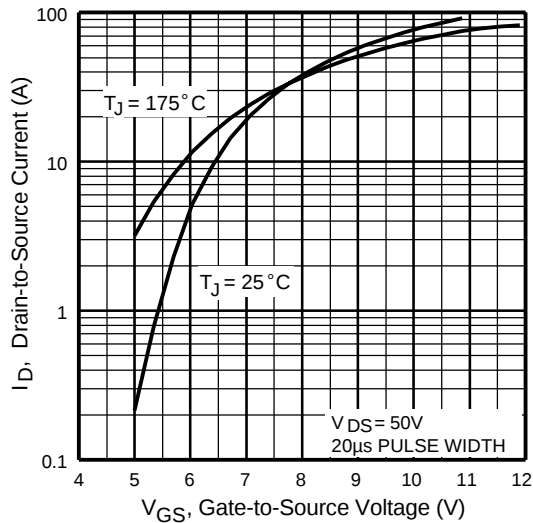


Fig 3. Typical Transfer Characteristics

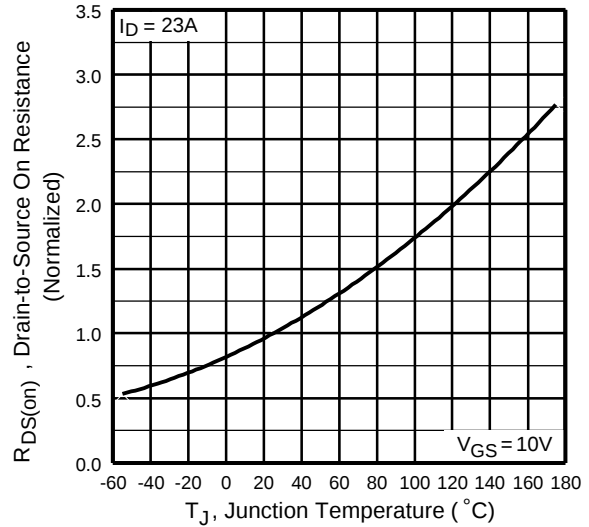
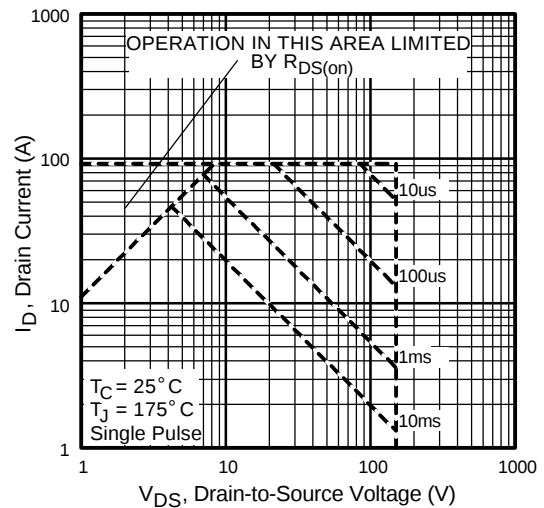
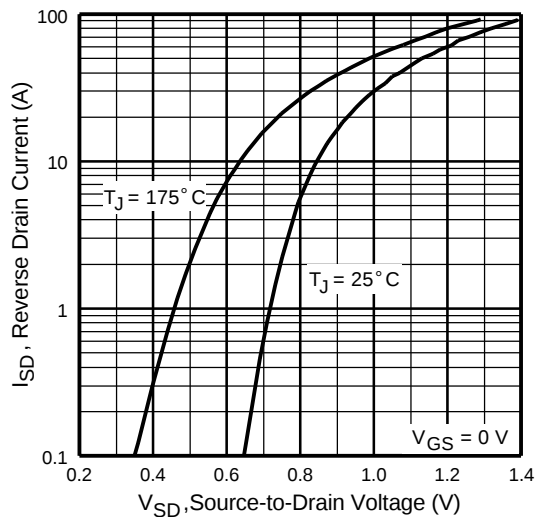
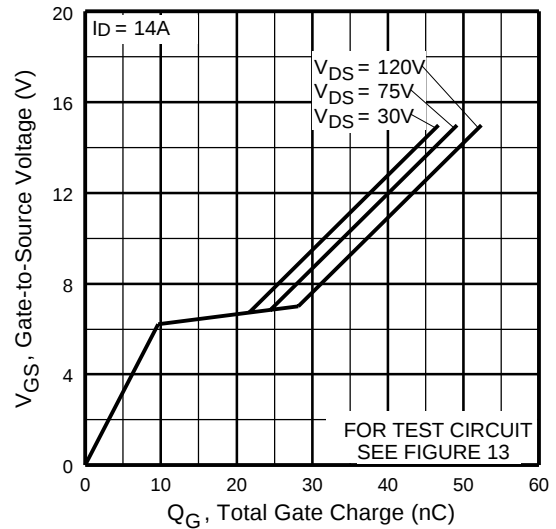
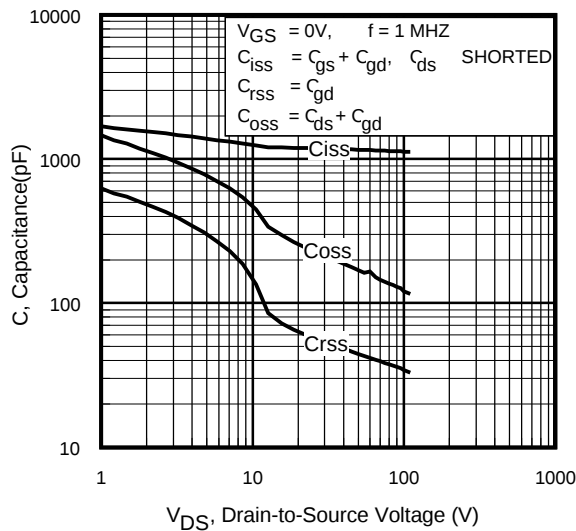


Fig 4. Normalized On-Resistance Vs. Temperature



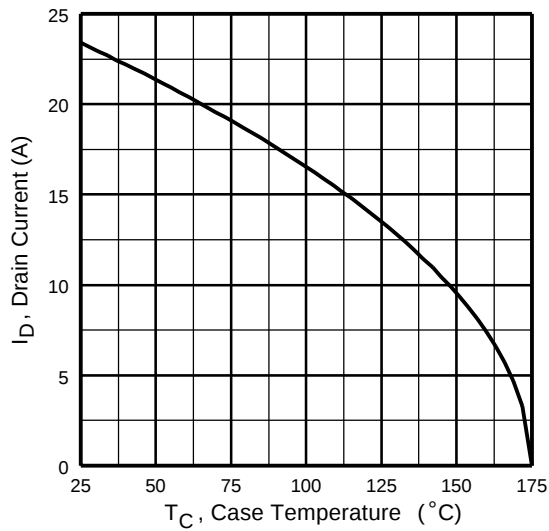


Fig 9. Maximum Drain Current Vs. Case Temperature

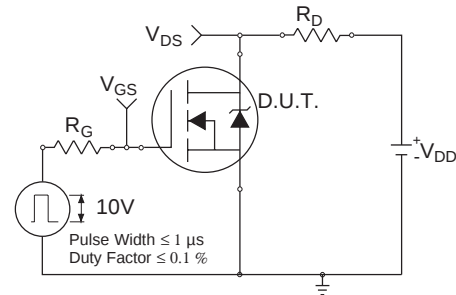


Fig 10a. Switching Time Test Circuit

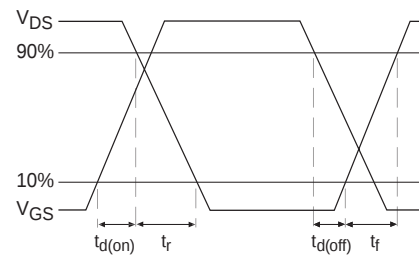


Fig 10b. Switching Time Waveforms

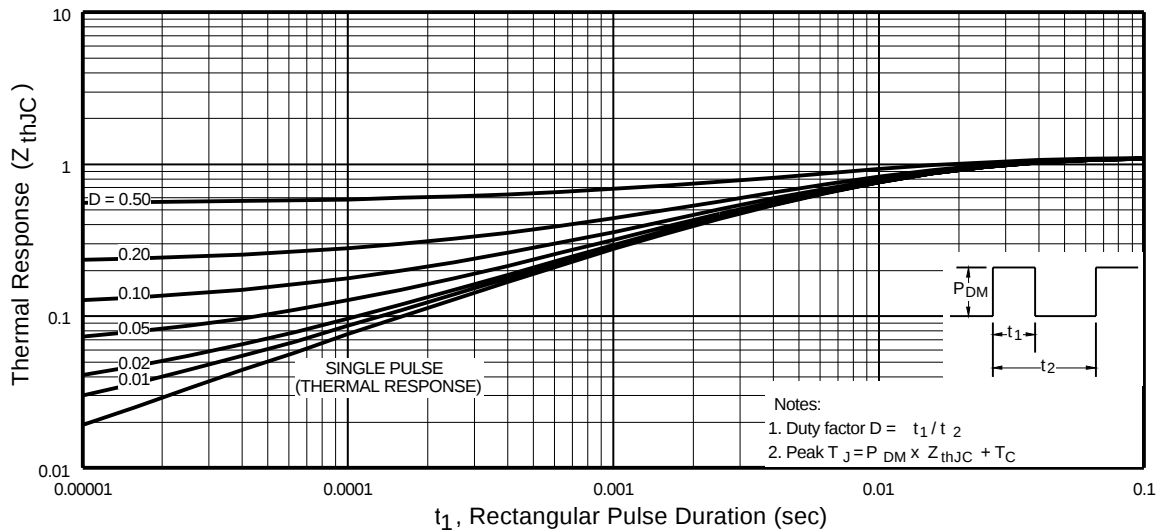


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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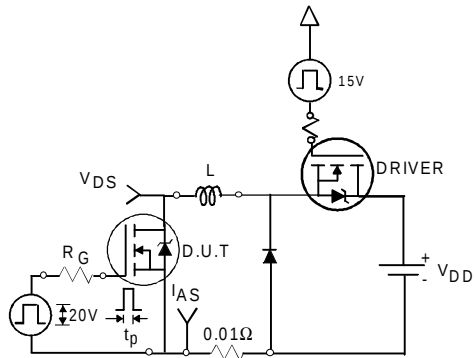


Fig 12a. Unclamped Inductive Test Circuit

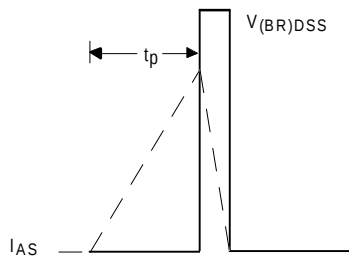


Fig 12b. Unclamped Inductive Waveforms

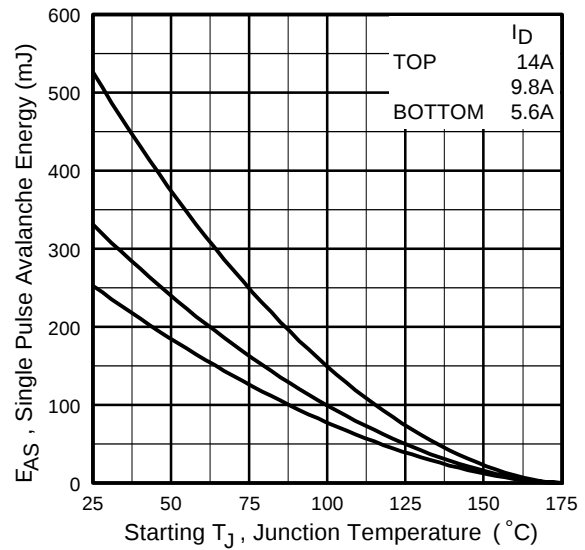


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

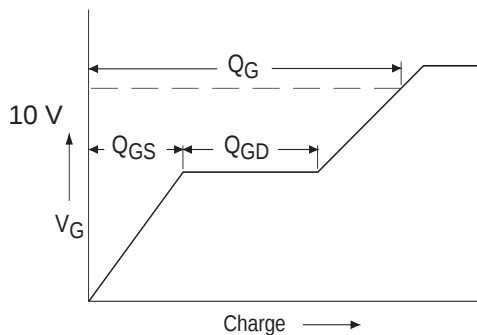


Fig 13a. Basic Gate Charge Waveform

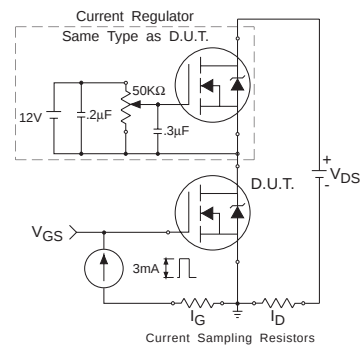
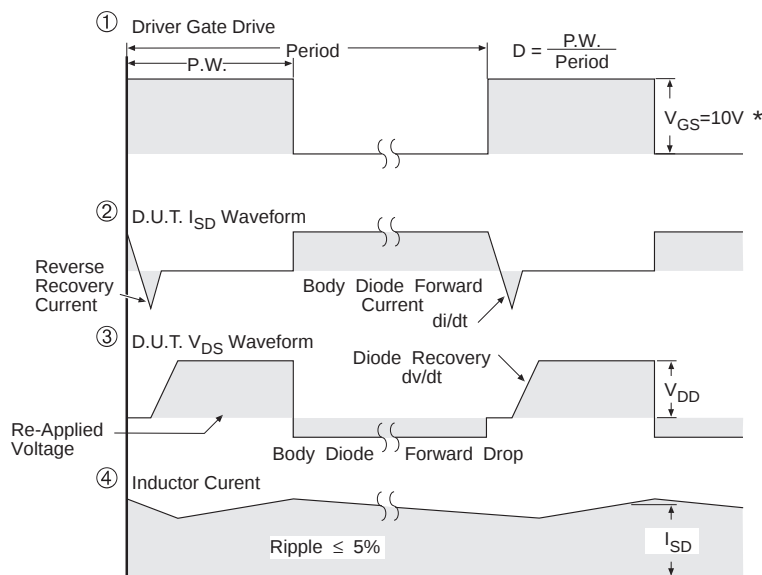
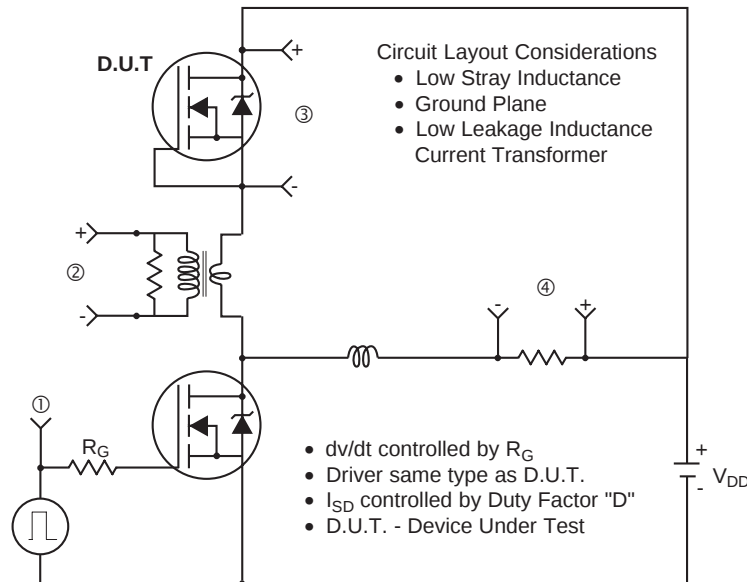


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

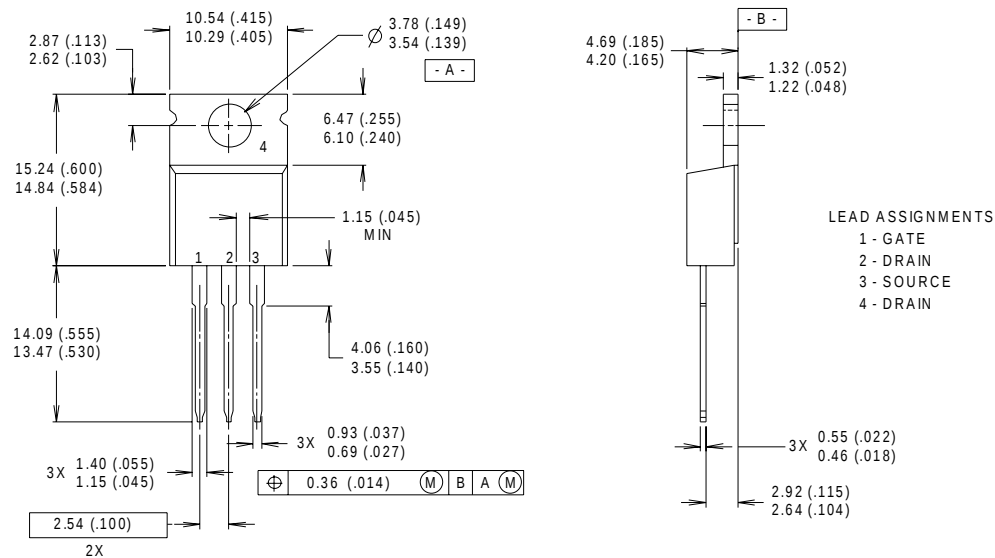
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



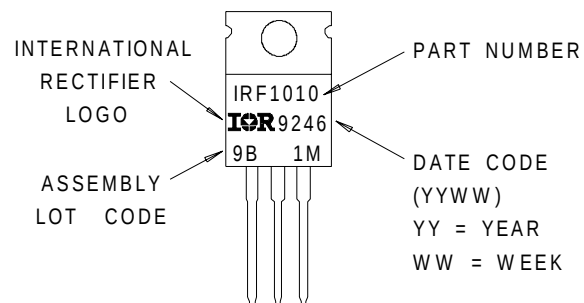
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

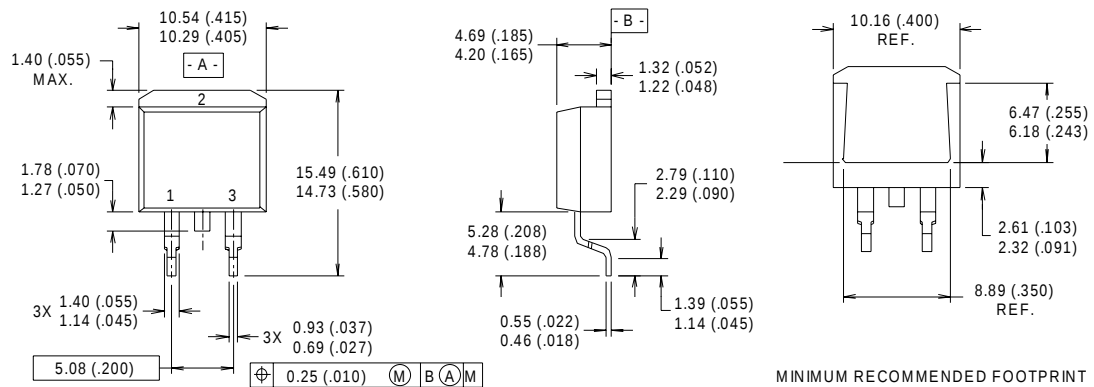
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



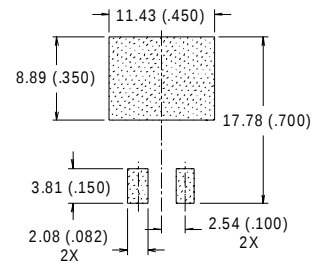
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

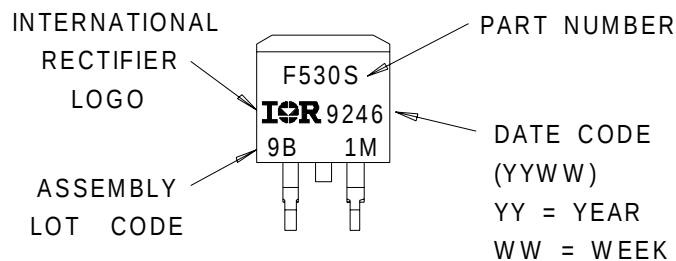
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



D²Pak Part Marking Information



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Technical drawing of a 3-pin connector. The drawing shows a top view and a side view. The top view is a rectangle with a central slot. The side view shows the profile of the connector with three pins. Dimensions are given in inches and millimeters. Lead assignments are provided for each pin.

Dimensions:

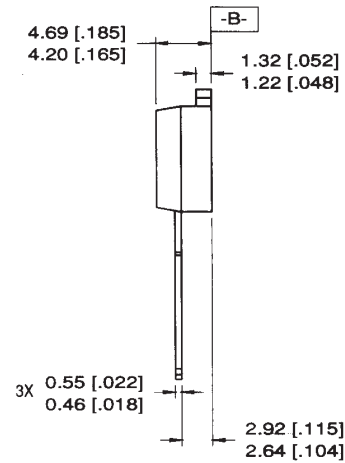
- Top width: 10.54 [.415]
- Top width: 10.29 [.405]
- Top width: -A-
- Top width: 4
- Top width: 1.15 [.045] MIN.
- Top width: 1
- Top width: 2
- Top width: 3
- Top width: -C-
- Top width: 14.09 [.555]
- Top width: 13.47 [.530]
- Top width: 4.06 [.160]
- Top width: 3.55 [.140]
- Top width: 3X 1.40 [.055]
- Top width: 1.15 [.045]
- Top width: 0.93 [.037]
- Top width: 0.69 [.027]
- Top width: 3X
- Top width: 2.54 [.100]
- Top width: 2X

Lead Assignments:

- 1 = GATE
- 2 = DRAIN
- 3 = SOURCE
- 4 = DRAIN

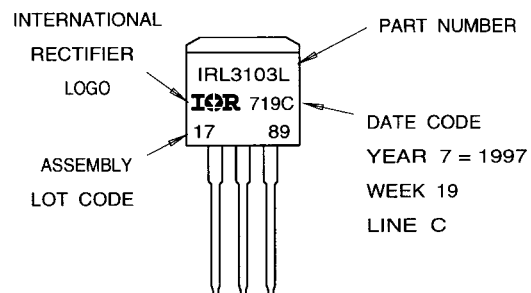
Surface Markings:

- 0.36 [.014]
- M
- B
- A
- M

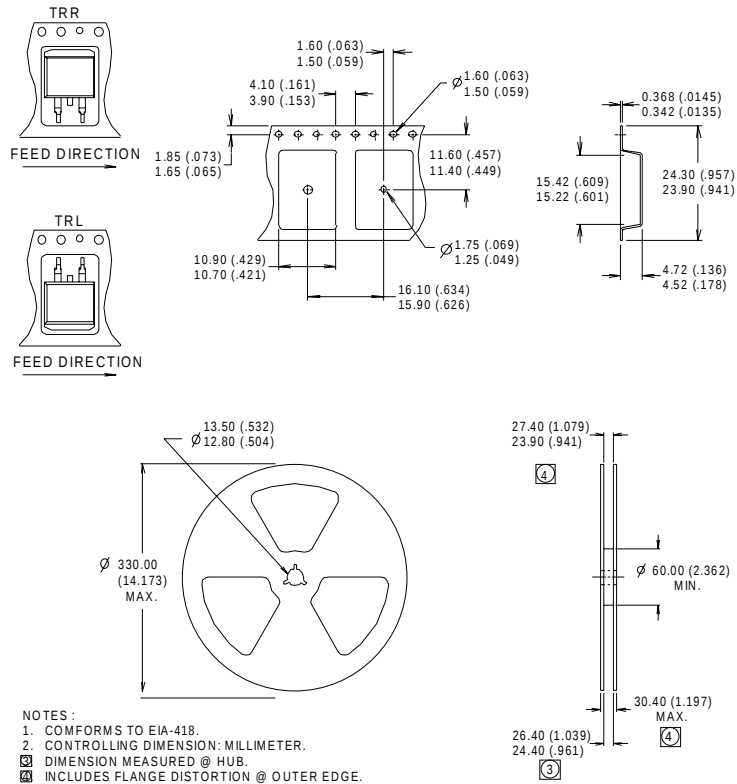


1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 2.7\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 14\text{A}$.
- ③ $I_{SD} \leq 14\text{A}$, $di/dt \leq 240\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>