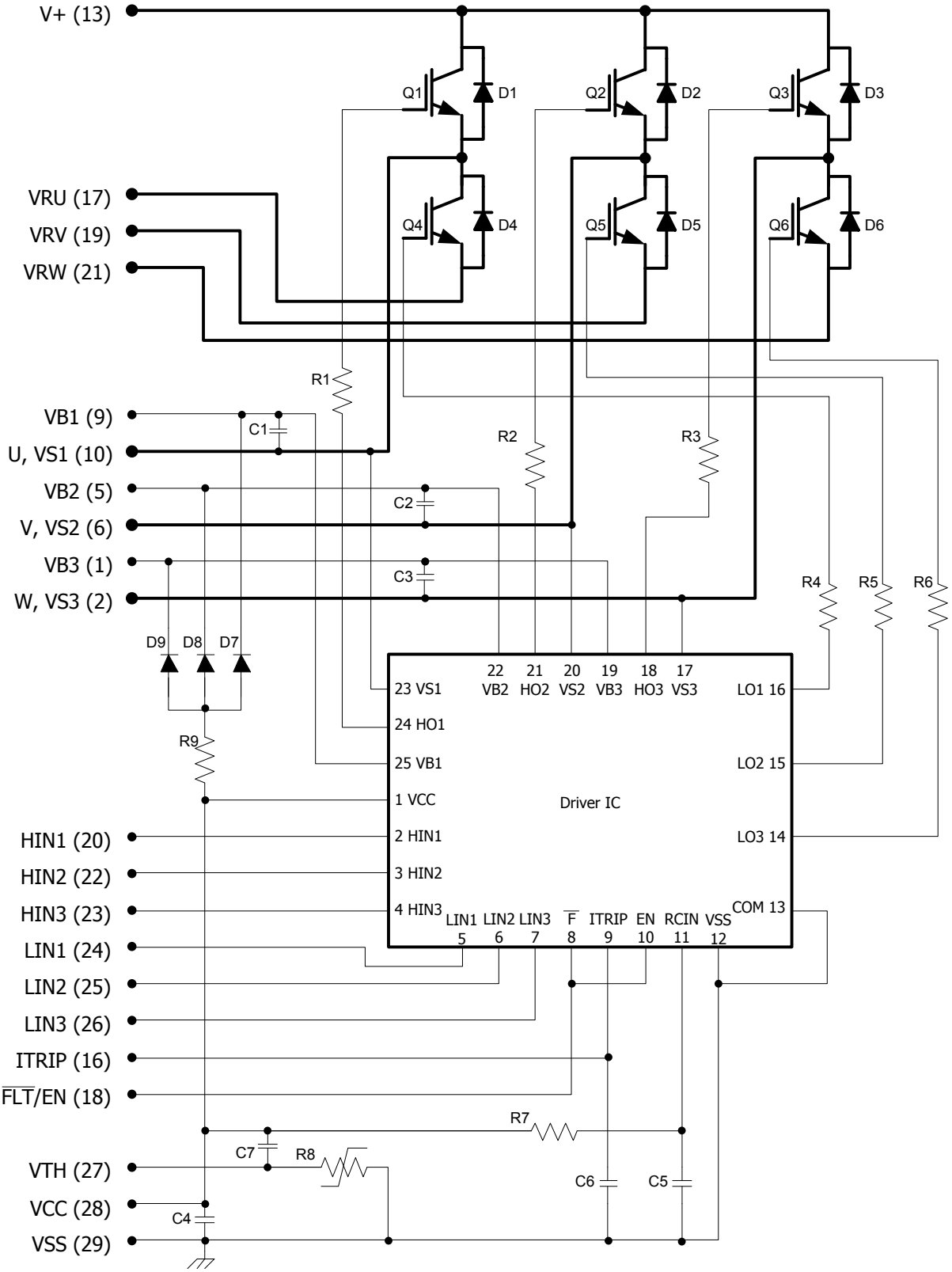
Internal Electrical Schematic – IRAM256-1067A



Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{CES} / V_{RRM}	IGBT/ FW Diode Blocking Voltage	---	600	V
V+	Positive Bus Input Voltage	---	450	
I_O @ T_C=25°C	RMS Phase Current (Note 1)	---	10	A
I_O @ T_C=100°C	RMS Phase Current (Note 1)	---	5	
I_{PK}	Maximum Peak Phase Current (Note 2)	---	15	
F_P	Maximum PWM Carrier Frequency	---	20	kHz
P_D	Maximum Power dissipation per IGBT @ TC =25°C	---	28	W
V_{ISO}	Isolation Voltage (1min)	---	2000	V_{RMS}
T_J (IGBT/Diode/IC)	Operating Junction Temperature	-40	150	°C
T_C	Operating Case Temperature Range	-40	125	
T_{STG}	Storage Temperature Range	-40	125	
T	Mounting torque Range (M3 screw)	0.8	1.0	Nm
I_{BDF}	Bootstrap Diode Peak Forward Current	---	1.0	A
P_{BR_Peak}	Bootstrap Resistor Peak Power (Single Pulse)	---	15	W
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3}$ - 20	$V_{B1,2,3}$ +0.3	V
$V_{B1,2,3}$	High side floating supply voltage	-0.3	600	V
V_{CC}	Low Side and logic fixed supply voltage	-0.3	20	V
V_{IN}	Input voltage LIN, HIN, I_{TRIP}, FLT/EN	-0.3	7	V

Note 1: See Figure 4 and IR IPM Design Tool.
Note 2: t_P<100ms.

Inverter Section Electrical Characteristics

V_{BIAS}(V_{CC}, $V_{BS1,2,3}$)=15V, T_J=25°C unless otherwise specified.

Symbol	Description	Min	Typ	Max	Unit	Conditions
$V_{(BE)CES}$	Collector-to-Emitter Breakdown Voltage	600	---	---	V	V_{IN}=0V, I_C=100µA
$\Delta V_{(BR)CES}$ / ΔT	Temperature Coeff. Of Breakdown Voltage	---	0.3	---	V/°C	V_{IN}=0V, I_C=250A (25°C - 150°C)
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	---	1.5	1.75	V	I_C=4A
		---	1.7	---		I_C=4A, T_J=150°C
I_{CES}	Zero Gate Voltage Collector Current	---	5	80	µA	V_{IN}=0V, V^+=600V
		---	80	---		V_{IN}=0V, V^+=600V, T_J=150°C
V_{FM}	Diode Forward Voltage Drop	---	1.6	2.35	V	I_F=4A
		---	1.3	---		I_F=4A, T_J=150°C
V_{BDFM}	Bootstrap Diode Forward Voltage Drop	---	1.65	1.8	V	I_F=1A
		---	1.3	---		I_F=1A, T_J=150°C
R_{BR}	Bootstrap Resistor Value	---	22	---	Ω	
$\Delta R_{BR}/R_{BR}$	Bootstrap Resistor Tolerance	---	---	±5	%	
$C_{1,2,3,4}$	VCC / VBS Capacitor Value	---	47	---	nF	
C_6	I_{TRIP} Capacitor Value	---	1	---	nF	
C_7	NTC Capacitor Value	---	2.2	---	nF	

Inverter Section Switching Characteristics

V_{BIAS}(V_{CC}, $V_{BS1,2,3}$)=15V, T_J=25°C unless otherwise specified.

Symbol	Description	Min	Typ	Max	Unit	Conditions
E_{ON}	Turn-On Switching Loss	---	170	---	µJ	I_C=4A, V^+=400V V_{CC}=15V, L=1.2mH Energy losses include "tail" and diode reverse recovery See CT1
E_{OFF}	Turn-Off Switching Loss	---	60	---		
E_{TOT}	Total Switching Loss	---	230	---		
E_{REC}	Diode Reverse Recovery energy	---	15	---		
T_{RR}	Diode Reverse Recovery time	---	115	---	ns	
E_{ON}	Turn-On Switching Loss	---	260	---	µJ	I_C=4A, V^+=400V V_{CC}=15V, L=1.2mH, T_J=150°C Energy losses include "tail" and diode reverse recovery See CT1
E_{OFF}	Turn-Off Switching Loss	---	100	---		
E_{TOT}	Total Switching Loss	---	360	---		
E_{REC}	Diode Reverse Recovery energy	---	40	---		
T_{RR}	Diode Reverse Recovery time	---	150	---	ns	
Q_G	Turn-On IGBT Gate Charge	---	13	---	nC	I_C=6A, V^+=400V, V_{GE}=15V
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J=150°C, I_C=20A, V_P=600V V^+= 450V, V_{CC}=+15V to 0V See CT3
SCSOA	Short Circuit Safe Operating Area	5	---	---	µs	T_J=25°C, V^+= 400V, V_{GE}=+15V to 0V
SCSOA	Short Circuit Safe Operating Area	3	---	---	µs	T_J=100°C, V^+= 400V, V_{GE}=+15V to 0V

Recommended Operating Conditions Driver Function

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM. The VS offset is tested with all supplies biased at 15V differential (Note 3)

Symbol	Description	Min	TYP	Max	Unit
$V_{B1,2,3}$	High side floating supply voltage	V_S+12.5	V_S+15	V_S+17.5	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 4	---	450	V
V_{CC}	Low side and logic fixed supply voltage	13.5	15	16.5	V
V_{IN}	Input voltage LIN, HIN, I_{TRIP}, FLT/EN	V_{SS}	---	V_{SS}+5	V
HIN	High side PWM pulse width	1	---	---	µs
Deadtime	External dead time between HIN and LIN	1	---	---	µs

Note 3: For more details, see IR21364 data sheet
Note 4: Logic operational for V_S from COM-5V to COM+600V. Logic state held for V_S from COM-5V to COM-V_{BS}. (please refer to DT97-3 for more details)

Static Electrical Characteristics Driver Function

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$)=15V, T_J=25ºC, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to all six channels. (Note 3)

Symbol	Description	Min	TYP	Max	Unit
$V_{IN,TH+}$	Positive going input threshold for LIN, HIN, FLT/EN	2.5	---	---	V
$V_{IN,TH-}$	Negative going input threshold for LIN, HIN, FLT/EN	---	---	0.8	V
V_{CCUV+}, V_{BSUV+}	VCC/VBS supply undervoltage, Positive going threshold	10.6	11.1	11.6	V
V_{CCUV-}, V_{BSUV-}	VCC/VBS supply undervoltage, Negative going threshold	10.4	10.9	11.4	V
V_{CCUVH}, V_{BSUVH}	VCC and VBS supply undervoltage lock-out hysteresis	---	0.2	---	V
I_{QBS}	Quiescent VBS supply current	---	---	150	µA
I_{QCC}	Quiescent VCC supply current	---	---	3.2	mA
I_{LK}	Offset Supply Leakage Current	---	---	50	µA
I_{IN+}	Input bias current VIN=3.3V for LIN, HIN, FLT/EN	---	100	195	µA
I_{IN-}	Input bias current VIN=0V for LIN, HIN, FLT/EN	-1	---	---	µA
I_{ITRIP+}	I_{TRIP} bias current V_{ITRIP}=3.3V	---	3.3	6	µA
I_{ITRIP-}	I_{TRIP} bias current V_{ITRIP}=0V	-1	---	---	µA
V_{ITRIP}	I_{TRIP} threshold Voltage	0.44	0.49	0.54	V
V_{ITRIP_HYS}	I_{TRIP} Input Hysteresis	---	0.07	---	V
R_{FLT}	Fault low on resistance	---	50	100	Ω

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$)=15V, T_J=25ºC, unless otherwise specified. Dynamic parameters are guaranteed by design. (Note 3)

Symbol	Description	Min	Typ	Max	Unit	Conditions
T_{ON}	Input to Output propagation turn-on delay time (see Fig.12)	---	---	1.15	µs	I_C=4A, V^+=300V
T_{OFF}	Input to Output propagation turn-off delay time (see Fig.12)	---	---	1.15	µs	
T_{FILIN}	Input filter time (HIN,LIN)	---	310	---	ns	V_{IN}=0 or V_{IN}=5V
T_{FILEN}	Input filter time (FLT/EN)	100	200	---	ns	V_{EN}=0 or V_{EN}=5V
T_{EN}	EN low to six switch turn-off propagation delay (see fig. 3)	---	---	1.35	µs	V_{IN}=0 or V_{IN}=5V, V_{EN}=0
T_{FLT}	I_{TRIP} to Fault propagation delay	400	600	800	ns	V_{IN}=0 or V_{IN}=5V, V_{ITRIP}=5V
$T_{BLT-TRIP}$	I_{TRIP} Blanking Time	100	150	---	ns	V_{IN}=0 or V_{IN}=5V, V_{ITRIP}=5V
T_{ITRIP}	I_{TRIP} to six switch turn-off propagation delay (see fig. 2)	---	---	1.5	µs	I_C=4A, V^+=300V
D_T	Internal Dead Time injected by driver	220	290	360	ns	V_{IN}=0 or V_{IN}=5V
M_T	Matching Propagation Delay Time (On & Off) all channels	---	40	75	ns	External dead time> 400ns
$T_{FLT-CLR}$	Post I_{TRIP} to six switch turn-off clear time (see fig. 2)	1.1	1.7	2.3	ms	T_C = 25°C
		1	1.5	1.9		T_C = 100°C

Thermal and Mechanical Characteristics

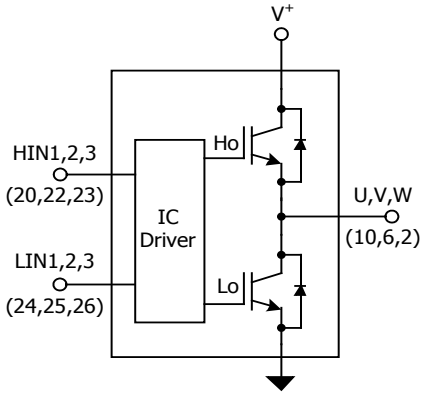
Symbol	Description	Min	Typ	Max	Unit	Conditions
$R_{TH(J-C)}$	Thermal resistance, per IGBT	---	3.5	4.4	°C/W	Inverter Operating Condition Flat, greased surface. Heatsink compound thermal conductivity 1W/mK
$R_{TH(J-C)}$	Thermal resistance, per Diode	---	5.0	6.3		
$R_{TH(C-S)}$	Thermal resistance, C-S	---	0.1	---		
CTI	Comparative Tracking Index	600	---	---	V	
BKCurve	Curvature of module backside	0	---	---	µm	Convex only

Note 5: Flatness of the heatsink should be between -50µm to 100µm.

Internal NTC - Thermistor Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
R_{25}	Resistance	44.65	47	49.35	kΩ	T_C = 25°C
R_{125}	Resistance	1.27	1.41	1.56	kΩ	T_C = 125°C
B	B-constant (25-50°C)	3989	4050	4111	k	$R_2 = R_1 e^{[B(1/T2 - 1/T1)]}$
Temperature Range		-40	---	125	°C	
Typ. Dissipation constant		---	1	---	mW/°C	T_C = 25°C

Input-Output Logic Level Table



FLT/EN	I_{TRIP}	HIN1,2,3	LIN1,2,3	U,V,W
1	0	1	0	V+
1	0	0	1	0
1	0	0	0	Off
1	0	1	1	Off
1	1	X	X	Off
0	X	X	X	Off

Qualification Information†

Qualification Level		Industrial†† (per JEDEC JESD 47E)
ESD	**Machine Model**	Class C (per JEDEC standard JESD22-A115-A)
	Human Body Model	Class 1C (per JEDEC standard JESD22-A114-D)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

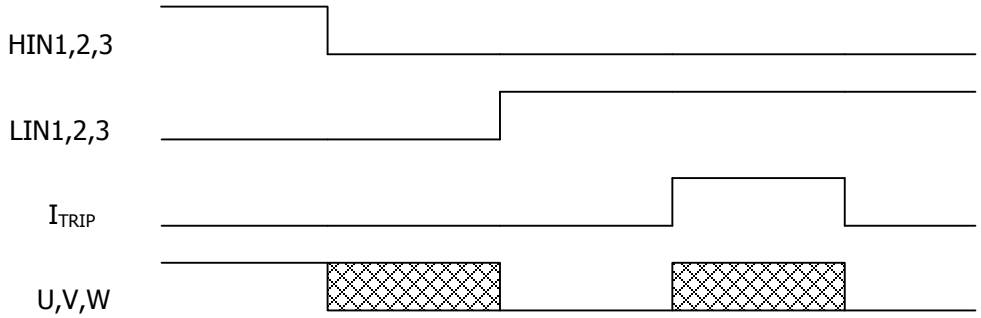


Figure 1. Input/Output Timing Diagram

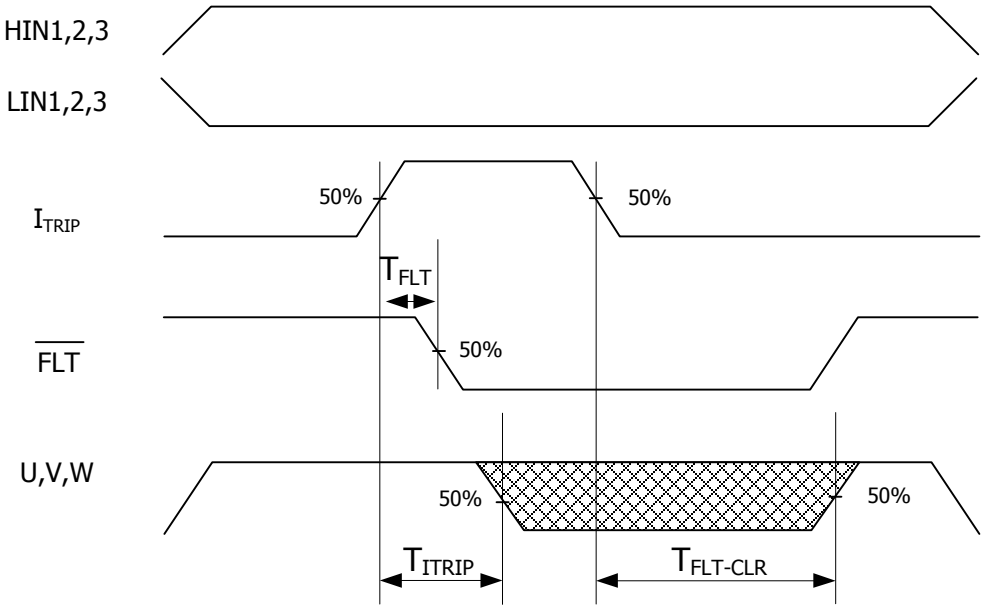


Figure 2. I_{TRIP} Timing Waveform

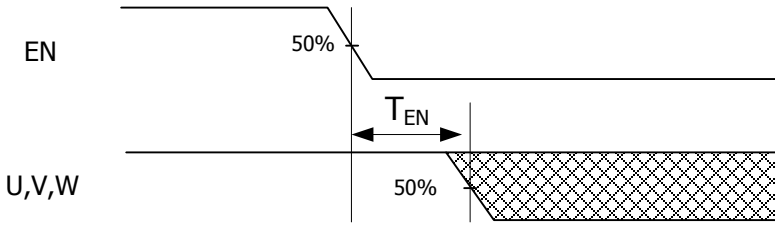


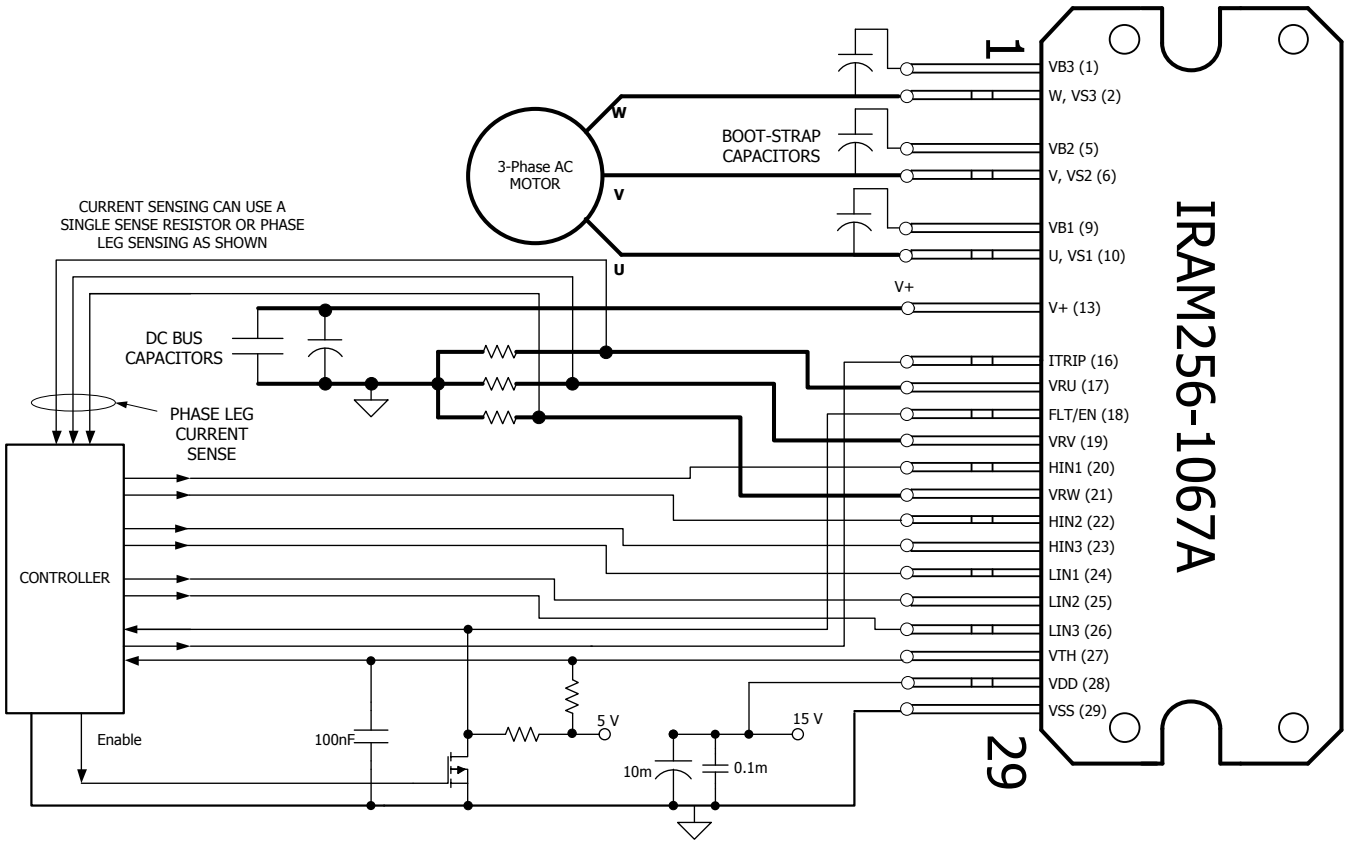
Figure 3. Output Enable Timing Diagram

Note 5: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

Module Pin-Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W,VS3	Output 3 - High Side Floating Supply Offset Voltage
3	N/A	None
4		
5	VB2	High Side Floating Supply Voltage 2
6	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
7	N/A	None
8		
9	VB1	High Side Floating Supply Voltage 1
10	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
11	N/A	None
12		
13	V+	Positive Bus Input Voltage
14	N/A	None
15		
16	I_{TRIP}	Current Protection Pin
17	VRU	Low Side Emitter Connection - Phase 1
18	FLT/EN	Fault Output and Enable Pin
19	VRV	Low Side Emitter Connection - Phase 2
20	HIN1	Logic Input High Side Gate Driver - Phase 1
21	VRW	Low Side Emitter Connection - Phase 3
22	HIN2	Logic Input High Side Gate Driver - Phase 2
23	HIN3	Logic Input High Side Gate Driver - Phase 3
24	LIN1	Logic Input Low Side Gate Driver - Phase 1
25	LIN2	Logic Input Low Side Gate Driver - Phase 2
26	LIN3	Logic Input Low Side Gate Driver - Phase 3
27	VTH	Temperature Feedback
28	VCC	+15V Main Supply
29	VSS	Negative Main Supply

Typical Application Connection IRAM256-1067A



1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

2. In order to provide good decoupling between VCC-VSS and VB1,2,3-VS1,2,3 terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1µF, are strongly recommended.

3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a, application note AN-1044 or Figure 9. Bootstrap capacitor value must be selected to limit the power dissipation of the internal resistor in series with the VCC. (see maximum ratings Table on page 3).

4. After approx. 2ms the FAULT is reset. (see Dynamic Characteristics Table on page 5).

5. PWM generator must be disabled within Fault duration to guarantee shutdown of the system, overcurrent condition must be cleared before resuming operation.

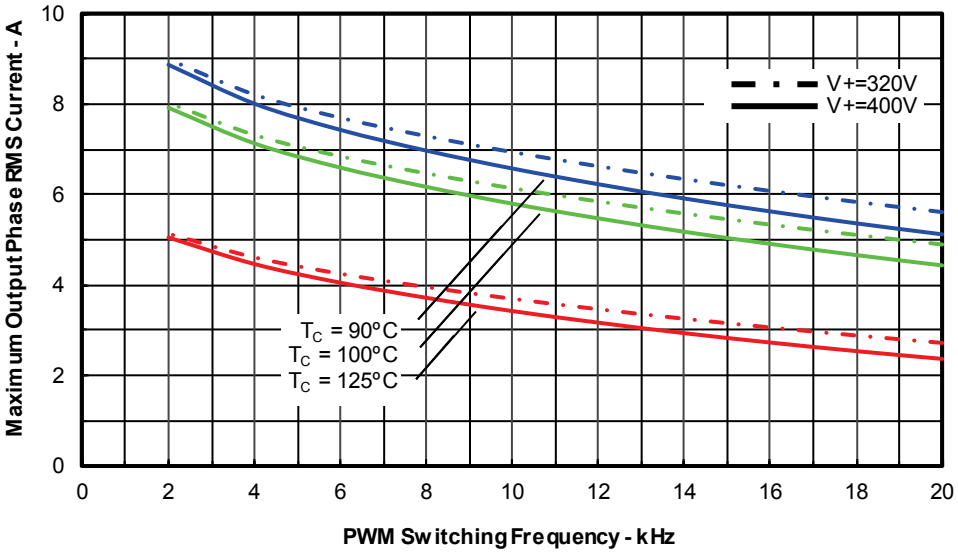


Figure 4. Maximum Sinusoidal Phase Current vs. PWM Switching Frequency
Sinusoidal Modulation, T_J=150°C, MI=0.8, PF=0.6, fmod=50Hz

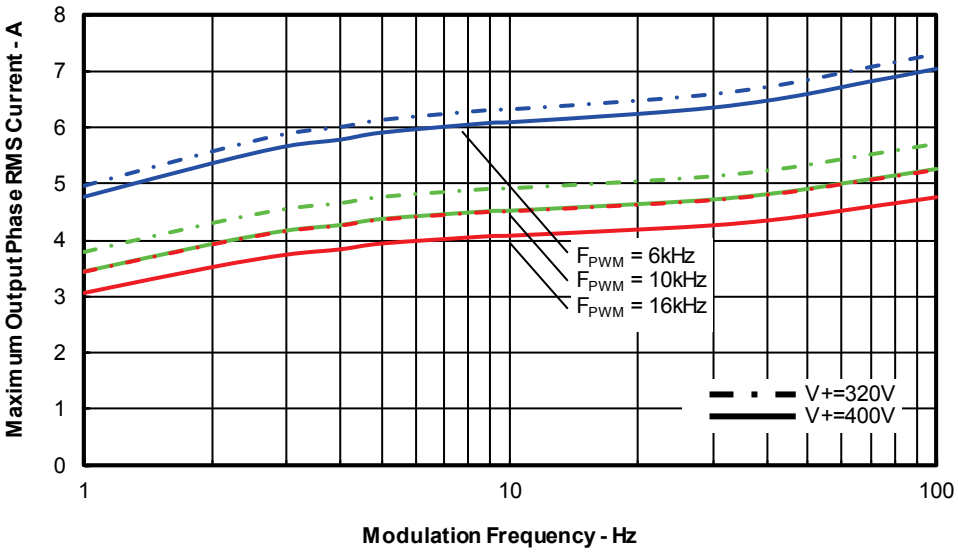


Figure 5. Maximum Sinusoidal Phase Current vs. Modulation Frequency
Sinusoidal Modulation, T_J=150°C, T_C=100°C, MI=0.8, PF=0.6

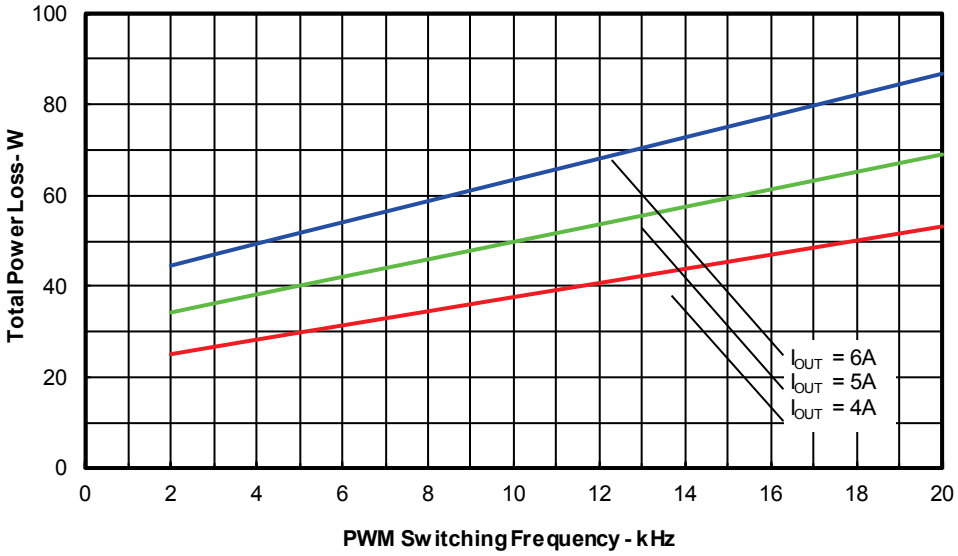


Figure 6. Total Power Losses vs. PWM Switching Frequency
Sinusoidal Modulation, V^+=400V, T_J=150°C, MI=0.8, PF=0.6, fmod=50Hz

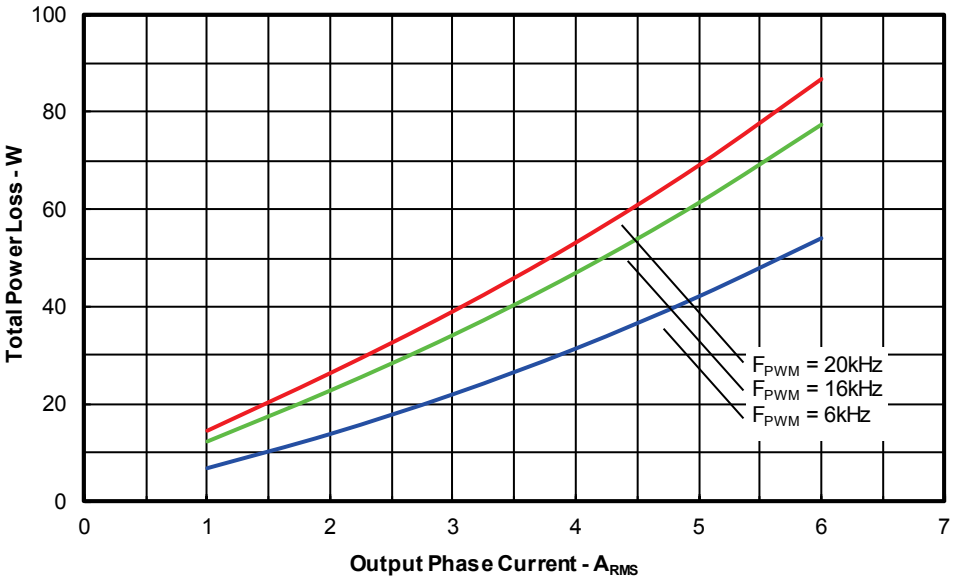


Figure 7. Total Power Losses vs. Output Phase Current
Sinusoidal Modulation, V^+=400V, T_J=150°C, MI=0.8, PF=0.6, fmod=50Hz

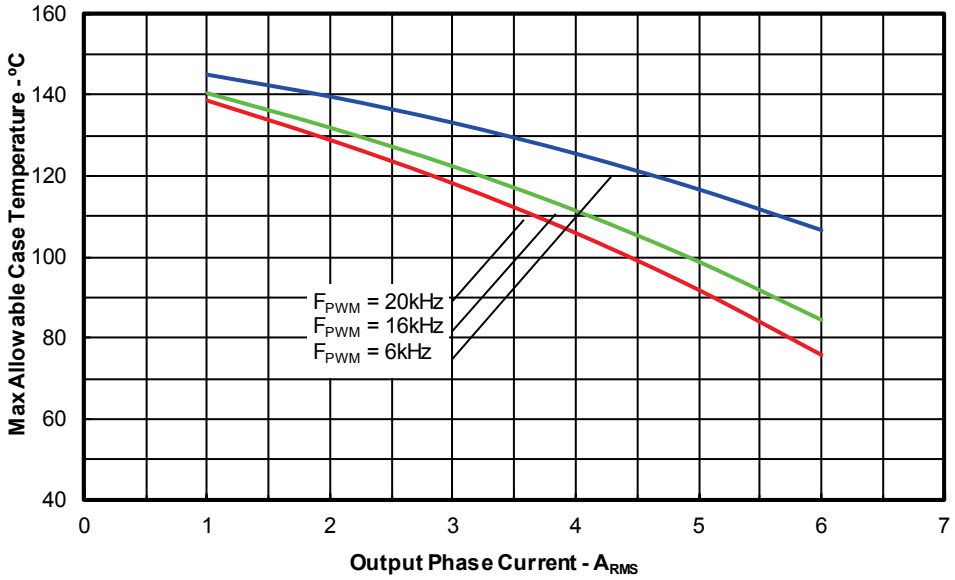


Figure 8. Maximum Allowable Case Temperature vs. Output RMS Current per Phase
Sinusoidal Modulation, V^+=400V, T_J=150°C, MI=0.8, PF=0.6, fmod=50Hz

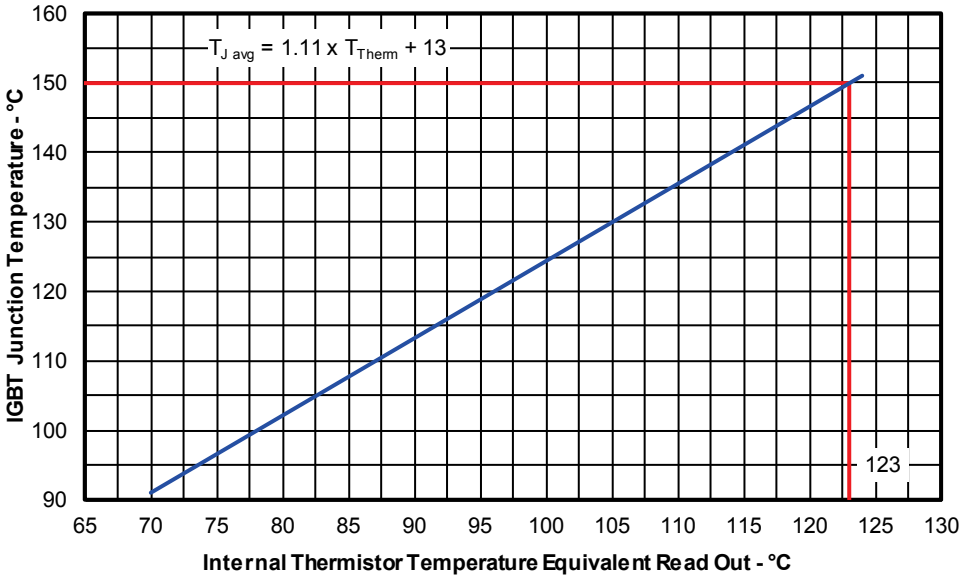
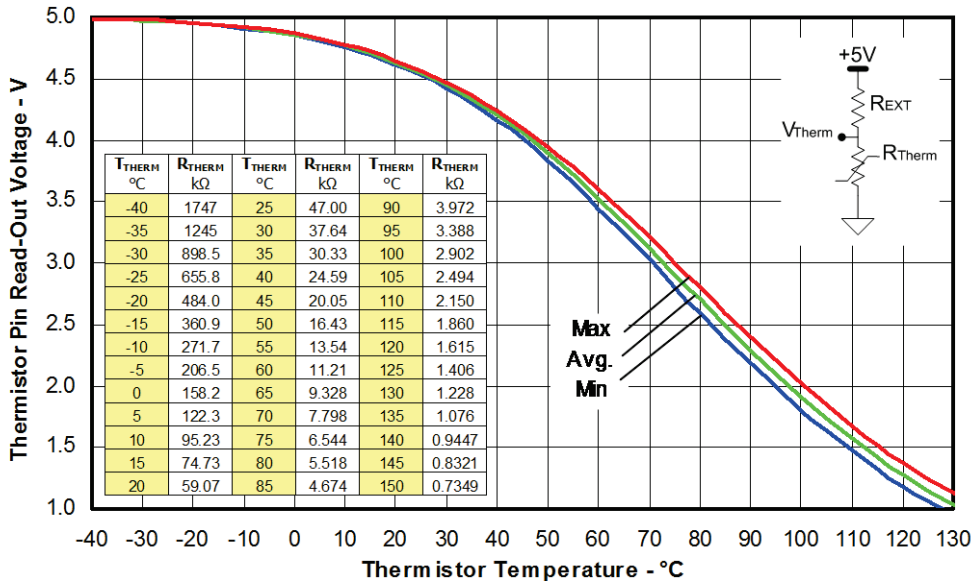


Figure 9. Estimated Maximum IGBT Junction Temperature vs. Thermistor Temperature
Sinusoidal Modulation, V^+=400V, Iphase=5Arms, fsw=6kHz, fmod=50Hz, MI=0.8, PF=0.6



T_{THERM} °C	R_{THERM} kΩ	T_{THERM} °C	R_{THERM} kΩ	T_{THERM} °C	R_{THERM} kΩ
-40	1747	25	47.00	90	3.972
-35	1245	30	37.64	95	3.388
-30	898.5	35	30.33	100	2.902
-25	655.8	40	24.59	105	2.494
-20	484.0	45	20.05	110	2.150
-15	360.9	50	16.43	115	1.860
-10	271.7	55	13.54	120	1.615
-5	206.5	60	11.21	125	1.406
0	158.2	65	9.328	130	1.228
5	122.3	70	7.798	135	1.076
10	95.23	75	6.544	140	0.9447
15	74.73	80	5.518	145	0.8321
20	59.07	85	4.674	150	0.7349

Figure 10. Thermistor Readout vs. Temperature (7.5kohm REXT pull-down resistor) and Normal Thermistor Resistance values vs. Temperature Table.

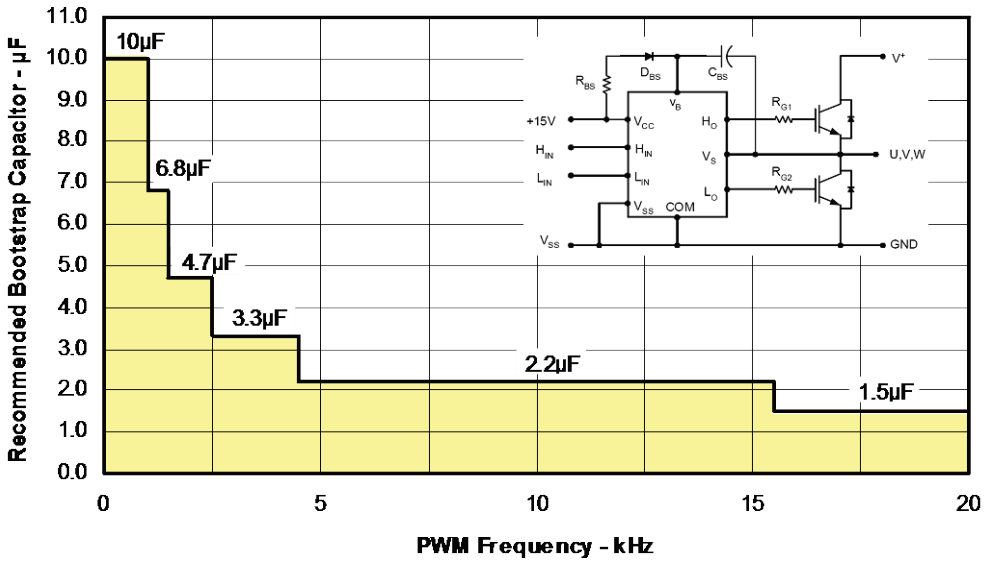


Figure 11. Recommended Bootstrap Capacitor Value vs. Switching Frequency

Figure 12. Switching Parameter Definitions

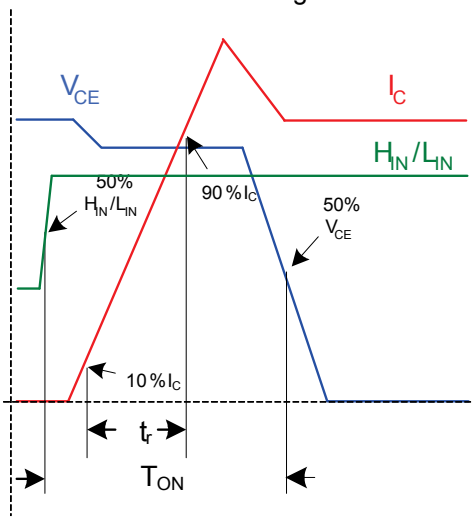


Figure 12a. Input to Output propagation turn-on delay time.

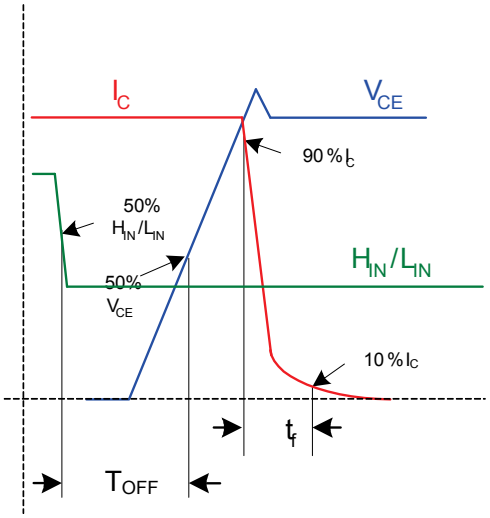


Figure 12b. Input to Output propagation turn-off delay time.

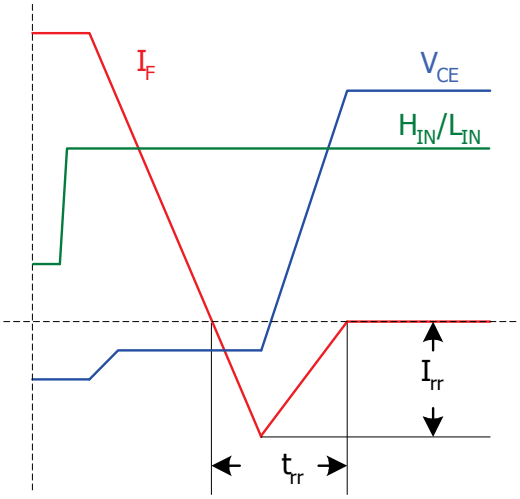


Figure 12c. Diode Reverse Recovery.

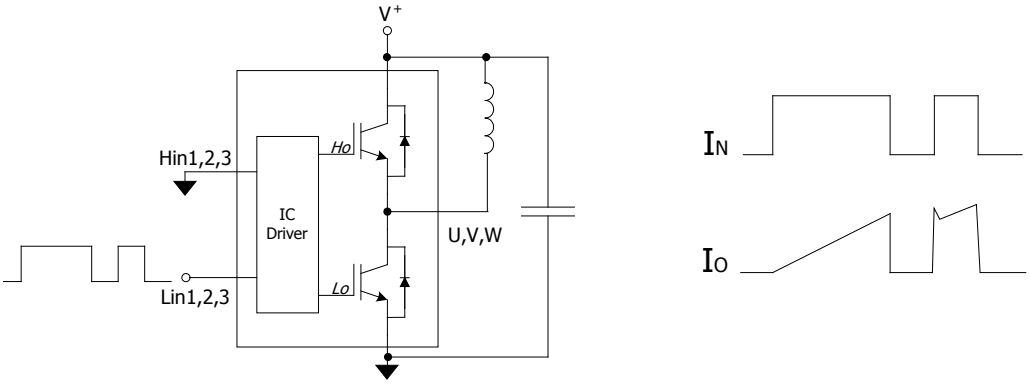


Figure CT1. Switching Loss Circuit

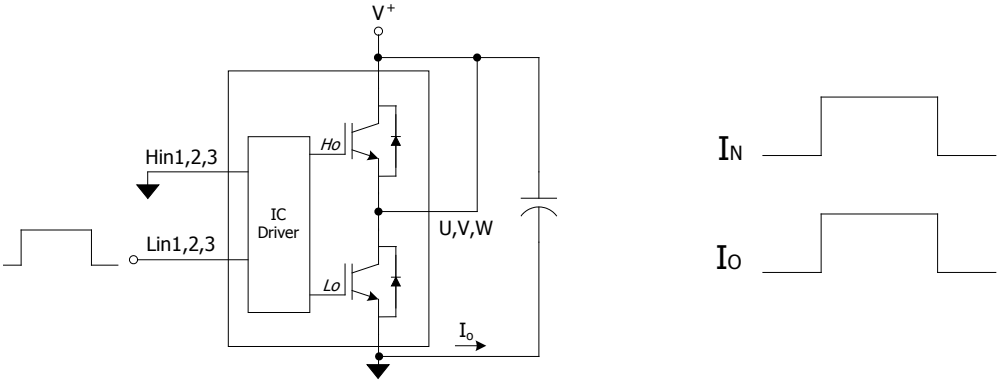


Figure CT2. S.C.SOA Circuit

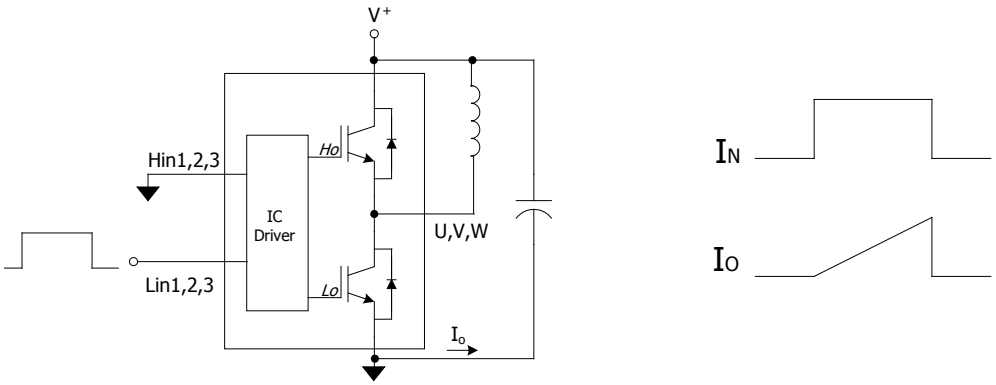
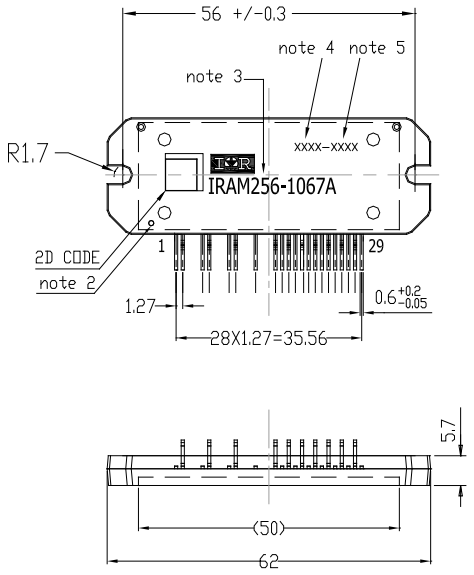
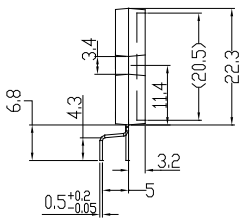


Figure CT3. R.B.SOA Circuit

Package Outline IRAM256-1067A

Missing pins: 3,4,7,8,11,12,14,15





note1: Unit tolerance is +/−0.5mm,
Unless Otherwise Specified.

note2: Mirror Surface Mark indicates Pin 1 Identification.

note3: Part Number Marking.
Characters Font in this drawing differs from Font shown on Module.

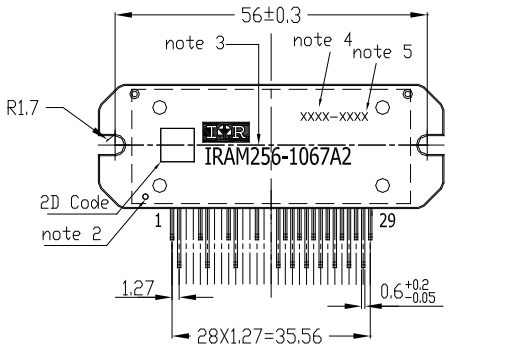
note4: Lot Code Marking.
Characters Font in this drawing differs from Font shown on Module.

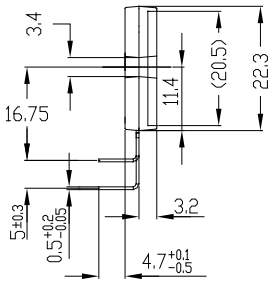
note5: Date Code Marking.
Characters Font in this drawing differs from Font shown on Module.

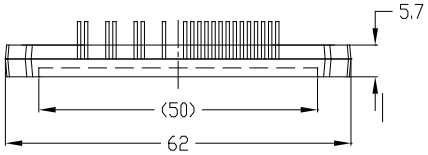
Dimensions in mm
For mounting instruction see AN-1049

Package Outline IRAM256-1067A2

Missing pins: 3,4,7,8,11,12,14,15







note1: Unit tolerance is +/−0.5mm,
Unless Otherwise Specified.
note2: Mirror Surface Mark indicates Pin 1 Identification.
note3: Part Number Marking.
Characters Font in this drawing differs from
Font shown on Module.
note4: Lot Code Marking.
Characters Font in this drawing differs from
Font shown on Module.
note5: Date Code Marking.
Characters Font in this drawing differs from
Font shown on Module.

Dimensions in mm
For mounting instruction see AN-1049