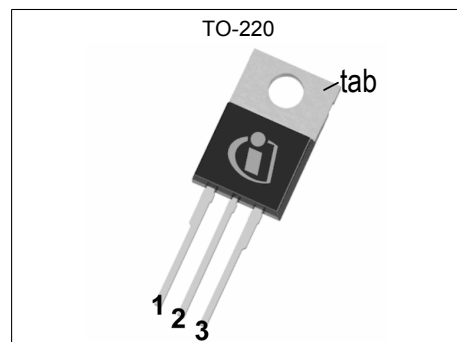


1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- Easy to use/drive
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Enabling higher system efficiency
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures

Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

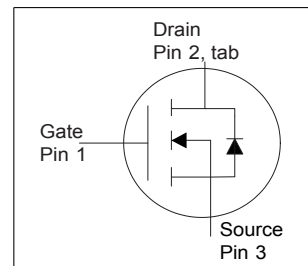


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	95	mΩ
$Q_{g,typ}$	45	nC
$I_{D,pulse}$	100	A
$E_{oss@400V}$	5.5	μJ
Body diode di/dt	60	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPP65R095C7	PG-TO 220	65C7095	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	24 15	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	100	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	118	mJ	$I_D=8.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.59	mJ	$I_D=8.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	8.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	128	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	24	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	100	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1.5	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	60	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.98	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.59mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=650$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.084 0.202	0.095 -	Ω	$V_{GS}=10V$, $I_D=11.8A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=11.8A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.9	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2140	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	33	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	69	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	763	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=11.8A$, $R_G=5.3\Omega$; see table 9
Rise time	t_r	-	12	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=11.8A$, $R_G=5.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	60	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=11.8A$, $R_G=5.3\Omega$; see table 9
Fall time	t_f	-	7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=11.8A$, $R_G=5.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	$V_{DD}=400V$, $I_D=11.8A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	15	-	nC	$V_{DD}=400V$, $I_D=11.8A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	45	-	nC	$V_{DD}=400V$, $I_D=11.8A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400V$, $I_D=11.8A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=11.8A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	800	-	ns	$V_R=400V$, $I_F=24A$, $di_F/dt=60A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	9	-	μC	$V_R=400V$, $I_F=24A$, $di_F/dt=60A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	25	-	A	$V_R=400V$, $I_F=24A$, $di_F/dt=60A/\mu s$; see table 8

5 Electrical characteristics diagrams

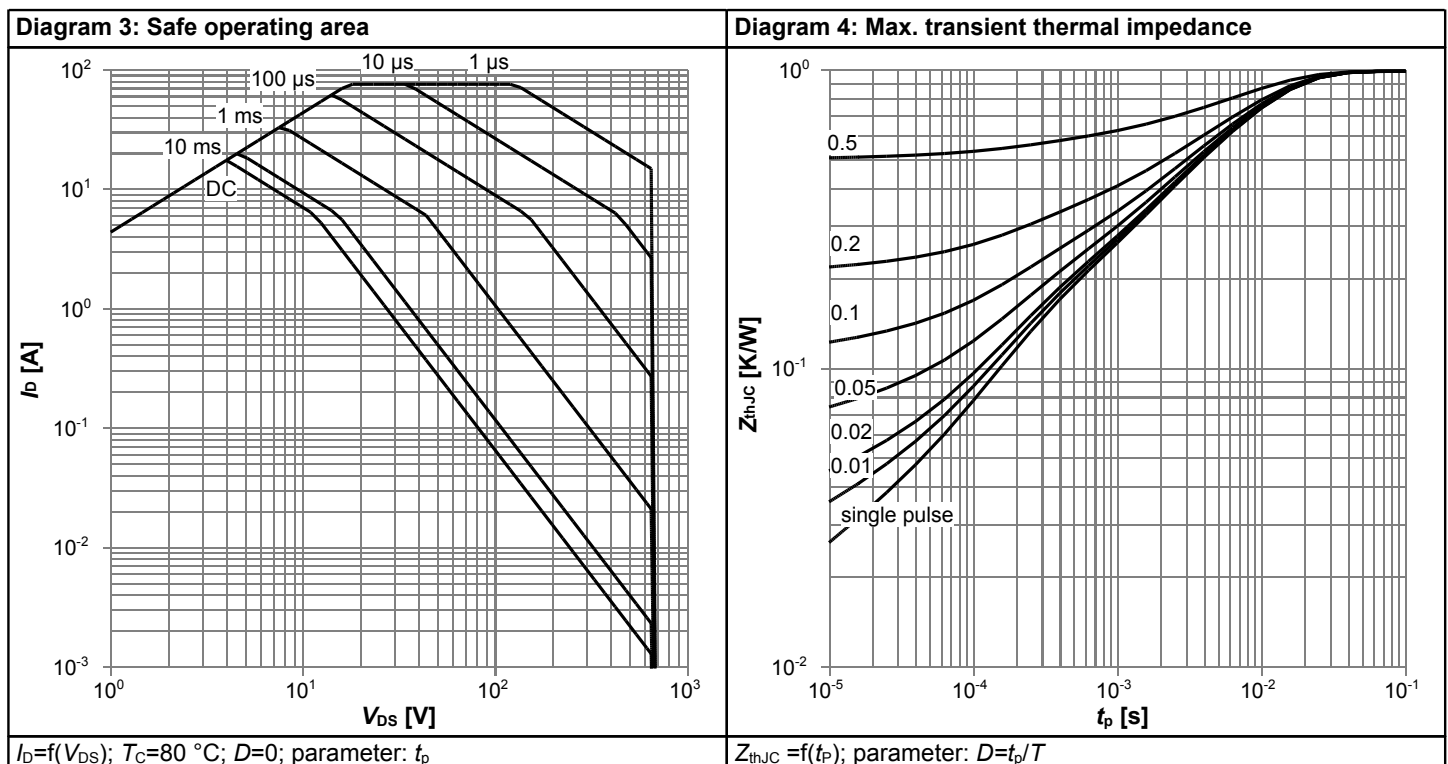
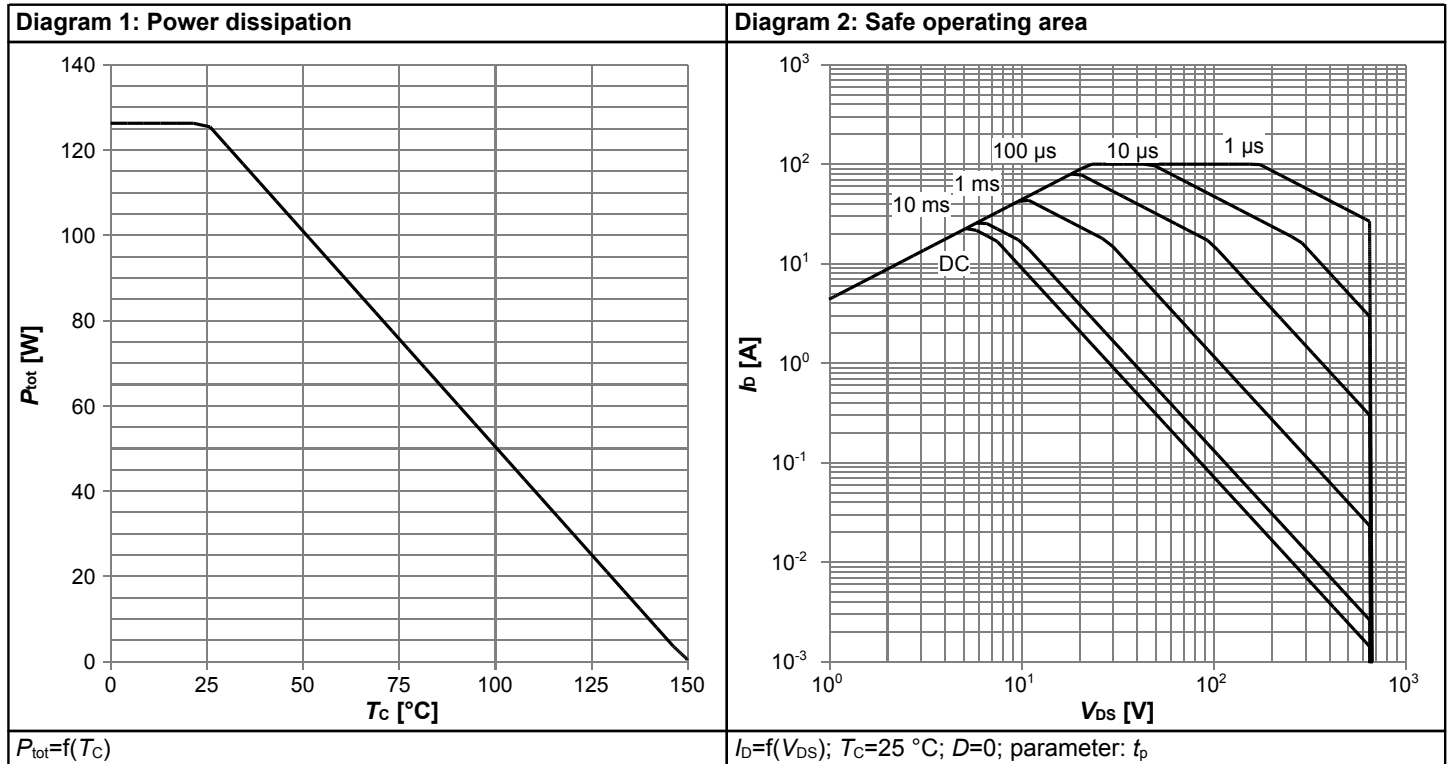


Diagram 5: Typ. output characteristics

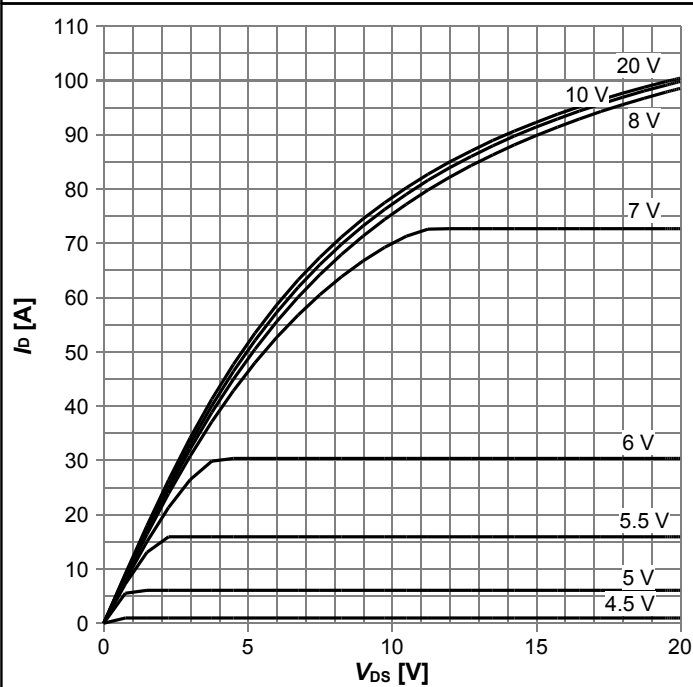

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics

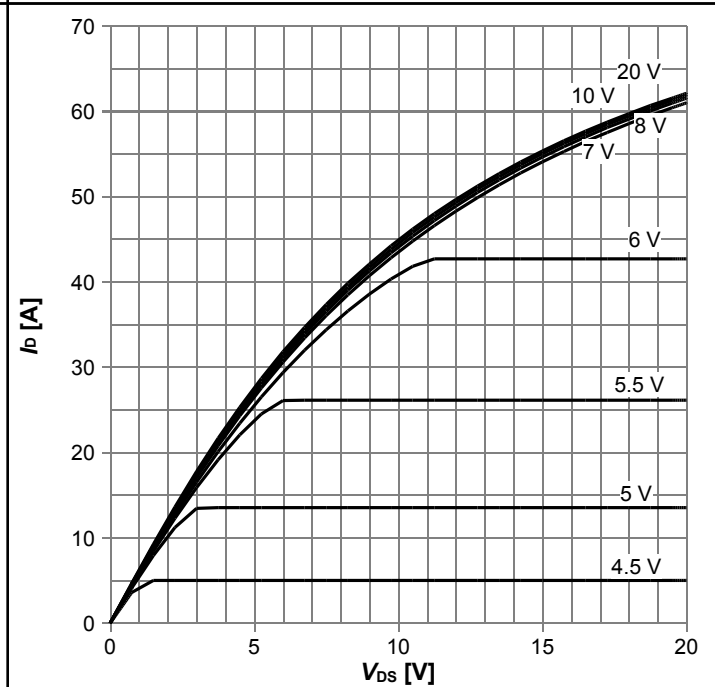

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance

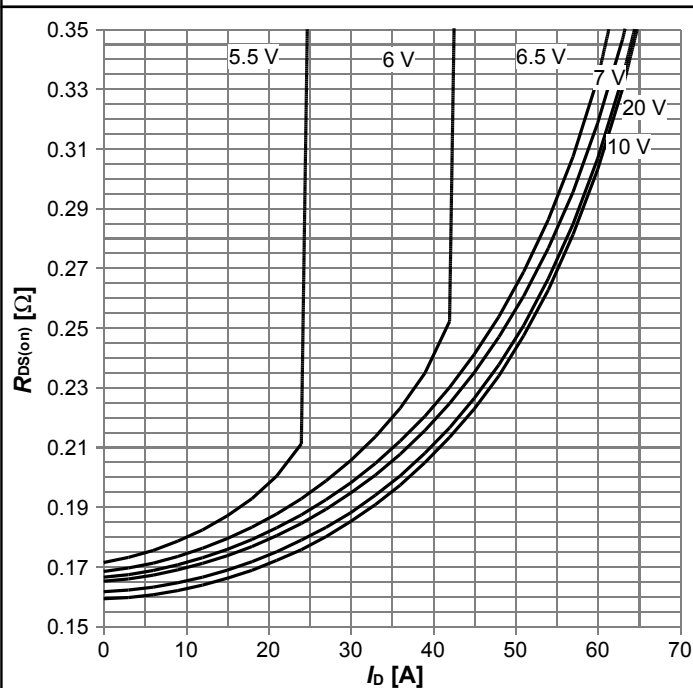

 $R_{DS(on)} = f(I_D); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance

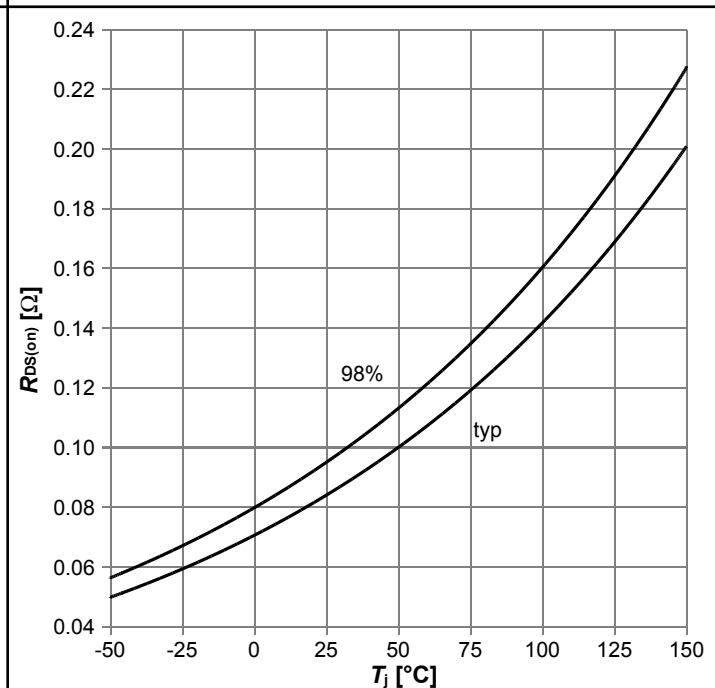

 $R_{DS(on)} = f(T_J); I_D = 11.8\text{ A}; V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics

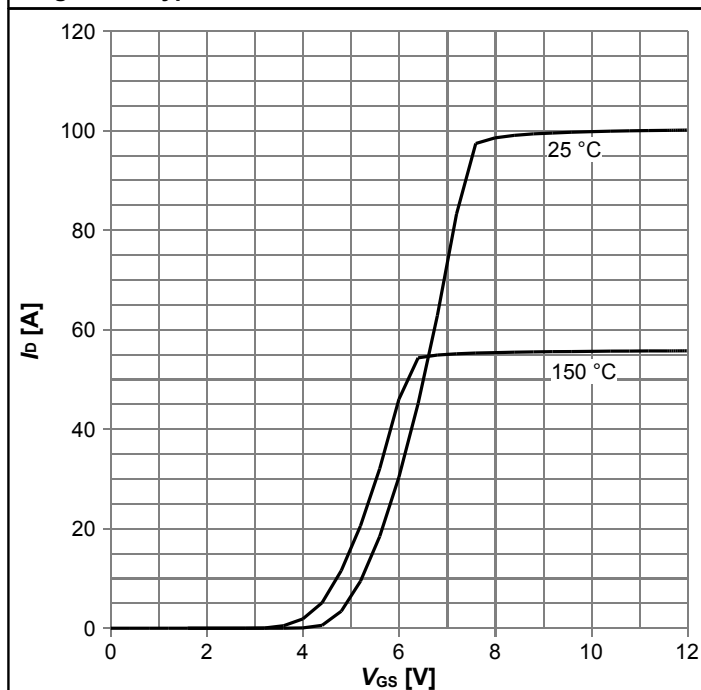

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

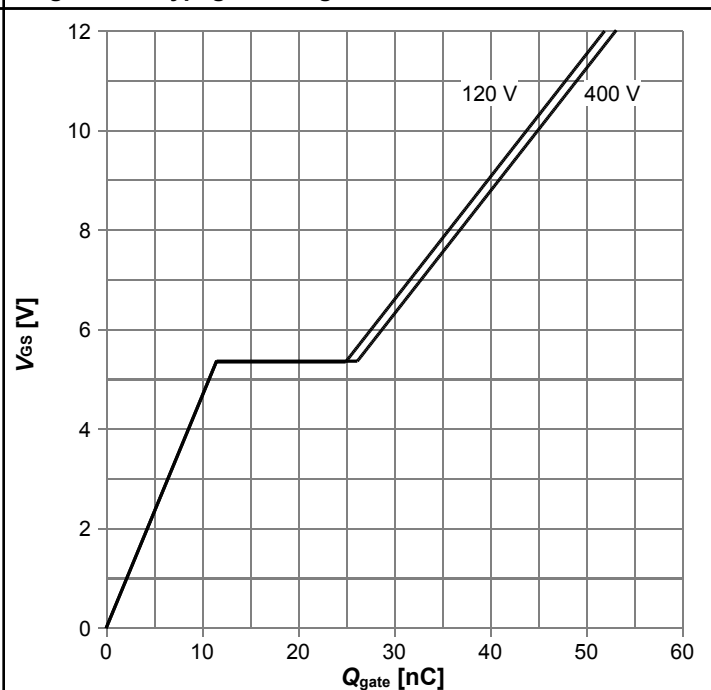

 $V_{GS} = f(Q_{gate}); I_D = 11.8A \text{ pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode

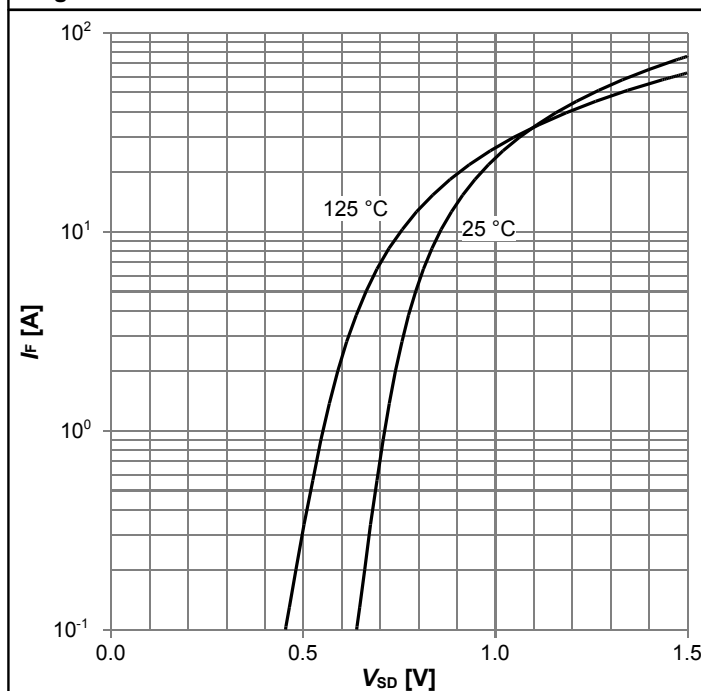

 $I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

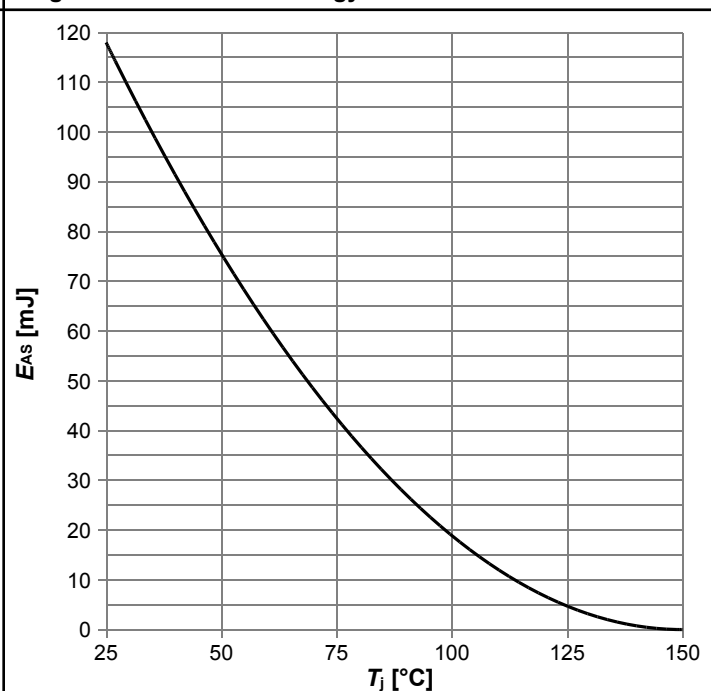
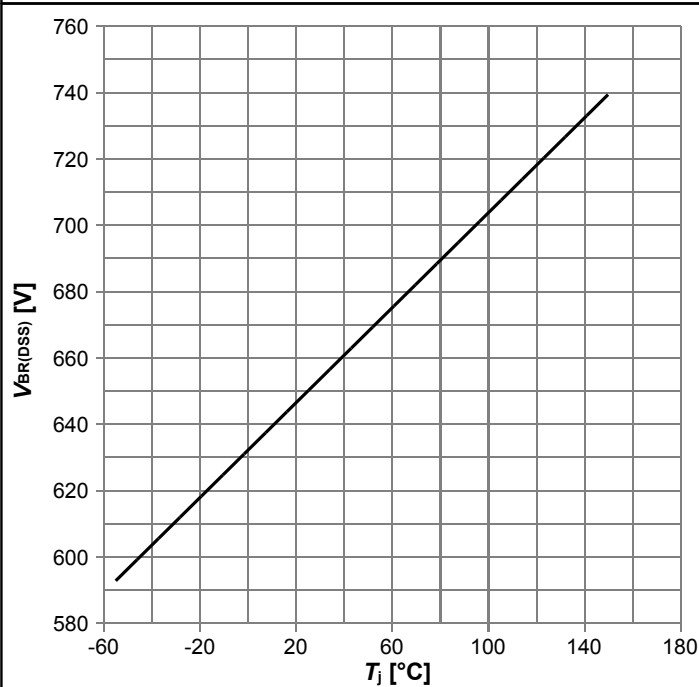
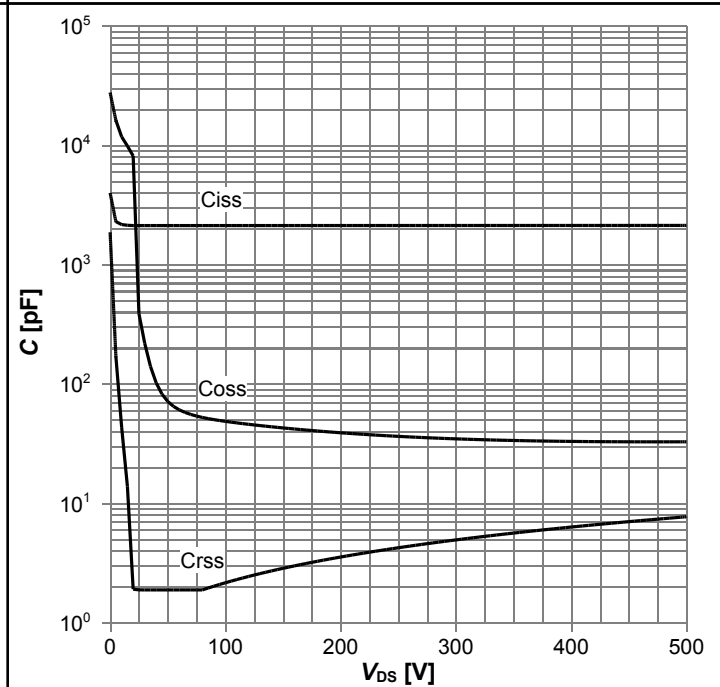

 $E_{AS} = f(T_j); I_D = 8.4 A; V_{DD} = 50 V$

Diagram 13: Drain-source breakdown voltage



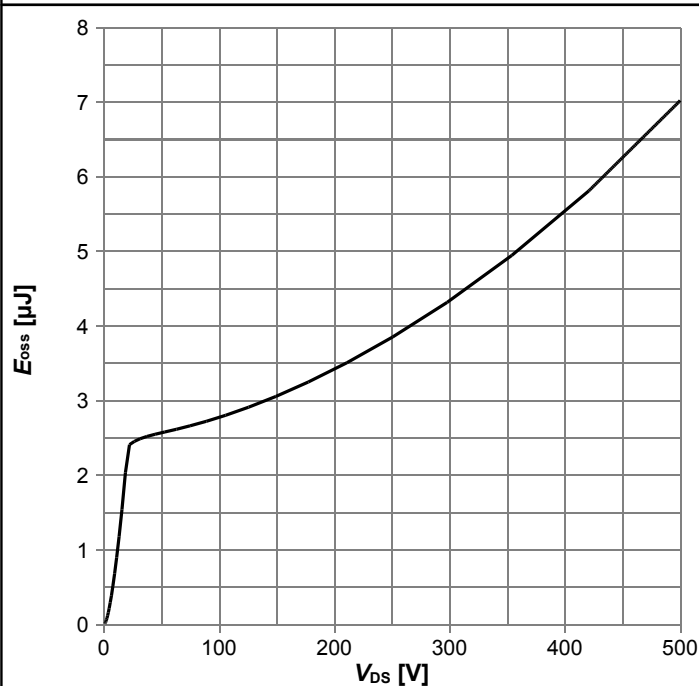
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

The figure consists of two parts:

- Test circuit for diode characteristics:** A schematic diagram showing two identical test circuits connected in parallel. Each circuit includes a pulse voltage source, a gate resistor R_{g1} , a MOSFET, a diode, a drain resistor R_g , a load capacitor, and a DC supply. The output voltage is labeled V_{DS} and the output current is labeled I_F . Below the circuit, it is noted that $R_{g1} = R_g$.
- Diode recovery waveform:** A graph plotting voltage V and current I against time t . It shows the transition from forward conduction at current I_F to reverse blocking at voltage V_{DS} . Key parameters indicated include:
 - t_F : Forward fall time.
 - t_{rr} : Reverse recovery time, which is the sum of storage time t_S and reverse fall time t_r ($t_{rr} = t_r + t_S$).
 - Q_F and Q_S : Forward and storage charges, respectively, shown as shaded areas under the current curve.
 - $Q_{rr} = Q_F + Q_S$: Total reverse recovery charge.
 - The reverse current decays from $-I_{rm}$ towards zero, reaching $10\% I_{rm}$ at the end of t_{rr} .

Table 9 Switching times

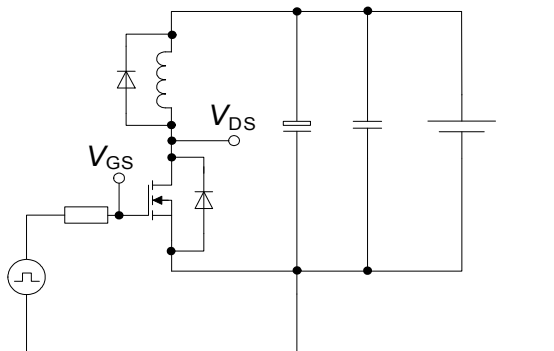
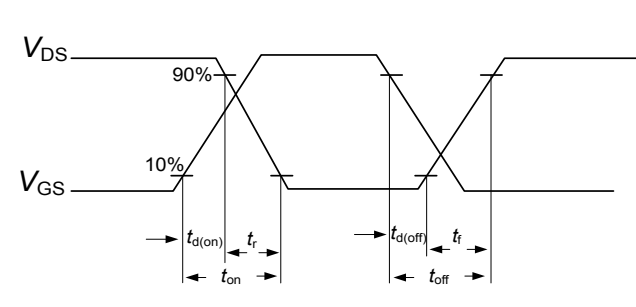
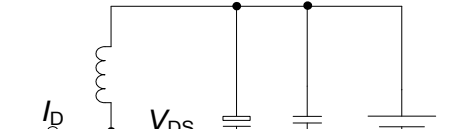
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a switching test setup for an inductive load. A MOSFET is driven by a pulse generator connected to its gate through a resistor. The gate voltage is labeled V_{GS}. The MOSFET's drain is connected to an inductive load (represented by an inductor and a diode in parallel) which is powered by a DC source. The drain-source voltage V_{DS} is measured across the load. The load is connected to ground.	 The timing diagram shows the relationship between the drain-source voltage V_{DS} and the gate-source voltage V_{GS} during switching transitions. The V_{GS} signal is a square wave that transitions between a low level and a high level. The V_{DS} signal shows the resulting voltage across the inductive load. Key time intervals are marked: $t_{d(on)}$: Delay time from the start of the V_{GS} rise to the 10% point of the V_{DS} fall. t_r: Rise time of V_{DS} from 90% to 10% during the V_{GS} fall. t_{on}: Total on-time from the 10% point of V_{DS} fall to the start of the V_{GS} fall. $t_{d(off)}$: Delay time from the start of the V_{GS} rise to the 90% point of the V_{DS} rise. t_f: Fall time of V_{DS} from 90% to 10% during the V_{GS} rise. t_{off}: Total off-time from the 90% point of V_{DS} rise to the start of the V_{GS} rise.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

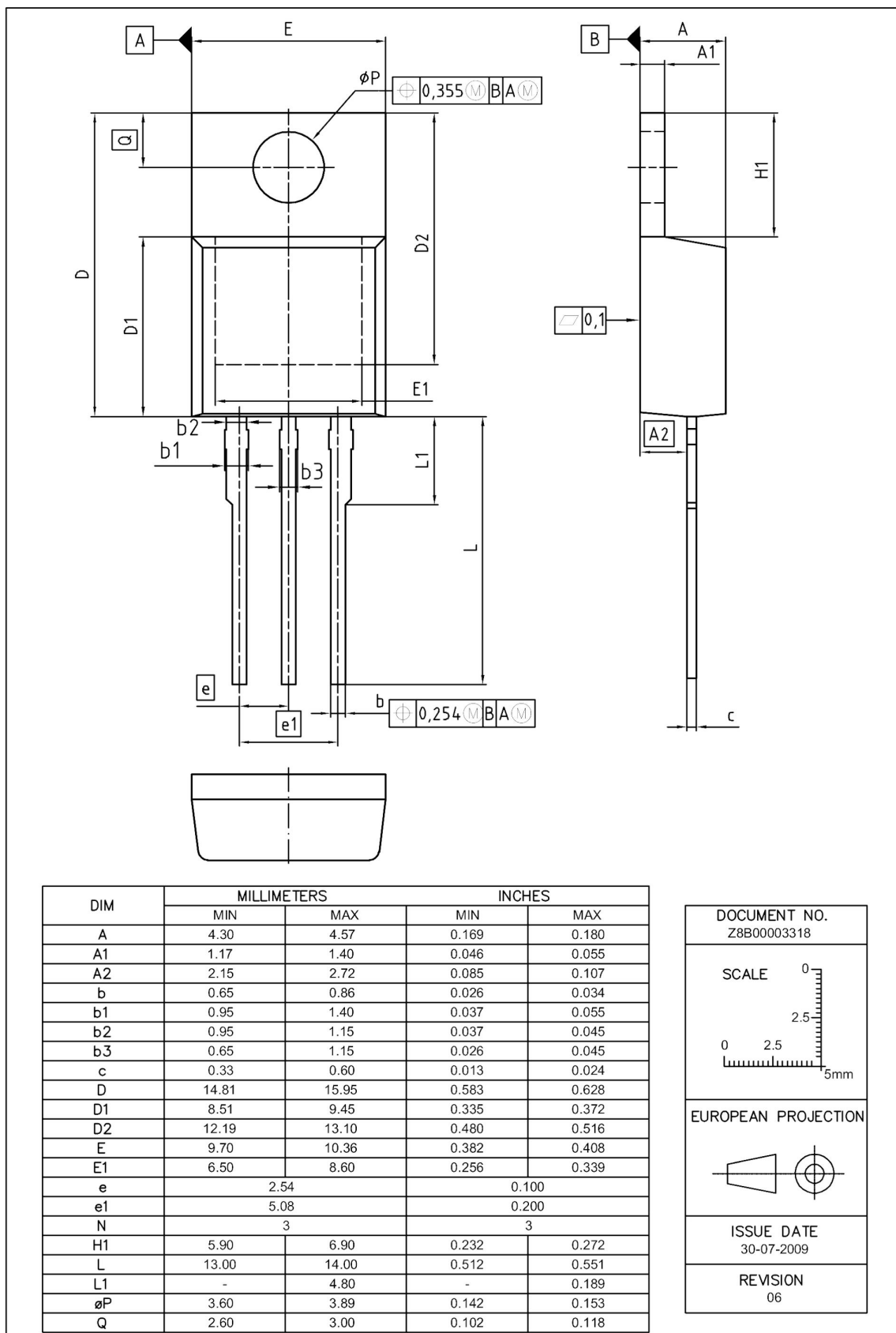


Figure 1 Outline PG-TO 220, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPP65R095C7

Revision: 2013-10-11, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-10-11	Release of final version

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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