

ON Semiconductor®

FSUSB42 — Low-Power, Two-Port, High-Speed, USB2.0 (480Mbps) UART Switch

Features

- Low On Capacitance: 3.7 pF Typical
 Low On Resistance: 3.9 Ω Typical
- Low Pow er Consumption: 1 μA Maximum
 - 15 μA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN} =1.8 V, V_{CC} =4.4 V)
- Wide -3 db Bandwidth: > 720 MHz
- Packaged in:
 - 10-Lead UMLP (1.4 x 1.8 mm)
 - 10-Lead MSOP
- 8 kV ESD Rating, >16 kV Power / GND ESD Rating
- Over-Voltage Tolerance (OVT) on all USB Ports
 Up to 5.25 V without External Components

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSUSB42 is a bi-directional, low-power, two-port, high-speed, USB2.0 switch. Configured as a double-pole, double-throw switch (DPDT) switch, it is optimized for switching between any combination of high-speed (480 Mbps) or Full-Speed (12 Mbps) sources.

The FSUSB42 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.7 pF. The wide bandwidth of this device (720 MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB42 contains special circuitry on the switch VO pins for applications where the Vcc supply is powered-off (Vcc=0 V), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage (Vcc). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general-purpose VOs of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSUSB42UMX	HE	-40 to +85°C	10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8 mm
FSUSB42MUX	FSUSB42	-40 to +85°C	10-Lead, Molded Small-Outline Package (MSOP) JEDEC MO-187, 3.0 mm Wide

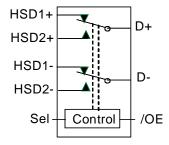
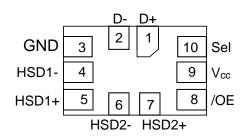


Figure 1. Analog Symbol

Pin Assignments



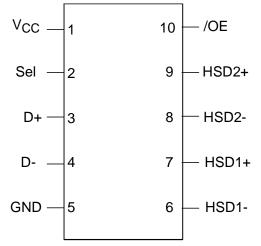


Figure 2. 10-Lead UMLP (Top-Through View)

Figure 3. 10-Lead MSOP (Top-Through View)

Pin Definitions

UMLP Pin#	MSOP Pin#	Name	Description
1	3	D+	Common USB Data Bus
2	4	D-	Common USB Data Bus
3	5	GND	Ground
4	6	HSD1-	Multiplexed Source Input 1
5	7	HSD1+	Multiplexed Source Input 1
6	8	HSD2-	Multiplexed Source Input 2
7	9	HSD2+	Multiplexed Source Input 2
8	10	/OE	Sw itch Enable
9	1	Vcc	Supply Voltage
10	2	Sel	Sw itch Select

Truth Table

SEL	/OE	Function
X	HIGH	Disconnect
LOW	LOW	D+= HSD1+, D-= HSD1-
HIGH	LOW	D+= HSD2+, D-= HSD2-

- Notes: 1. LOW ≤V_{IL}.
- HIGH ≥V_{IH}.
- X=Don't Care.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
Vcc	Supply Voltage		-0.5	5.6	V
VCNTRL	DC Input Voltage (S, /OE) ⁽⁴⁾		-0.5	Vcc	V
Vsw	DC Switch I/O Voltage ⁽⁴⁾ (VCC=0V)		-0.50	5.25	V
lık	DC Input Diode Current		-50		mA
ЮИТ	DC Output Current			100	mA
T _{STG}	Storage Temperature	-65	+150	°C	
MSL	Moisture Sensitivity Level (JEDEC J-STD-020	A)		1	Level
		All Pins	7		
	Human Body Model, JEDEC: JESD22-A114	I/O to GND	8		
		Pow er to GND	16		
ESD		D+/D-	9		kV
	IEC 61000-4-2 System on USB Connector	Air Discharge	15		
	Pins D+ & D-	Contact	8		
	Charged Device Model, JEDEC: JESD22-C101		2		

Note:

4. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage	2.4	4.4	V
VCNTRL	Control Input Voltage (S, /OE) ⁽⁵⁾	0	Vcc	V
V_{SW}	Sw itch I/O Voltage	-0.5	4.5	V
T _A	Operating Temperature	-40	+85	°C

Note:

5. The control input must be held HIGH or LOW and it must not float.

DC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V _{cc} (V)	T _A =- 4	Unit		
Symbol	T didiliotoi		▼CC (▼)	Min.	Тур.	Max.	Oilit
Vıĸ	Clamp Diode Voltage	I _{IN} =-18mA	3.0			-1.2	V
VIH	Input Voltago High		2.4 to 3.6	1.3			V
V IH	Input Voltage High		4.3	1.7			V
VII	Input Voltage Low		2.4 to 3.6			0.5	V
VIL	TPUL VOILAGE LOW	4.3			0.7	V	
I _{IN}	Control Input Leakage	V _{SW} =0 to V _{CC}	0 to 4.3	-1		1	μΑ
loz	Off State Leakage	$\begin{array}{l} 0 \leq Dn, \ HSD1n, \ HSD2n \\ \leq 3.6 \ V \end{array}$	4.3	-2		2	μΑ
loff	Pow er-Off Leakage Current (All VO Ports)	V _{SW} =0 V to 4.3 V, V _{CC} =0 V Figure 5	0	-2		2	μΑ
Ron	HS Switch On Resistance ⁽⁶⁾	V _{SW} =0.4 V, I _{ON} =-8 mA	2.4		4.5	7.5	Ω
NON	The Switch on Nesistance	Figure 4	3.0		3.9	6.5	2.2
ΔR_{ON}	HS Delta R _{ON} ⁽⁷⁾	V _{SW} =0.4 V, I _{ON} =-8 mA	3.0		0.65		Ω
lcc	Quiescent Supply Current	V _{CNTRL} =0 or V _{CC} , l _{OUT} =0	4.3			1	μΑ
loor	Increase in Icc Current per	V _{CNTRL} =2.6 V, V _{CC} =4.3 V	4.3			10	μΑ
Ісст	Control Voltage and V _{CC}	V _{CNTRL} =1.8 V, V _{CC} =4.3 V	4.3			15	μΑ

Notes:

- 6. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
- 7. Guaranteed by characterization.

AC Electrical Characteristics

All typical value are for V_{CC} =3.3 V at T_A =25°C unless otherwise specified.

Symbol	Parameter	Condition	V _{cc} (V)	T _A =- 40°C to +85°C			Unit
Syllibol			V _{CC} (V)	Min.	Тур.	Max.	Oilit
ton	Turn-On Time	R _L =50 Ω , C _L =5 pF, V _{SW} =0.8 V,	2.4		24	40	ns
ION	S, /OE to Output	Figure 6, Figure 7	3.0 to 3.6		13	30	115
toff	Turn-Off Time	R _L =50 Ω , C _L =5 pF, V _{SW} =0.8 V,	2.4		15	35	ns
TOFF	S, /OE to Output	Figure 6, Figure 7	3.0 to 3.6		12	25	118
t _{PD}	Propagation Delay ⁸	C_L =5 pF, R_L =50 Ω , Figure 6, Figure 8	3.3		0.25		ns
t _{BBM}	Break-Before-Make	R _L =50 Ω, C _L =5 pF,	2.4	2.0		10	ns
rbbivi	DI Eak-Dei OI E-IVIAKE	V _{SW1} =V _{SW2} =0.8 V, Figure 10	3.0 to 3.6	2.0		6.5	113
O _{IRR}	Off Isolation	R _L =50 Ω , f=240 MHz, Figure 12	3.0 to 3.6		-30		dB
Xtalk	Non-Adjacent Channel Crosstalk	R _L =50 Ω , f=240 MHz, Figure 13	3.0 to 3.6		-45		dB
BW	-3db Bandwidth	R _L =50 Ω, C _L =0 pF, Figure 11	3.0 to 3.6		720		MHz
DVV	Januw Idili	R _L =50 Ω , C _L =5 pF, Figure 11			550		MHz

Note:

USB High-Speed-Related AC Electrical Characteristics

All typical value are for V_{CC} =3.3 V at T_A =25°C unless otherwise specified.

Symbol	Parameter	Condition	V _{cc} (V)	T _A =- 40°C to +85°C			Unit
	raiametei			Min.	Тур.	Max.	Oiiit
t _{SK(P)}	Skew of Opposite Transitions of the Same Output (9)	$C_L=5$ pF, $R_L=50$ Ω , Figure 9			20		ps
tı	Total Jitter ⁽⁹⁾	R _L =50 Ω, C _L =5 pF, t _R =t _F =500 ps (10-90%) at 480 Mbps (PRBS=2 ¹⁵ – 1)			200		ps

Note:

Capacitance

Symbol	Parameter	Condition	T _A =- 40°C to +85°C			Unit
Symbol	Farailleter	Condition	Min.	Тур.	Max.	Oiiit
C _{IN}	Control Pin Input Capacitance	V _{CC} =0 V		1.5		
Con	D+/D- On Capacitance	V _{CC} =3.3 V,/OE=0 V, f=240 MHz, Figure 15		3.7		pF
Coff	D1n, D2n Off Capacitance	V _{CC} and /OE=3.3 V, Figure 14		2.0		

^{8.} Guaranteed by characterization.

^{9.} Guaranteed by characterization.

Test Diagrams

HSD_n

GND RS

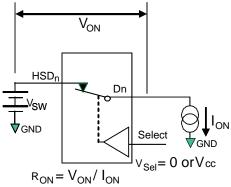


Figure 4. On Resistance



 R_L , R_S , and C_L are functions of the application environment (see AC Tables for specific values) C_L includes test fixture and stray capacitance.

Dn

Figure 6. AC Test Circuit Load

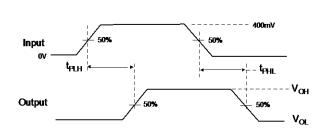
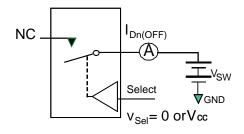


Figure 8. Propagation Delay (t_Rt_F - 500 ps)



**Each switch port is tested separately

Figure 5. Off Leakage

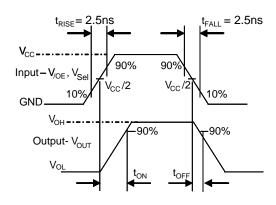


Figure 7. Turn-On / Turn-Off Waveforms

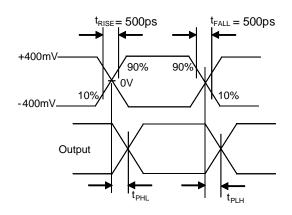


Figure 9. Intra-Pair Skew Test t_{SK(P)}

Test Diagrams (Continued)

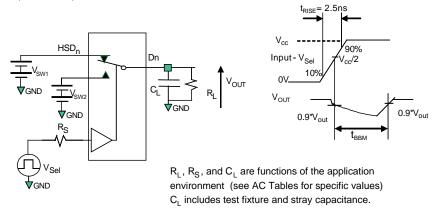


Figure 10. Break-Before-Make Interval Timing

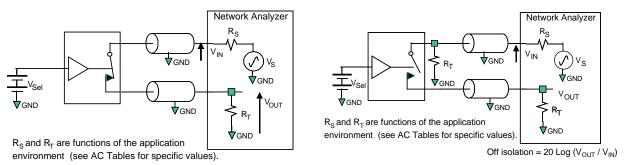


Figure 11. Bandwidth

Figure 12. Channel Off Isolation

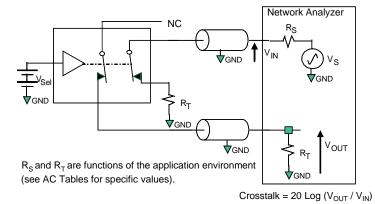
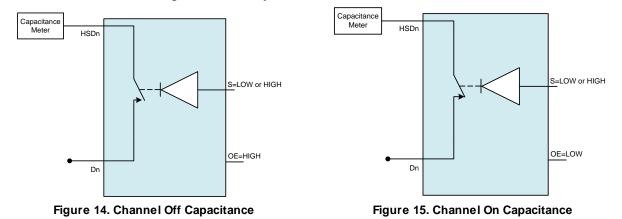
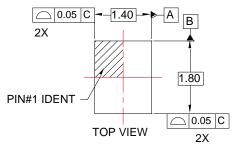
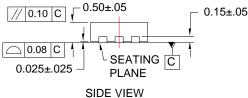


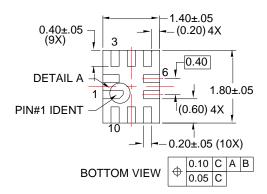
Figure 13. Non-Adjacent Channel-to-Channel Crosstalk

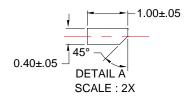


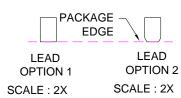
Physical Dimensions

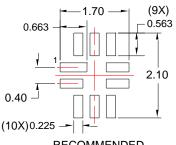




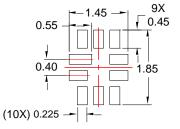








RECOMMENDED LAND PATTERN



OPTIONAL MINIMIAL TOE LAND PATTERN

NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-UMLP10Arev6.

Figure 16. 10-Lead, Ultrathin Molded Leadless Package (UMLP)

Physical Dimensions (Continued) 3.00±0.10 Α В (0.30) -2.45 4.90 3.00±0.10 PIN#1 ID QUADRANT Ħ 0.50 (0.381) TOP VIEW 0.85±0.10 1.10 MAX 0.15 0.00 Ċ **END VIEW** ○ 0.10 C 0.08 ALL LEAD TIPS .08 M A B C 12° TOP & BOTTOM SIDE VIEW GAUGE **R0.13 TYP** SEATING 4°-8 PLANE NOTES: UNLESS OTHERWISE SPECIFIED 0.80 0.40 0.22 THIS PACKAGE CONFORMS TO JEDEC MO-187 VARIATION BA. B. ALL DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES AS PER ASME 🕶 (0.95) 🖛 DETAIL A SCALE 20 : 1 Y14.5-1994. E. LAND PATTERN AS PER IPC7351#SOP50P490X110-10AN F. FILE NAME: MKT-MUA10AREV3

Figure 17. 10-Lead, Molded Small Outline Package (MSOP)

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