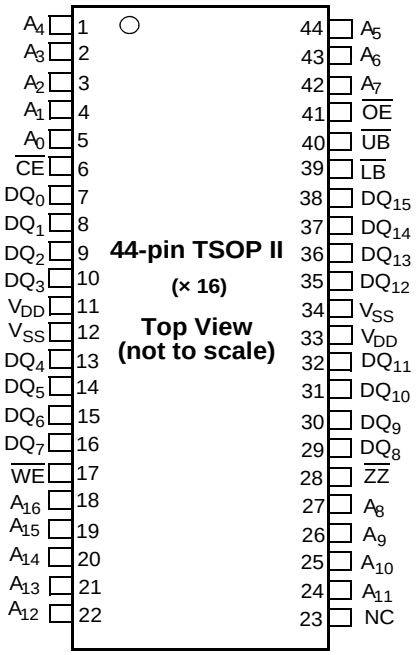
Contents

Pinout

Figure 1. 44-pin TSOP II pinout



Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{16}	Input	**Address inputs**: The 17 address lines select one of 128K words in the F-RAM array. The lowest two address lines A_1–A_0 may be used for page mode read and write operations.
DQ_0–DQ_{15}	Input/Output	**Data I/O Lines**: 16-bit bidirectional data bus for accessing the F-RAM array.
$\overline{WE}$	Input	**Write Enable**: A write cycle begins when $\overline{WE}$ is asserted. The rising edge causes the FM28V202 to write the data on the DQ bus to the F-RAM array. The falling edge of $\overline{WE}$ latches a new column address for page mode write cycles.
$\overline{CE}$	Input	**Chip Enable**: The device is selected and a new memory access begins on the falling edge of $\overline{CE}$. The entire address is latched internally at this point. Subsequent changes to the A_1–A_0 address inputs allow page mode operation.
$\overline{OE}$	Input	**Output Enable**: When $\overline{OE}$ is LOW, the FM28V202 drives the data bus when the valid read data is available. Deasserting $\overline{OE}$ HIGH tristates the DQ pins.
$\overline{UB}$	Input	**Upper Byte Select**: Enables DQ_{15}–DQ_8 pins during reads and writes. These pins are HI-Z if $\overline{UB}$ is HIGH. If the user does not perform byte writes and the device is not configured as a 256K × 8, the $\overline{UB}$ and $\overline{LB}$ pins may be tied to ground.
$\overline{LB}$	Input	**Lower Byte Select**: Enables DQ_7–DQ_0 pins during reads and writes. These pins are HI-Z if $\overline{LB}$ is HIGH. If the user does not perform byte writes and the device is not configured as a 256 K × 8, the $\overline{UB}$ and $\overline{LB}$ pins may be tied to ground.
$\overline{ZZ}$	Input	**Sleep**: When $\overline{ZZ}$ is LOW, the device enters a low-power sleep mode for the lowest supply current condition. $\overline{ZZ}$ must be HIGH for a normal read/write operation. The $\overline{ZZ}$ pin is internally pulled up.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply inputs to the device.
NC	No connect	No connect. This pin is not connected to the die.

Device Operation

The FM28V202 is a wordwide F-RAM memory logically organized as 131,072 × 16 and accessed using an industry-standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation, which provides high-speed access to addresses within a page (row). Access to a different page requires that either $\overline{CE}$ transitions LOW or the upper address (A_{16}–A_2) changes. See the Functional Truth Table on page 17 for a complete description of read and write modes.

Memory Operation

Users access 131,072 memory locations, each with 16 data bits through a parallel interface. The F-RAM array is organized as eight blocks, each having 4096 rows. Each row has four column locations, which allow fast access in page mode operation. When an initial address is latched by the falling edge of $\overline{CE}$, subsequent column locations may be accessed without the need to toggle $\overline{CE}$. When $\overline{CE}$ is deasserted HIGH, a pre-charge operation begins. Writes occur immediately at the end of the access with no delay. The $\overline{WE}$ pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay writes.

Read Operation

A read operation begins on the falling edge of $\overline{CE}$. The falling edge of $\overline{CE}$ causes the address to be latched and starts a memory read cycle if $\overline{WE}$ is HIGH. Data becomes available on the bus after the access time is met. When the address is latched and the access completed, a new access to a random location (different row) may begin while $\overline{CE}$ is still LOW. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM28V202's $\overline{CE}$-initiated access time is faster than the address access time.

The FM28V202 will drive the data bus when $\overline{OE}$ and at least one of the byte enables ($\overline{UB}$, $\overline{LB}$) is asserted LOW. The upper data byte is driven when $\overline{UB}$ is LOW, and the lower data byte is driven when $\overline{LB}$ is LOW. If $\overline{OE}$ is asserted after the memory access time is met, the data bus will be driven with valid data. If $\overline{OE}$ is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven to the bus. When $\overline{OE}$ is deasserted HIGH, the data bus will remain in a HI-Z state.

Write Operation

In the FM28V202, writes occur in the same interval as reads. The FM28V202 supports both $\overline{CE}$- and $\overline{WE}$-controlled write cycles. In both cases, the address A_{16}–A_2 is latched on the falling edge of $\overline{CE}$.

In a $\overline{CE}$-controlled write, the $\overline{WE}$ signal is asserted before beginning the memory cycle. That is, $\overline{WE}$ is LOW when $\overline{CE}$ falls. In this case, the device begins the memory cycle as a write. The FM28V202 will not drive the data bus regardless of the state of $\overline{OE}$ as long as $\overline{WE}$ is LOW. Input data must be valid when $\overline{CE}$ is deasserted HIGH. In a $\overline{WE}$-controlled write, the memory cycle begins on the falling edge of $\overline{CE}$. The $\overline{WE}$ signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if $\overline{OE}$ is LOW; however, it will be HI-Z when $\overline{WE}$ is asserted LOW. The $\overline{CE}$- and $\overline{WE}$-controlled write timing cases are shown in the Switching Waveforms on page 13.

Write access to the array begins on the falling edge of $\overline{WE}$ after the memory cycle is initiated. The write access terminates on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting $\overline{WE}$ or $\overline{CE}$. The data setup time indicates the interval during which data cannot change before the end of the write access (rising edge of $\overline{WE}$ or $\overline{CE}$).

Unlike other nonvolatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The F-RAM array is organized as eight blocks, each having 4096 rows. Each row has four column-address locations. Address inputs A_1–A_0 define the column address to be accessed. An access can start on any column address, and other column locations may be accessed without the need to toggle the $\overline{CE}$ pin. For fast access reads, after the first data byte is driven to the bus, the column address inputs A_1–A_0 may be changed to a new value. A new data byte is then driven to the DQ pins no later than t_{AAP}, which is less than half the initial read access time. For fast access writes, the first write pulse defines the first write access. While $\overline{CE}$ is LOW, a subsequent write pulse along with a new column address provides a page mode write access.

Pre-charge Operation

The pre-charge operation is an internal condition in which the memory state is prepared for a new access. Pre-charge is user-initiated by driving the $\overline{CE}$ signal HIGH. It must remain HIGH for at least the minimum pre-charge time, t_{PC}.

Pre-charge is also activated by changing the upper addresses, A_{16}–A_2. The current row is first closed before accessing the new row. The device automatically detects an upper order address change, which starts a pre-charge operation. The new address is latched and the new read data is valid within the t_{AA} address access time; see Figure 8 on page 13. A similar sequence occurs for write cycles; see Figure 13 on page 14. The rate at which random addresses can be issued is t_{RC} and t_{WC}, respectively.

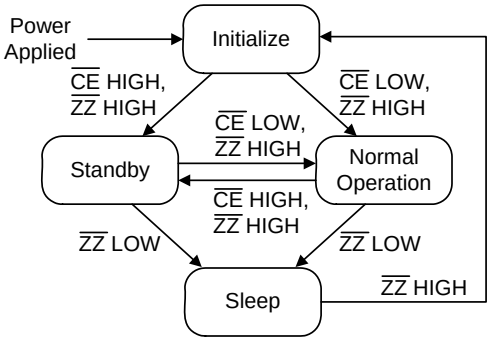
Sleep Mode

The device incorporates a sleep mode of operation, which allows the user to achieve the lowest power supply current condition. It enters a low-power sleep mode by asserting the $\overline{ZZ}$ pin LOW. Read and write operations must complete before the $\overline{ZZ}$ pin going LOW. When $\overline{ZZ}$ is LOW, all pins are ignored except the $\overline{ZZ}$

pin. When $\overline{ZZ}$ is deasserted HIGH, there is some time delay (t_{ZZEX}) before the user can access the device.

If sleep mode is not used, the $\overline{ZZ}$ pin may be floated (internal pull-up) or tied to V_{DD}.

Figure 2. Sleep/Standby State Diagram



Software Write Protect

The 128 K × 16 address space is divided into eight sectors (blocks) of 16 K × 16 each. Each sector can be individually software write-protected and the settings are nonvolatile. A unique address and command sequence invokes the write-protect mode.

To modify write protection, the system host must issue six read commands, three write commands, and a final read command. The specific sequence of read addresses must be provided to access the write-protect mode. Following the read address sequence, the host must write a data byte that specifies the desired protection state of each sector. For confirmation, the system must then write the complement of the protection byte immediately after the protection byte. Any error that occurs including read addresses in the wrong order, issuing a seventh read address, or failing to complement the protection value will leave the write protection unchanged.

The write-protect state machine monitors all addresses, taking no action until this particular read/write sequence occurs. During the address sequence, each read will occur as a valid operation and data from the corresponding addresses will be driven to the data bus. Any address that occurs out of sequence will cause the software protection state machine to start over. After the address sequence is completed, the next operation must be a write cycle. The lower data byte contains the write-protect settings. This value will not be written to the memory array, so the address is a don't-care. Rather it will be held pending the next cycle, which must be a write of the data complement to the protection settings. If the complement is correct, the write-protect settings will be adjusted. Otherwise, the process is aborted and the address sequence starts over. The data value written after the correct six addresses will not be entered into the memory.

The protection data byte consists of eight bits, each associated with the write-protect state of a sector. The data byte must be driven to the lower eight bits of the data bus, DQ_7–DQ_0. Setting a bit to ‘1’ write-protects the corresponding sector; a 0 enables writes for that sector. The following table shows the write-protect sectors with the corresponding bit that controls the write-protect setting.

Table 1. Write Protect Sectors - 16K x 16 Blocks

Sectors	Blocks
Sector 7	1FFFFh–1C000h
Sector 6	1BFFFh–18000h
Sector 5	17FFFh–14000h
Sector 4	13FFFh–10000h
Sector 3	0FFFFh–0C000h
Sector 2	0BFFFh–08000h
Sector 1	07FFFh–04000h
Sector 0	03FFFh–00000h

The write-protect address sequence follows:

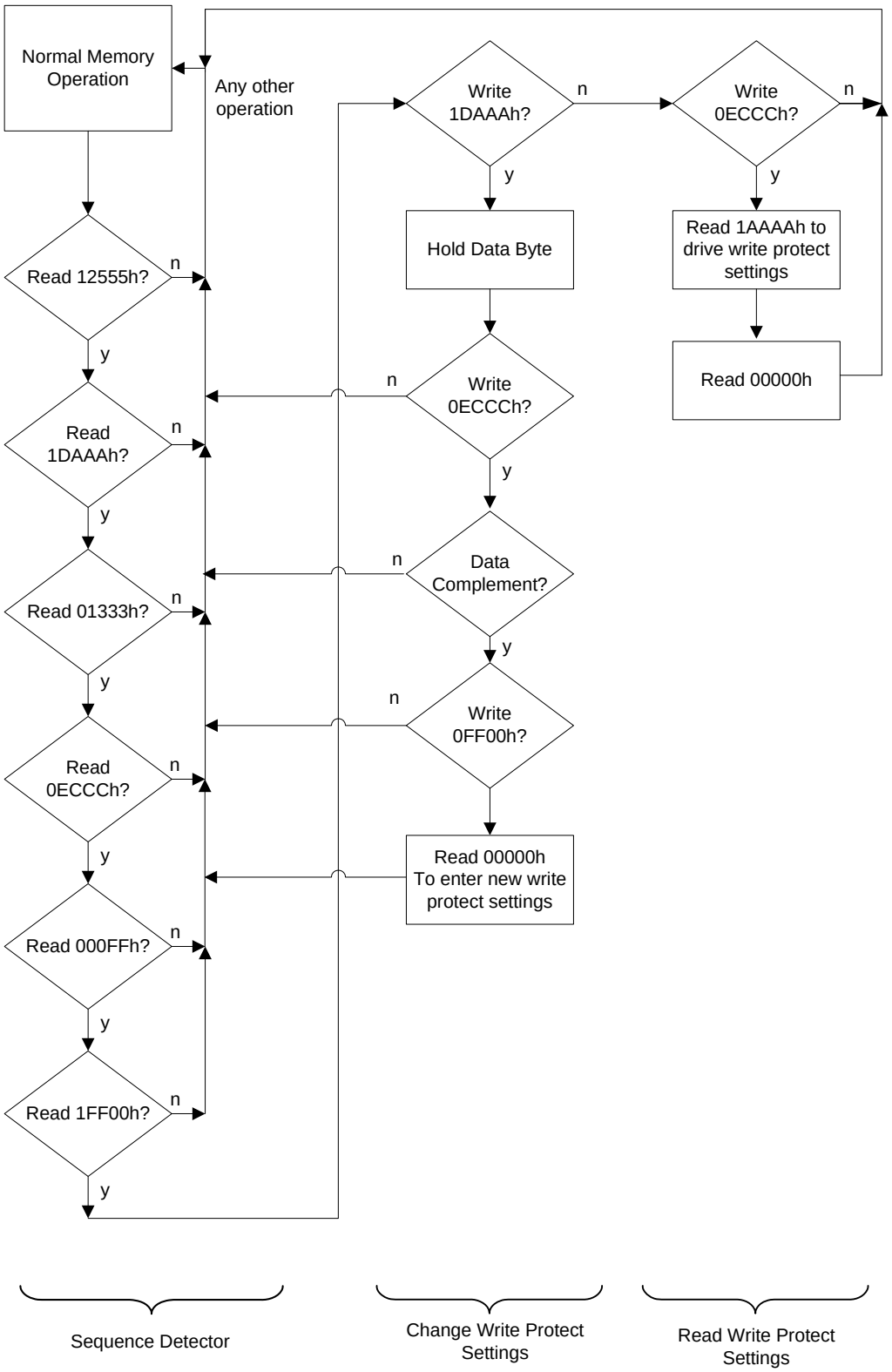
1. Read address 12555h
2. Read address 1DAAAh
3. Read address 01333h
4. Read address 0ECCCh
5. Read address 000FFh
6. Read address 1FF00h
7. Write address 1DAAAh
8. Write address 0ECCCh
9. Write address 0FF00h
10. Read address 00000h

The address sequence provides a secure way of modifying the protection. The write-protect sequence has a one in 3×10^{32} chance of randomly accessing exactly the first six addresses. The odds are further reduced by requiring three more write cycles, one that requires an exact inversion of the data byte. Figure 3 on page 6 shows a flow chart of the entire write-protect operation. The write-protect settings are nonvolatile. The factory default: all blocks are unprotected.

For example, the following sequence write-protects addresses from 0C000h to 13FFFh (sectors 3 and 4):

	Address	Data
Read	12555h	–
Read	1DAAAh	–
Read	01333h	–
Read	0ECCCh	–
Read	000FFh	–
Read	1FF00h	–
Write	1DAAAh	18h; bits 3 and 4 = 1
Write	0ECCCh	E7h; complement of 18h
Write	0FF00h	Don’t care
Read	00000h	

Figure 3. Write-Protect State Machine



Software Write-Protect Timing

Figure 4. Sequence to Set Write-Protect Blocks [1]

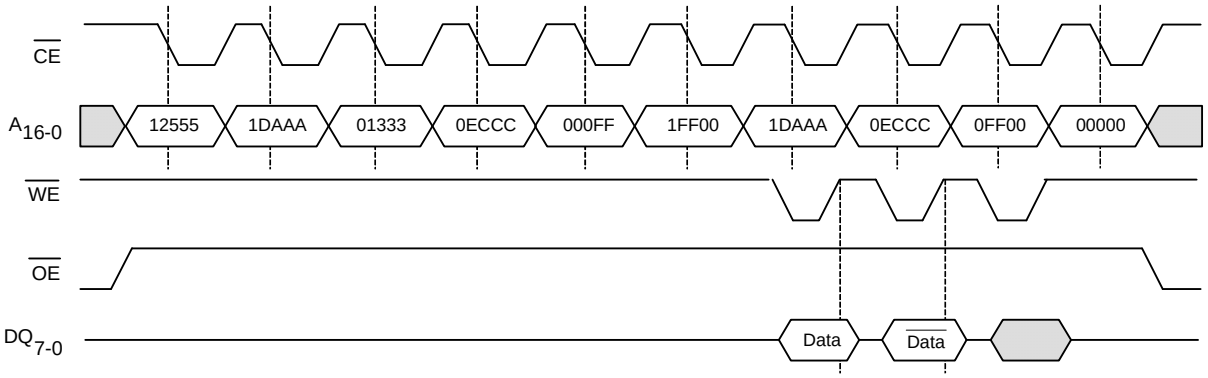
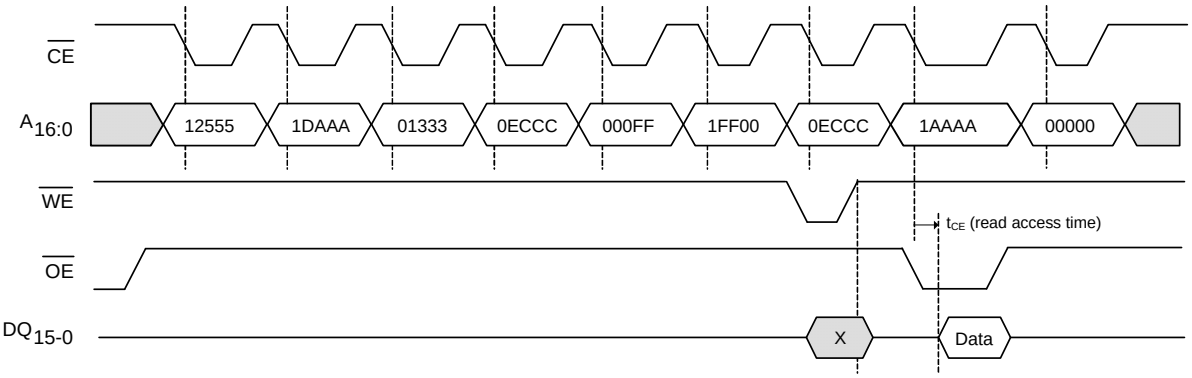


Figure 5. Sequence to Read Write-Protect Settings [1]

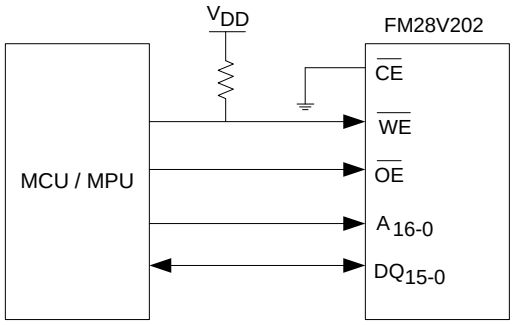


Note
1. This sequence requires $t_{AS} \geq 10$ ns and address must be stable while $\overline{CE}$ is LOW.

SRAM Drop-In Replacement

The FM28V202 is designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require $\overline{CE}$ to toggle for each new address. $\overline{CE}$ may remain LOW indefinitely. While $\overline{CE}$ is LOW, the device automatically detects address changes and a new access begins. This functionality allows $\overline{CE}$ to be grounded, similar to an SRAM. It also allows page mode operation at speeds up to 33 MHz. Note that if $\overline{CE}$ is tied to ground, the user must be sure $\overline{WE}$ is not LOW at power-up or power-down events. If $\overline{CE}$ and $\overline{WE}$ are both LOW during power cycles, data will be corrupted. Figure 6 shows a pull-up resistor on $\overline{WE}$, which will keep the pin HIGH during power cycles, assuming the MCU/MPU pin tristates during the reset condition.The pull-up resistor value should be chosen to ensure the $\overline{WE}$ pin tracks V_{DD} to a high enough value, so that the current drawn when $\overline{WE}$ is LOW is not an issue. A 10-kΩ resistor draws 330 µA when $\overline{WE}$ is LOW and V_{DD} = 3.3 V. Note that software write-protect is not available if the chip enable pin is hard-wired.

Figure 6. Use of Pull-up Resistor on $\overline{WE}$

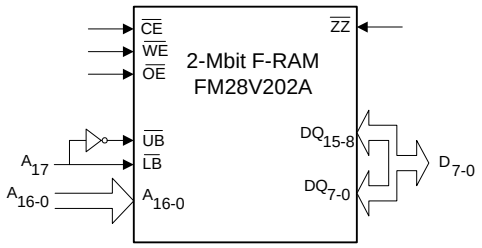


For applications that require the lowest power consumption, the $\overline{CE}$ signal should be active (LOW) only during memory accesses. The FM28V202 draws supply current while $\overline{CE}$ is LOW, even if addresses and control signals are static. While $\overline{CE}$ is HIGH, the device draws no more than the maximum standby current, I_{SB}.

The FM28V202 is backward compatible with the 2-Mbit FM21L16 device. There are some differences in the timing specifications. Refer to the FM21L16 datasheet.

The $\overline{UB}$ and $\overline{LB}$ byte select pins are active for both read and write cycles. They may be used to allow the device to be wired as a 256K × 8 memory. The upper and lower data bytes can be tied together and controlled with the byte selects. Individual byte enables or the next higher address line A_{17} may be available from the system processor.

Figure 7. FM28V202 Wired as 256 K x 8



Endurance

The FM28V202 is capable of being accessed at least 10^{14} times – reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A_{16-2} and column addresses by A_{1-0}. The array is organized as 32K rows of four words each. The entire row is internally accessed once whether a single 16-bit word or all four words are read or written. Each word in the row is counted only once in an endurance calculation.

The user may choose to write CPU instructions and run them from a certain address space. Table 2 shows endurance calculations for a 256-byte repeating loop, which includes a starting address, three-page mode accesses, and a $\overline{CE}$ pre-charge. The number of bus clock cycles needed to complete a four-word transaction is 4 + 1 at lower bus speeds, but 5 + 2 at 33 MHz due to initial read latency and an extra clock cycle to satisfy the device's pre-charge timing constraint t_{PC}. The entire loop causes each byte to experience only one endurance cycle. The F-RAM read and write endurance is virtually unlimited even at a 33-MHz system bus clock rate.

Table 2. Time to Reach 100 Trillion Cycles for Repeating 256-byte Loop

Bus Freq (MHz)	Bus Cycle Time (ns)	256-byte Transaction Time (µs)	Endurance Cycles/sec	Endurance Cycles/year	Years to Reach 10^{14} Cycles
33	30	10.56	94,690	2.98×10^{12}	33.5
25	40	12.8	78,125	2.46×10^{12}	40.6
10	100	28.8	34,720	1.09×10^{12}	91.7
5	200	57.6	17,360	5.47×10^{11}	182.8

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Maximum junction temperature ..... 95 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to + 4.5 V

Voltage applied to outputs in High Z state .....–0.5 V to V_{DD}+ 0.5 V

Input voltage ..... –1.0 V to + 4.5 V and $V_{IN} < V_{DD}$ + 1.0 V

Transient voltage (< 20 ns) on any pin to ground potential .....–2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount Pb soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Static discharge voltage

Human Body Model (AEC-Q100-002 Rev. E) ..... 4 kV

Charged Device Model (AEC-Q100-011 Rev. B) .. 1.25 kV

Machine Model (AEC-Q100-003 Rev. E) ..... 250 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Industrial	–40 °C to +85 °C	2.0 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2]	Max	Unit
V_{DD}	Power supply voltage			2.0	3.3	3.6	V
I_{DD}	V_{DD} supply current	V_{DD} = 3.6 V, $\overline{CE}$ cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or V_{DD} – 0.2 V), all DQ pins unloaded.		–	7	12	mA
I_{SB}	Sleep mode current	V_{DD} = 3.6 V, $\overline{CE}$ at V_{DD}, All other pins are static and at CMOS levels (0.2 V or V_{DD} – 0.2 V), $\overline{ZZ}$ is HIGH	At T_A = 25 °C	–	120	150	µA
			At T_A = 85 °C	–	–	250	µA
I_{ZZ}	Standby current	V_{DD} = 3.6 V, $\overline{ZZ}$ is LOW, all other inputs at CMOS levels (0.2 V or V_{DD} – 0.2 V).	At T_A = 25 °C	–	3	5	µA
			At T_A = 85 °C	–	–	8	µA
I_{LI}	Input leakage current	V_{IN} between V_{DD} and V_{SS}		–	–	±1	µA
I_{LO}	Output leakage current	V_{OUT} between V_{DD} and V_{SS}		–	–	±1	µA
V_{IH1}	Input HIGH voltage	V_{DD} = 2.7 V to 3.6 V		2.2	–	V_{DD} + 0.3	V
V_{IH2}	Input HIGH voltage	V_{DD} = 2.0 V to 2.7 V		0.7 × V_{DD}	–	–	V
V_{IL1}	Input LOW voltage	V_{DD} = 2.7 V to 3.6 V		– 0.3	–	0.8	V
V_{IL2}	Input LOW voltage	V_{DD} = 2.0 V to 2.7 V		– 0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} > 2.7 V		2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA		V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} > 2.7 V		–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	0.2	V
R_{IN}[3]	Input resistance ($\overline{ZZ}$ pin)	For V_{IN} = V_{IH} (min)		40	–	–	kΩ
		For V_{IN} = V_{IL} (max)		1	–	–	MΩ

Notes

2. Typical values are at 25 °C, V_{DD} = V_{DD} (typ). Not 100% tested.
3. The input pull-up circuit is strong (> 40 kΩ) when the input voltage is above V_{IH} and weak (>1 MΩ) when the input voltage is below V_{IL}.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	At +85 °C	10	–	Years
		At +75 °C	38	–	
		At +65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

Parameter	Description	Test Conditions	Max	Unit
$C_{I/O}$	Input/Output capacitance (DQ)	T_A = 25 °C, f = 1 MHz, V_{DD} = $V_{DD(Typ)}$	8	pF
C_{IN}	Input capacitance		6	pF
C_{ZZ}	Input capacitance of $\overline{ZZ}$ pin		8	pF

Thermal Resistance

Parameter	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	107	°C/W
Θ_{JC}	Thermal resistance (junction to case)		25	°C/W

AC Test Conditions

Input pulse levels .....0 V to 3 V

Input rise and fall times (10%–90%) ..... ≤ 3 ns

Input and output timing reference levels ..... 1.5 V

Output load capacitance..... 30 pF

AC Switching Characteristics

Over the Operating Range

Parameters [4]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{CE}	t_{ACE}	Chip enable access time	–	70	–	60	ns
t_{RC}	–	Read cycle time	105	–	90	–	ns
t_{AA}	–	Address access time	–	105	–	90	ns
t_{OH}	t_{OHA}	Output hold time	20	–	20	–	ns
t_{AAP}	–	Page mode address access time	–	40	–	30	ns
t_{OHP}	–	Page mode output hold time	3	–	3	–	ns
t_{CA}	–	Chip enable active time	70	–	60	–	ns
t_{PC}	–	Pre-charge time	35	–	30	–	ns
t_{BA}	t_{BW}	$\overline{UB}$, $\overline{LB}$ access time	–	25	–	15	ns
t_{AS}	t_{SA}	Address setup time (to $\overline{CE}$ LOW)	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time ($\overline{CE}$ Controlled)	70	–	60	–	ns
t_{OE}	t_{DOE}	Output enable access time	–	25	–	15	ns
t_{HZ}[5, 6]	t_{HZCE}	Chip Enable to output HI-Z	–	15	–	10	ns
t_{OHZ}[5, 6]	t_{HZOE}	Output enable HIGH to output HI-Z	–	15	–	10	ns
t_{BHZ}[5, 6]	t_{HZBE}	$\overline{UB}$, $\overline{LB}$ HIGHHIGH to output HI-Z	–	15	–	10	ns

Notes
4. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 0 to 3 V, output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in AC Test Conditions on page 10.
5. t_{HZ}, t_{OHZ} and t_{BHZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
6. This parameter is characterized but not 100% tested.

AC Switching Characteristics (continued)

Over the Operating Range

Parameters [4]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	105	–	90	–	ns
t_{CA}	–	Chip enable active time	70	–	60	–	ns
t_{CW}	t_{SCE}	Chip enable to write enable HIGH	70	–	60	–	ns
t_{PC}	–	Pre-charge time	35	–	30	–	ns
t_{PWC}	–	Page mode write enable cycle time	40	–	30	–	ns
t_{WP}	t_{PWE}	Write enable pulse width	22	–	18	–	ns
t_{WP2}	t_{BW}	$\overline{UB}$, $\overline{LB}$ pulse width	22	–	18	–	ns
t_{WP3}	t_{PWE}	$\overline{WE}$ LOW to $\overline{UB}$, $\overline{LB}$ HIGH	22	–	18	–	ns
t_{AS}	t_{SA}	Address setup time (to $\overline{CE}$ LOW)	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time ($\overline{CE}$ Controlled)	70	–	60	–	ns
t_{ASP}	–	Page mode address setup time (to $\overline{WE}$ LOW)	8	–	5	–	ns
t_{AHP}	–	Page mode address hold time (to $\overline{WE}$ LOW)	20	–	15	–	ns
t_{WLC}	t_{PWE}	Write enable LOW to chip disabled	30	–	25	–	ns
t_{BLC}	t_{BW}	$\overline{UB}$, $\overline{LB}$ LOW to chip disabled	30	–	25	–	ns
t_{WLA}	–	Write enable LOW to A_{16-2} change	30	–	25	–	ns
t_{AWH}	–	A_{16-2} change to write enable HIGH	105	–	90	–	ns
t_{DS}	t_{SD}	Data input setup time	20	–	15	–	ns
t_{DH}	t_{HD}	Data input hold time	0	–	0	–	ns
t_{WZ}[7, 8]	t_{HZWE}	Write enable LOW to output HI-Z	–	10	–	10	ns
t_{WX}[8]	–	Write enable HIGH to output driven	8	–	5	–	ns
t_{BDS}	–	Byte disable setup time (to $\overline{WE}$ LOW)	8	–	5	–	ns
t_{BDH}	–	Byte disable hold time (to $\overline{WE}$ HIGH)	8	–	5	–	ns

Notes
7. t_{WZ} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
8. This parameter is characterized but not 100% tested.

Switching Waveforms

Figure 8. Read Cycle Timing 1 ($\overline{CE}$ LOW, $\overline{OE}$ LOW)

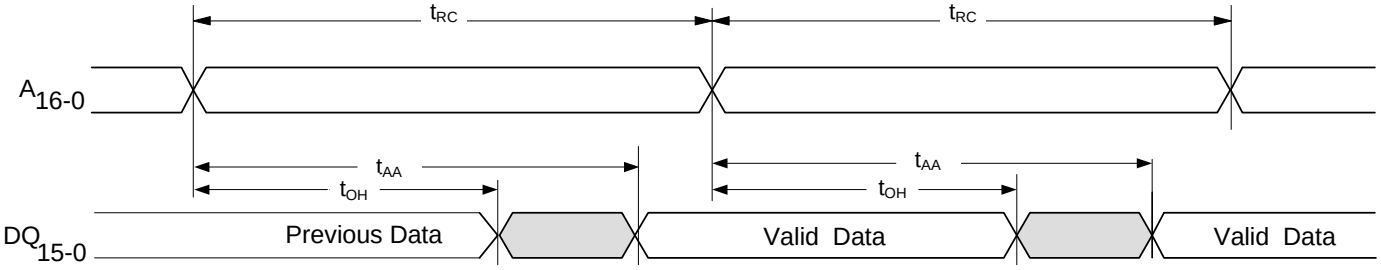


Figure 9. Read Cycle Timing 2 ($\overline{CE}$ Controlled)

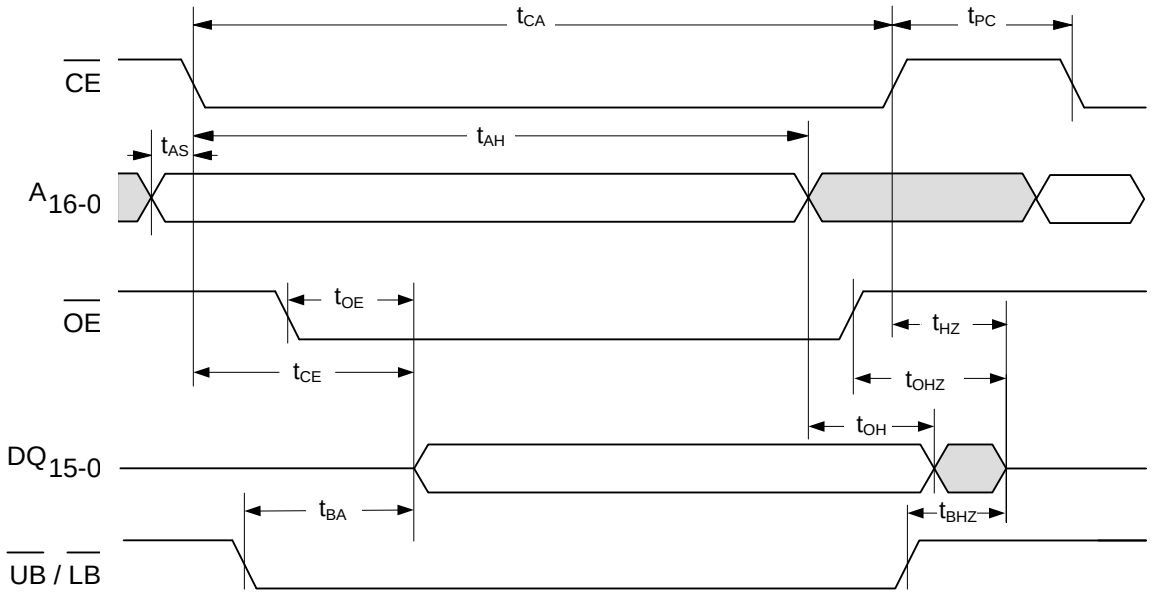
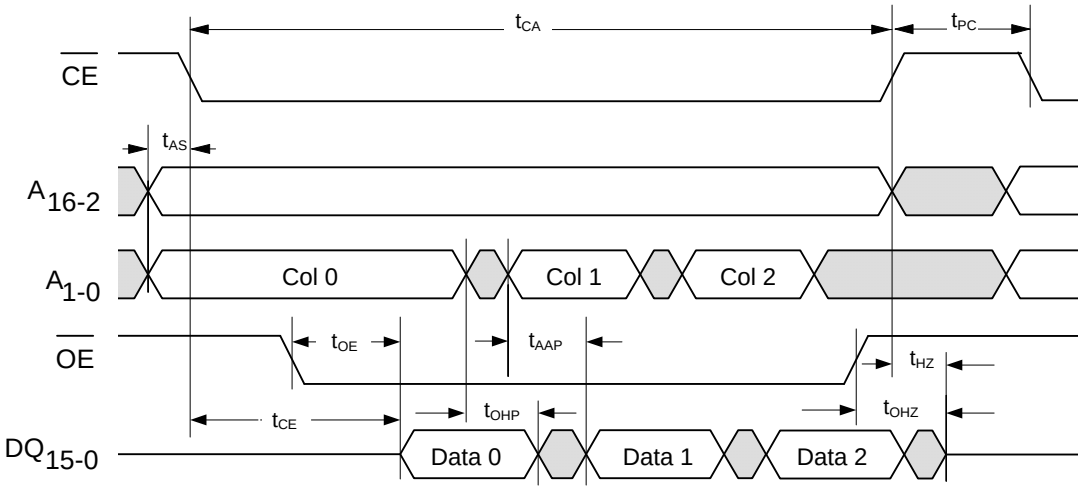


Figure 10. Page Mode Read Cycle Timing [9]



Note
9. Although sequential column addressing is shown, it is not required

Switching Waveforms (continued)

Figure 11. Write Cycle Timing 1 ($\overline{WE}$ Controlled) [10]

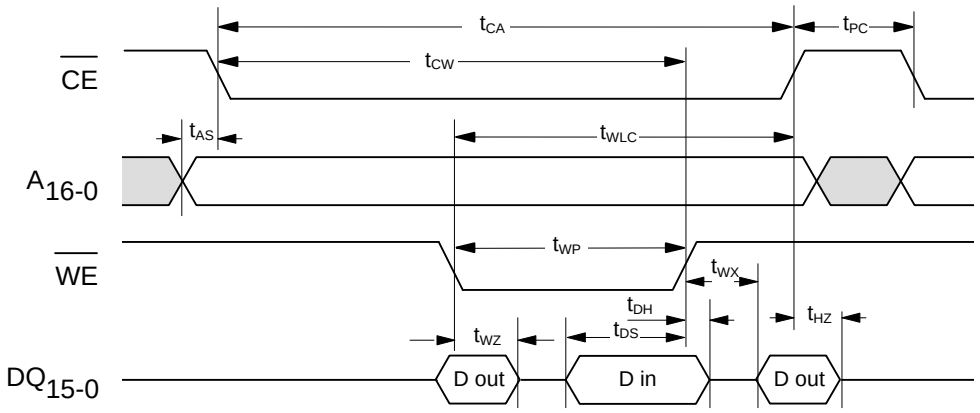


Figure 12. Write Cycle Timing 2 ($\overline{CE}$ Controlled)

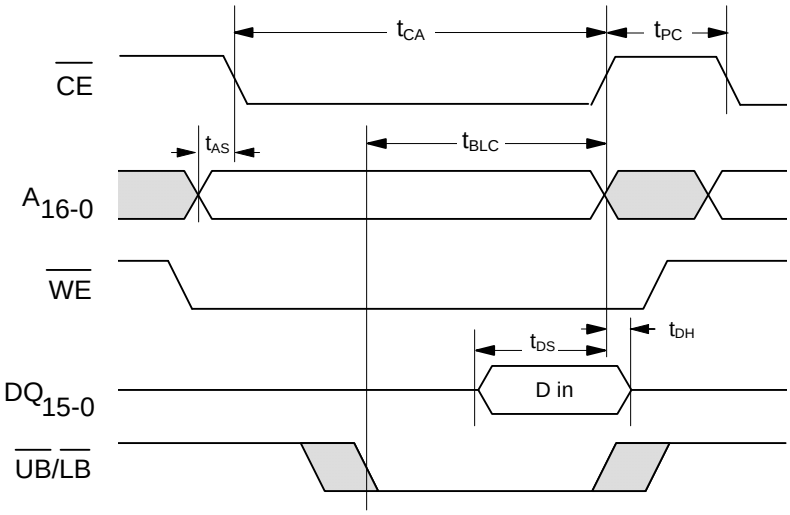
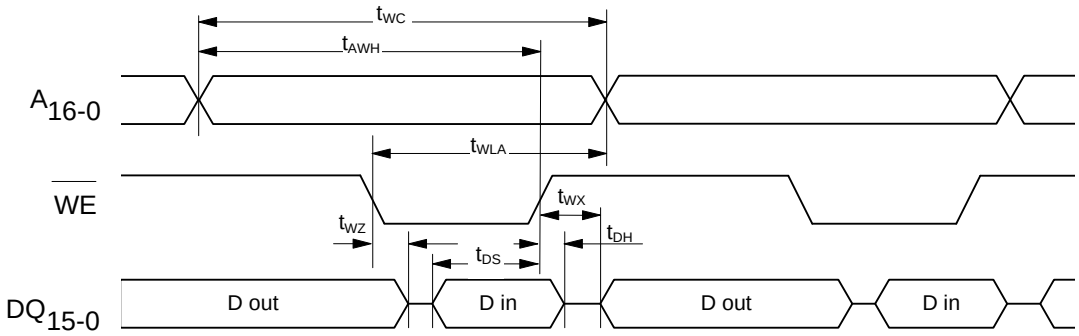


Figure 13. Write Cycle Timing 3 ($\overline{CE}$ LOW) [10]



Note
10. $\overline{OE}$ (not shown) is LOW only to show the effect of $\overline{WE}$ on DQ pins.

Switching Waveforms (continued)

Figure 14. Write Cycle Timing 4 ($\overline{CE}$ LOW) [11]

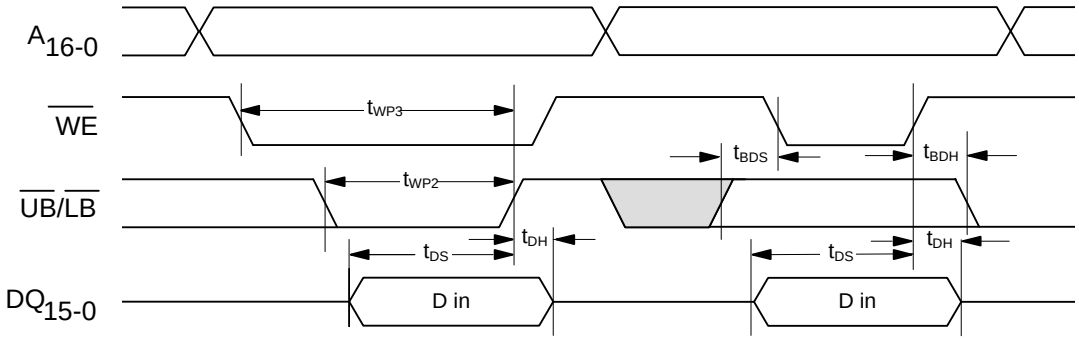
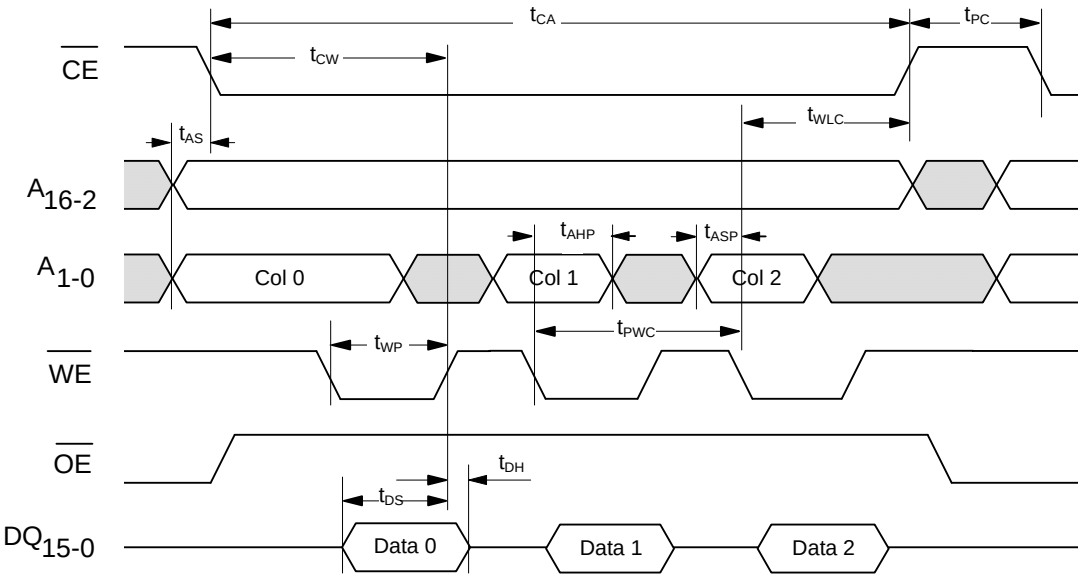


Figure 15. Page Mode Write Cycle Timing



Note
11. $\overline{UB}$ and $\overline{LB}$ to show byte enable and byte masking cases.

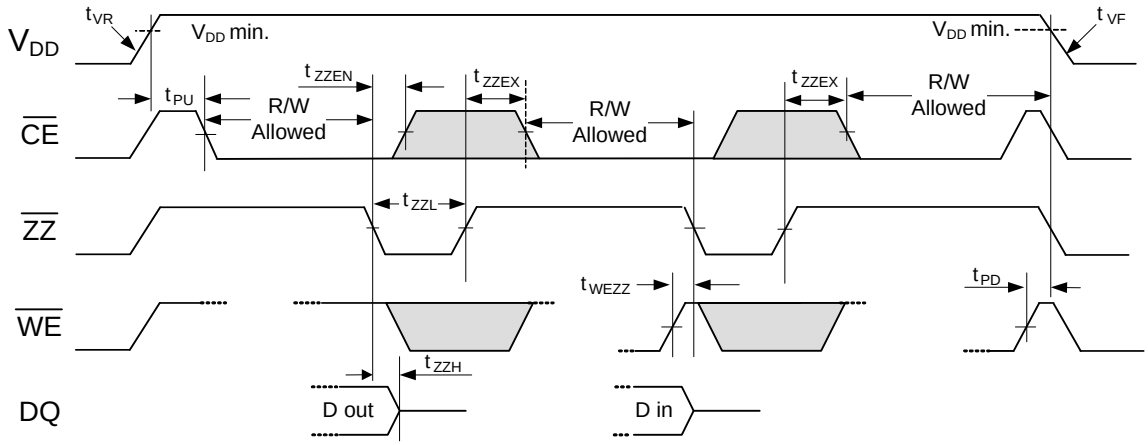
Power Cycle and Sleep Mode Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up (after V_{DD} min. is reached) to first access time	1	–	ms
t_{PD}	Last write ($\overline{WE}$ HIGH) to power down time	0	–	ms
t_{VR}[12]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF}[12]	V_{DD} power-down ramp rate	100	–	µs/V
t_{ZZH}	$\overline{ZZ}$ active to DQ HI-Z time	–	20	ns
t_{WEZZ}	Last write to sleep mode entry time	0	–	µs
t_{ZZL}	$\overline{ZZ}$ active LOW time	1	–	µs
t_{ZZEN}	Sleep mode entry time ($\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	0	µs
t_{ZZEX}	Sleep mode exit time ($\overline{ZZ}$ HIGH to 1st access after wakeup)	–	450	µs

Switching Waveform

Figure 16. Power Cycle and Sleep Mode Timing



Note
12. Slope measured at any point on the V_{DD} waveform.

Functional Truth Table

$\overline{CE}$	$\overline{WE}$	A_{16-2}	A_{1-0}	$\overline{ZZ}$	Operation [13, 14]
X	X	X	X	L	Sleep Mode
H	X	X	X	H	Standby/Idle
↓ L	H H	V V	V V	H H	Read
L	H	No Change	Change	H	Page Mode Read
L	H	Change	V	H	Random Read
↓ L	L L	V V	V V	H H	$\overline{CE}$-Controlled Write [14]
L	↓	V	V	H	$\overline{WE}$-Controlled Write [14, 15]
L	↓	No Change	V	H	Page Mode Write [16]
↑ L	X X	X X	X X	H H	Starts pre-charge

Byte Select Truth Table

$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Operation [17]
H	H	X	X	Read; Outputs disabled
	X	H	H	
H	L	H	L	Read upper byte; HI-Z lower byte
		L	H	Read lower byte; HI-Z upper byte
		L	L	Read both bytes
L	X	H	L	Write upper byte; Mask lower byte
		L	H	Write lower byte; Mask upper byte
		L	L	Write both bytes

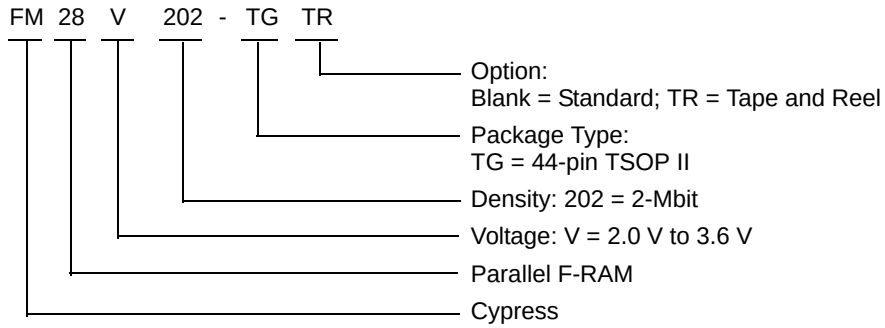
Notes
13. H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.
14. For write cycles, data-in is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever comes first.
15. $\overline{WE}$-controlled write cycle begins as a Read cycle and then A_{16-2} is latched.
16. Addresses A_{1-0} must remain stable for at least 15 ns during page mode operation.
17. The $\overline{UB}$ and $\overline{LB}$ pins may be grounded if 1) the system does not perform byte writes and 2) the device is not configured as a 256K x 8.

Ordering Information

Access time (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
60	FM28V202-TG	51-85087	44-pin TSOP II with software WP, sleep mode	Industrial
	FM28V202-TGTR	51-85087		

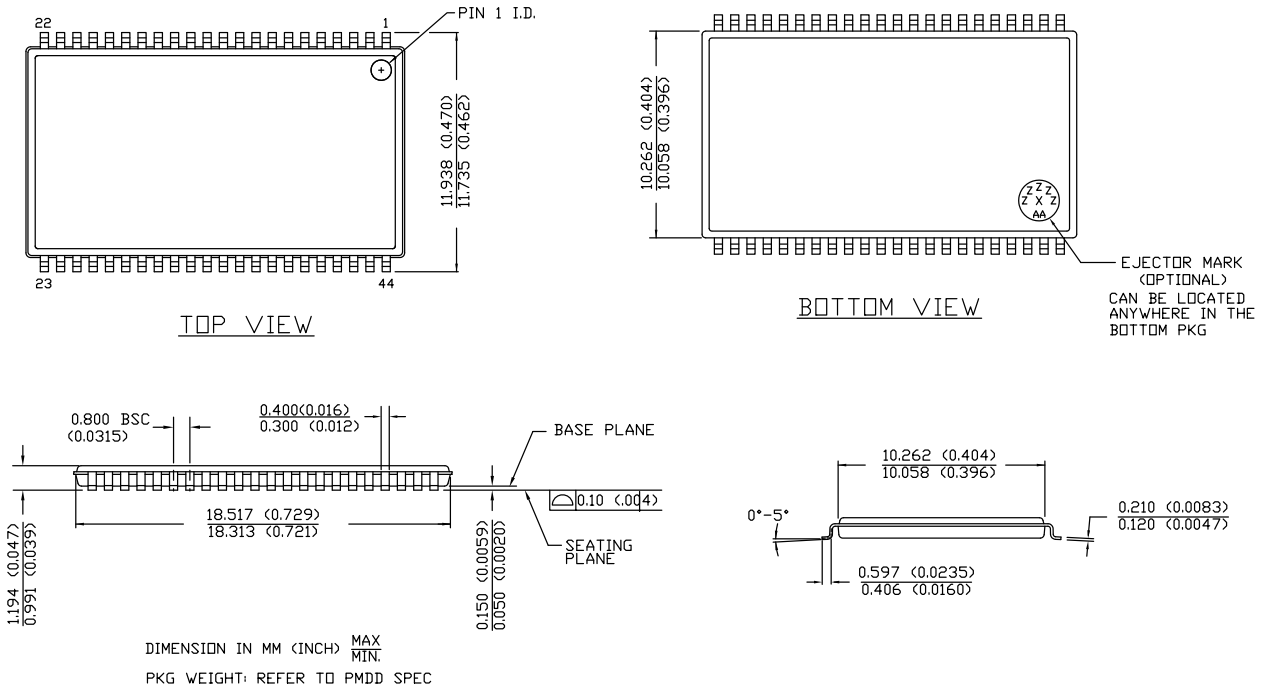
All the above parts are Pb-free.

Ordering Code Definitions



Package Diagram

Figure 17. 44-pin TSOP II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{UB}$	Upper Byte
$\overline{LB}$	Lower Byte
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
$\overline{OE}$	Output Enable
RoHS	Restriction of Hazardous Substances
RW	Read and Write
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
MΩ	megaohm
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM28V202, 2-Mbit (128 K × 16) F-RAM Memory Document Number: 001-86602				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3930342	GVCH	03/12/2013	New spec.
*A	4043471	GVCH	06/28/2013	Added 48-ball FBGA package
*B	4123023	GVCH	09/20/2013	Converted source from word file to frame maker file.
*C	4136685	GVCH	10/01/2013	Removed 48-ball FBGA package related information across the document. Updated AC Switching Characteristics: Changed minimum values of t_{WP} parameter from 20 ns to 22 ns for V_{DD} = 2.0 V to 2.7 V and from 30 ns to 18 ns for V_{DD} = 2.7 V to 3.6 V. Updated Power Cycle and Sleep Mode Timing: Changed description of t_{VR} parameter from "V_{DD} rise time" to "V_{DD} power-up slew rate". Changed description of t_{VF} parameter from "V_{DD} fall time" to "V_{DD} power-down slew rate".
*D	4211481	GVCH	01/23/2014	Updated DC Electrical Characteristics: Added Note 2 and referred the same note in "Typ" column. Updated Test Conditions of I_{LI} parameter (Removed V_{OUT}). Updated Test Conditions of I_{LO} parameter (Removed V_{IN}). Updated Data Retention and Endurance: Changed minimum value of T_{DR} parameter from 37 years to 38 years at Test Condition "75 °C". Changed minimum value of T_{DR} parameter from 145 years to 151 years at Test Condition "85 °C". Updated Power Cycle and Sleep Mode Timing: Changed description of t_{VR} parameter from "V_{DD} power-up slew rate" to "V_{DD} power-up ramp rate". Changed description of t_{VF} parameter from "V_{DD} power-down slew rate" to "V_{DD} power-down ramp rate".

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