ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EP53A7LQI	ADXX	-40°C to +125°C	16-pin (3mm x 3mm x 1.1mm) QFN
EP53A7HQI	AGXX	-40°C to +125°C	16-pin (3mm x 3mm x 1.1mm) QFN
EP53A7LQI-E		EP53A7LQI Evaluation Board	
EP53A7HQI-E		EP53A7HQI Evaluation Board	

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

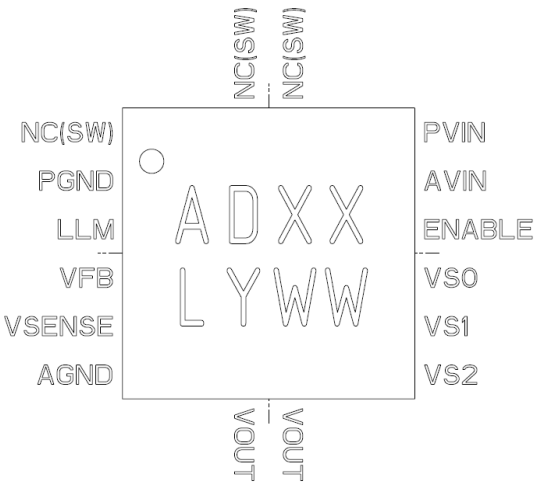


Figure 3. EP53A7LQI Pin Out Diagram (Top View)

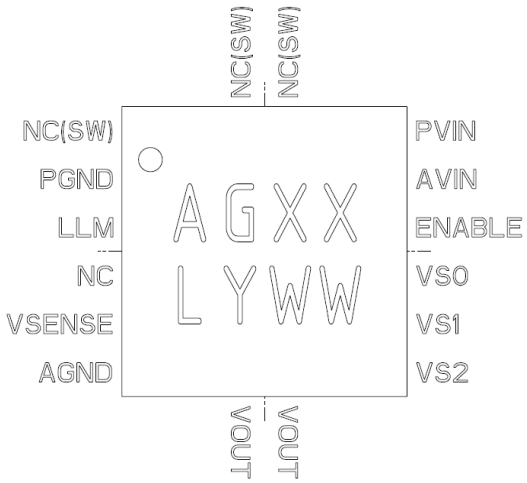


Figure 4. EP53A7HQI Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 15, 16	NC(SW)	-	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. NC (SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage to the device.
2	PGND	Ground	Power ground. Connect this pin to the ground electrode of the Input and output filter capacitors.
3	LLM	Analog	LLM (Light load mode – "LLM") pin. Logic-High enables automatic LLM/PWM and logic-low places the device in fixed PWM operation.
4	VFB/ NC	Analog	EP53A7LQI: Feedback pin for external divider option. EP53A7HQI: No Connect
5	VSENSE	Analog	Sense pin for preset output voltages. Refer to application section for proper configuration.
6	AGND	Power	Analog ground. This is the quiet ground for the internal control circuitry, and the ground return for external feedback voltage divider
7, 8	VOUT	Power	Regulated Output Voltage. Refer to application section for proper layout and decoupling.
9, 10, 11	VS2, VS1, VS0	Analog	Output voltage select. VS2 = pin 9, VS1 = pin 10, VS0 = pin 11. EP53A7LQI: Selects one of seven preset output voltages or an external resistor divider. EP53A7HQI: Selects one of eight preset output voltages. (Refer to section on output voltage select for more details.)
12	ENABLE	Analog	Output Enable. Enable = logic high; Disable = logic low
13	AVIN	Power	Input power supply for the controller circuitry. Connect to PVIN through a 100 Ohm resistor.
14	PVIN	Power	Input Voltage for the MOSFET switches.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage		-0.3	6.0	V
ENABLE, V_{SENSE}, $V_{SO} – V_{S2}$		-0.3	V_{IN}+0.3	V
V_{FB} (EP53A7LQI)		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.7	5.5	V
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Resistance: Junction to Ambient –0 LFM (1)	θ_{JA}	80	°C/W
Thermal Overload Trip Point	T_{J-TP}	+155	°C
Thermal Overload Trip Point Hysteresis		25	°C

(1) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VIN = 3.6V.

C_{IN} = -4.7µF MLCC, C_{OUT} = 10µF MLCC

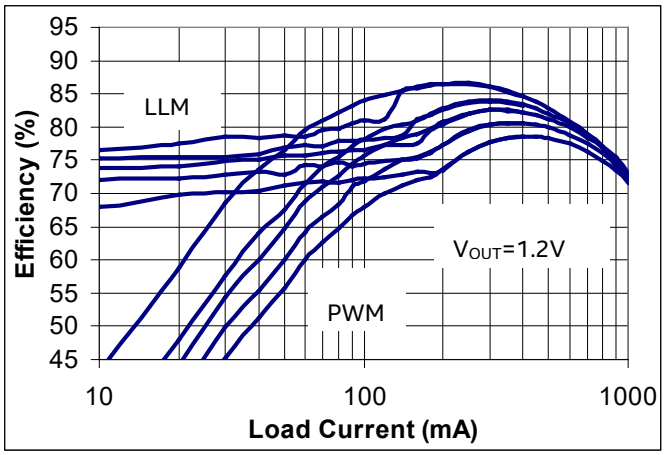
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLO_R}			2.0		V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLO_F}			1.9		V/ms
Drop Out Resistance	R_{DO}	Input to Output Resistance		350	500	mΩ
Output Voltage Range	V_{OUT}	EP53A7LQI (V_{DO} = I_{LOAD} X R_{DO}) EP53A7HQI	0.6 1.8		V_{IN}-V_{DO} 3.3	V
Dynamic Voltage Slew Rate	V_{SLEW}	EP53A7HQI EP53A7LQI		8 4		V/ms
VID Preset V_{OUT} Initial Accuracy	ΔV_{OUT}	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	-2		+2	%
VFB Pin Voltage (Load and Temperature)	V_{VFB}	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	0.588	0.6	0.612	V
Line Regulation	ΔV_{OUT_LINE}	2.4V ≤ V_{IN} ≤ 5.5V		0.03		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ I_{LOAD} ≤ 1A		0.6		%/A
Temperature Variation	ΔV_{OUT_TEMPL}	-40°C ≤ T_A ≤ +85°C		30		ppm/°C
Output Current Range	I_{OUT}		1000			mA
Shut-down Current	I_{SD}	Enable = Low		0.75		µA
EP53A7HQI Operating Quiescent Current	I_Q	I_{LOAD}=0; Preset Output Voltages, LLM=High		55		µA
EP53A7LQI Operating Quiescent Current	I_Q	I_{LOAD}=0; Preset Output Voltages, LLM=High		65		µA
OCP Threshold	I_{LIM}	2.4V ≤ V_{IN} ≤ 5.5V 0.6V ≤ V_{OUT} ≤ 3.3V	1.25	1.4		A

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Pin Input Current (1)	I_{FB}			<100		nA
VS0-VS2, Pin Logic Low	V_{VSLO}		0.0		0.3	V
VS0-VS2, Pin Logic High	V_{VSHI}		1.4		V_{IN}	V
VS0-VS2, Pin Input Current (1)	I_{VSX}			<100		nA
Enable Pin Logic Low	V_{ENLO}				0.3	V
Enable Pin Logic High	V_{ENHI}		1.4			V
Enable Pin Current (1)	I_{ENABLE}			<100		nA
LLM Engage Headroom		Minimum difference between V_{IN} and V_{OUT} to ensure proper LLM operation	700			mV
LLM Pin Logic Low	V_{LLMLO}				0.3	V
LLM Pin Logic High	V_{LLMHI}		1.4			V
LLM Pin Current	I_{LLM}			<100		nA
Operating Frequency	F_{OSC}			5		MHz
Soft Start Slew Rate	ΔV_{SS}	EP53A7HQI (VID only) EP53A7LQI (VID only)		8 4		V/ms
Soft Start Rise Time (2)	ΔT_{SS}	EP53A7LQI (VFB mode)	170	225	280	µs

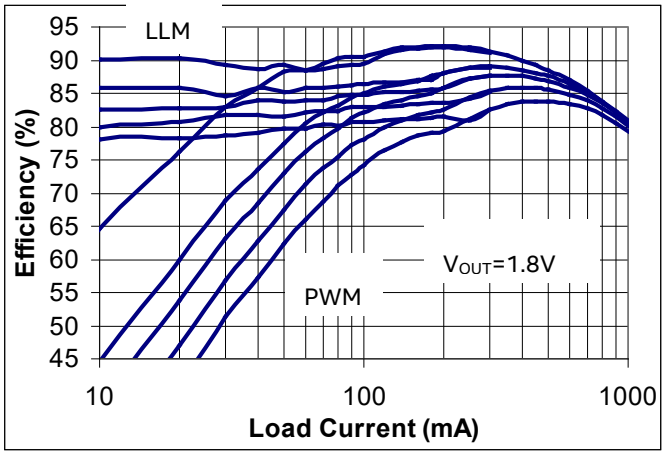
(1) Parameter guaranteed by design and characterization.

(2) Measured from when $V_{IN} \geq V_{UVLO\_R}$ & ENABLE pin crosses its logic High threshold.

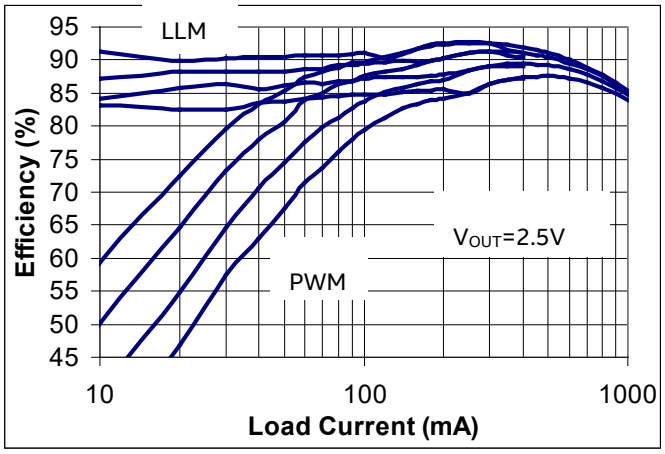
TYPICAL PERFORMANCE CURVES



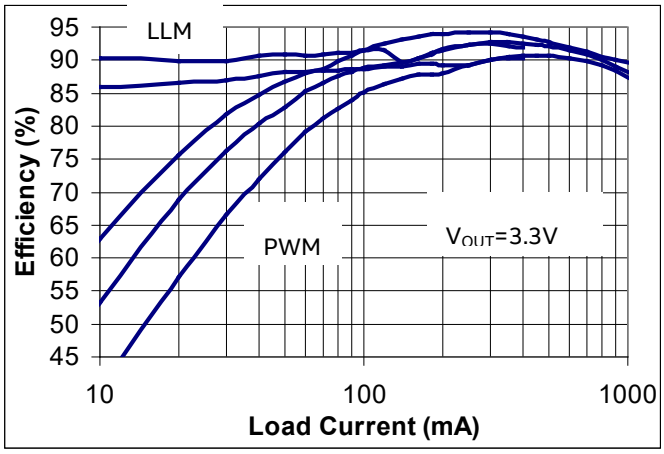
Efficiency vs. Load Current: V_{OUT} = 1.2V, V_{IN} (from top to bottom) = 2.5, 3.3, 3.7, 4.3, 5.0V



Efficiency vs. Load Current: V_{OUT} = 1.8V, V_{IN} (from top to bottom) = 2.5, 3.3, 3.7, 4.3, 5.0V

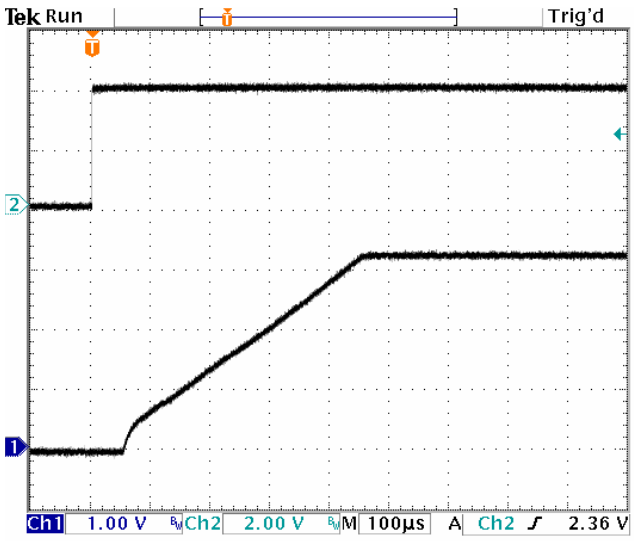


Efficiency vs. Load Current: V_{OUT} = 2.5V, V_{IN} (from top to bottom) = 3.3, 3.7, 4.3, 5.0V



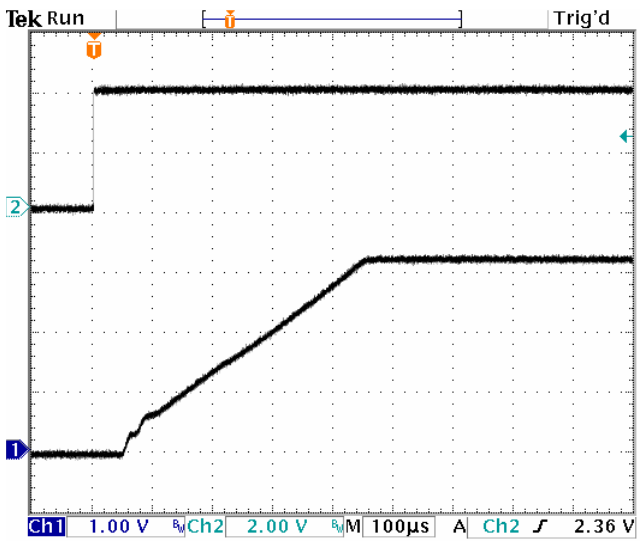
Efficiency vs. Load Current: V_{OUT} = 3.3V, V_{IN} (from top to bottom) = 3.7, 4.3, 5.0V

TYPICAL PERFORMANCE CHARACTERISTICS



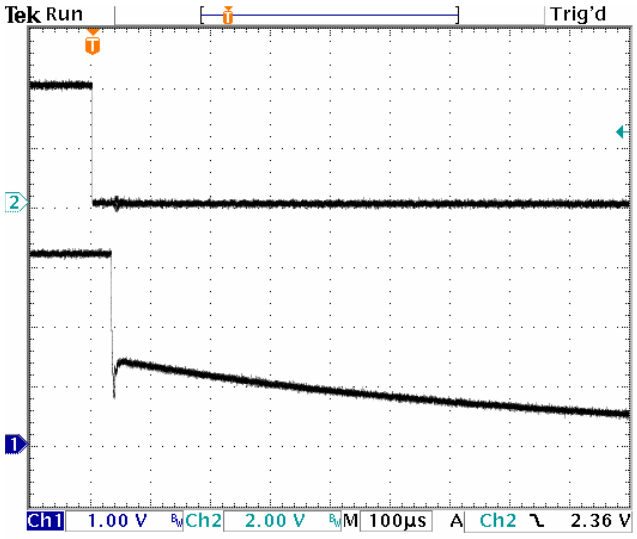
Start Up Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V;

I_{LOAD} = 10mA; VID Mode



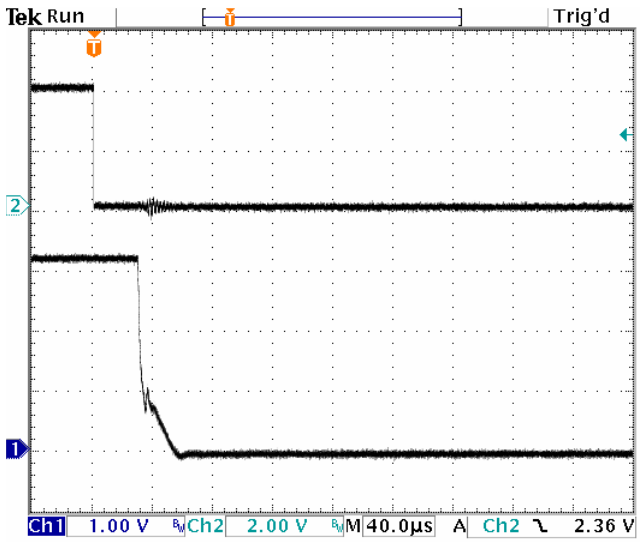
Start Up Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V;

I_{LOAD} = 1000mA; VID Mode



Shut-down Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V;

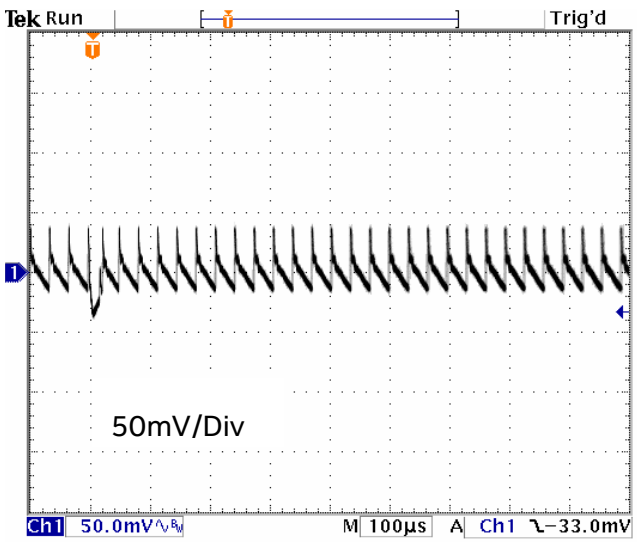
I_{LOAD} = 10mA, PWM



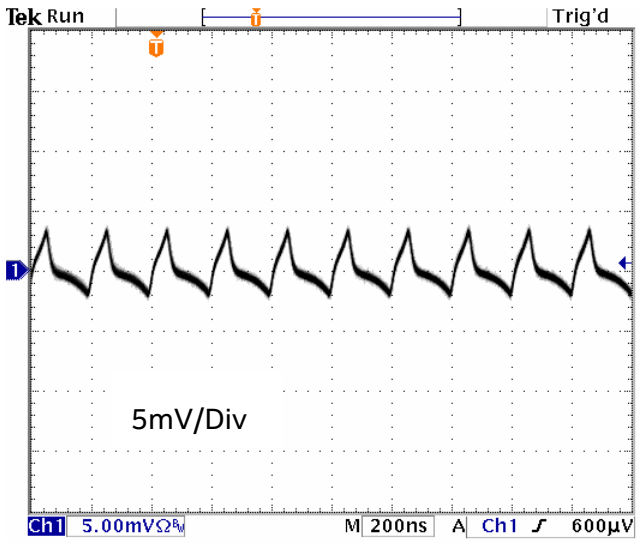
Shut-down Waveform: V_{IN} = 5.0V, V_{OUT} = 3.3V;

I_{LOAD} = 1000mA, PWM

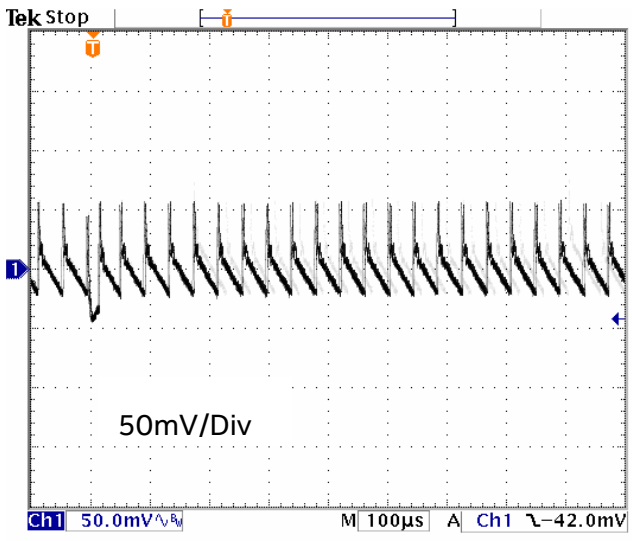
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



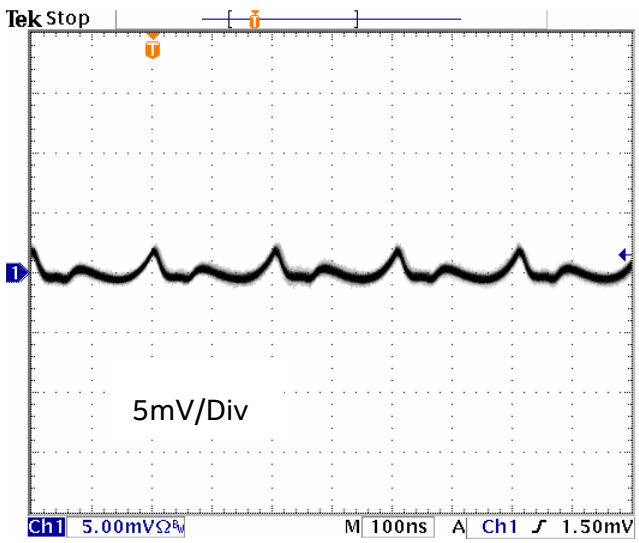
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 1.2V, Load = 10mA LLM enabled



Output Ripple: V_{IN} = 5.0V, V_{OUT} = 1.2V, Load = 1A

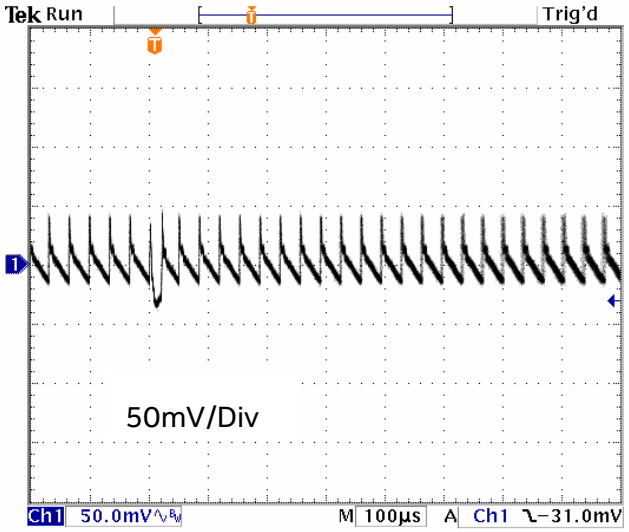


Output Ripple: V_{IN} = 5.0V, V_{OUT} = 3.3V, Load = 10mA LLM enabled



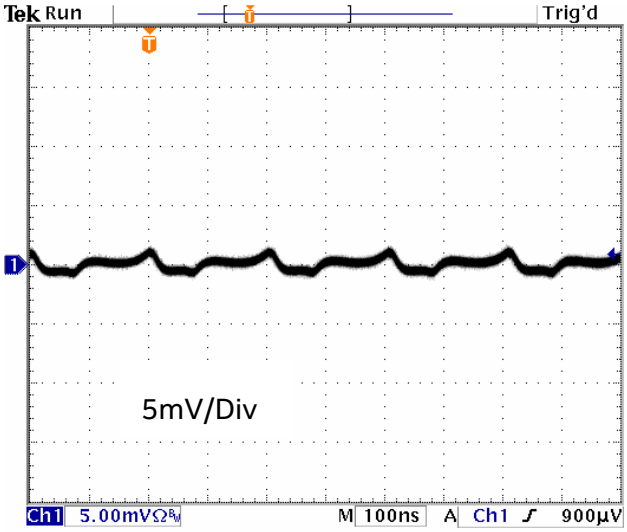
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 3.3V, Load = 1A

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



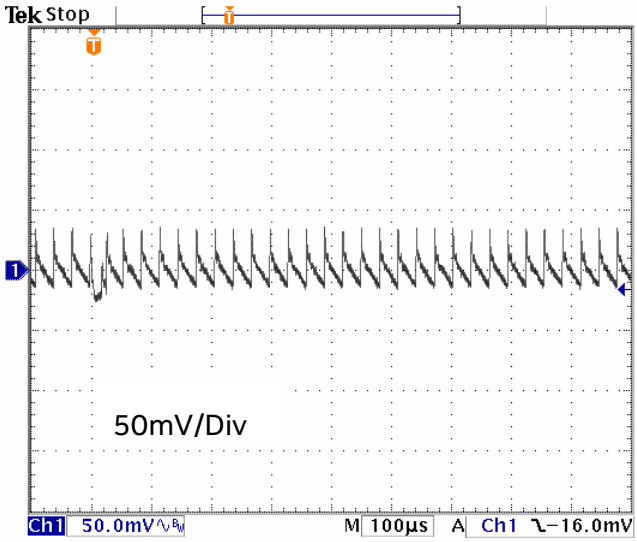
Output Ripple: VIN = 3.3V, VOUT = 1.8V, Load = 10mA

LLM enabled



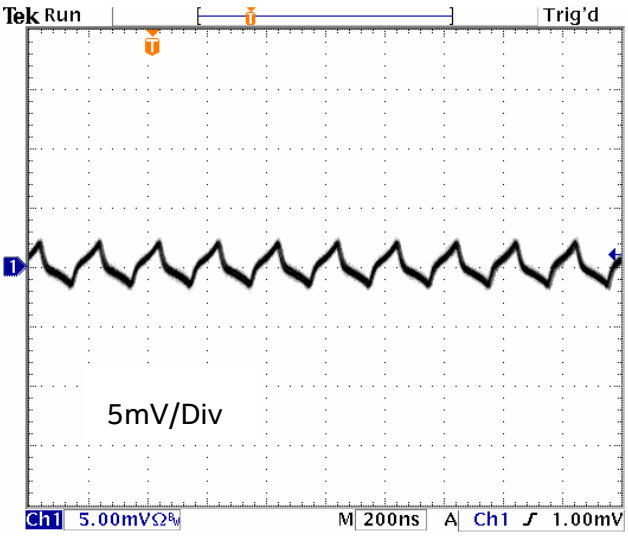
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.8V

Load = 1A



Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V, Load = 10mA

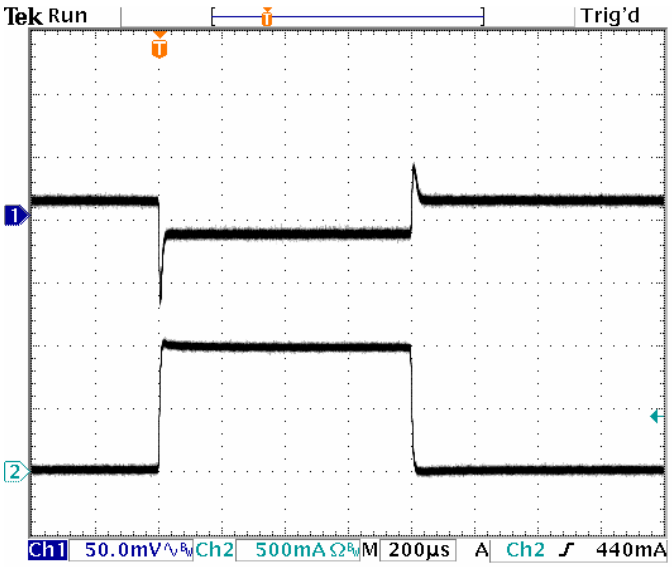
LLM enabled



Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V,

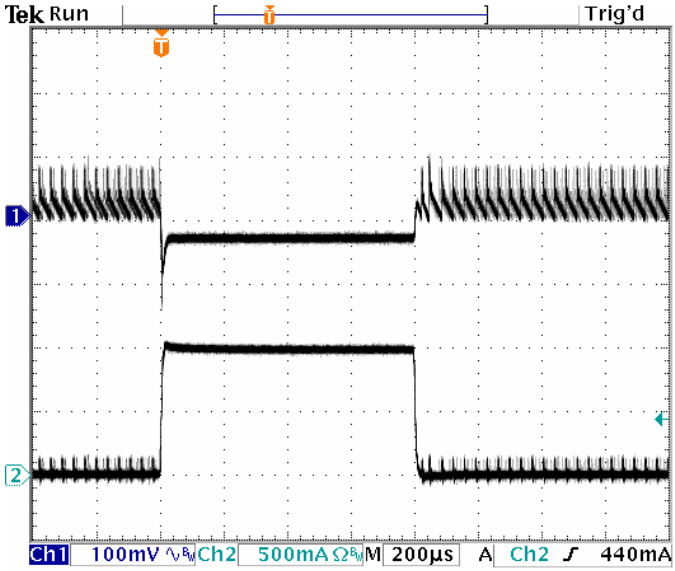
Load = 1A

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



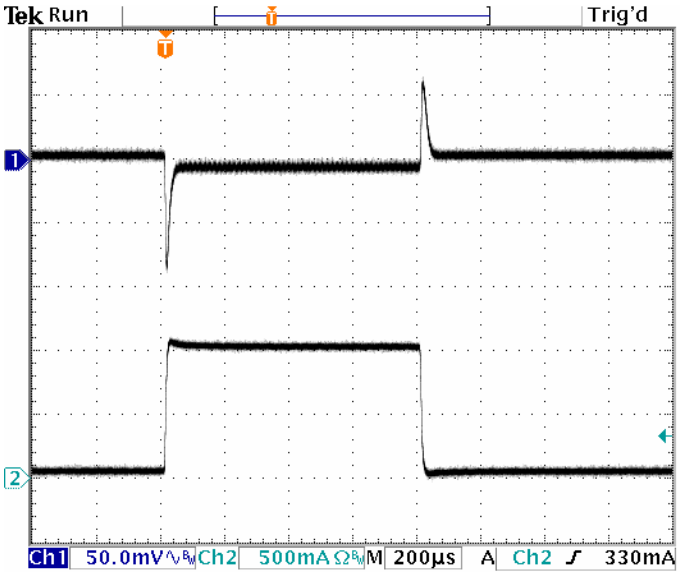
Load Transient: V_{IN} = 5.0V, V_{OUT} = 3.3V

Load stepped from 0mA to 1000mA



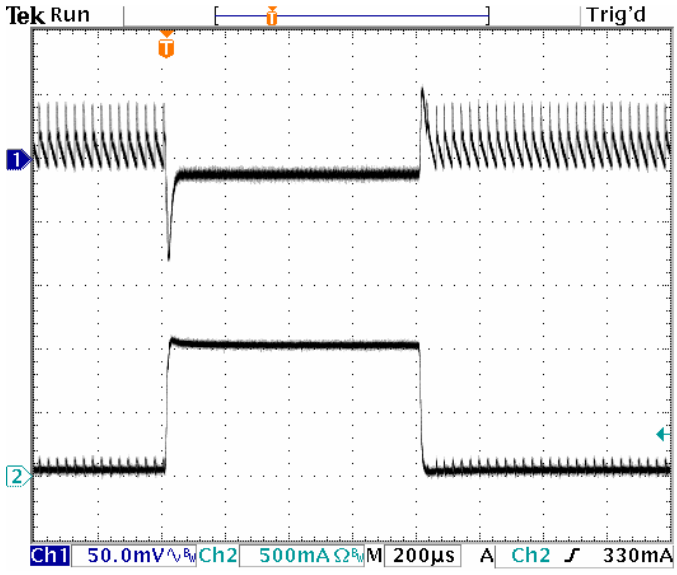
Load Transient: V_{IN} = 5.0V, V_{OUT} = 3.3V

Load stepped from 10mA to 1000mA, LLM enabled



Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.2V

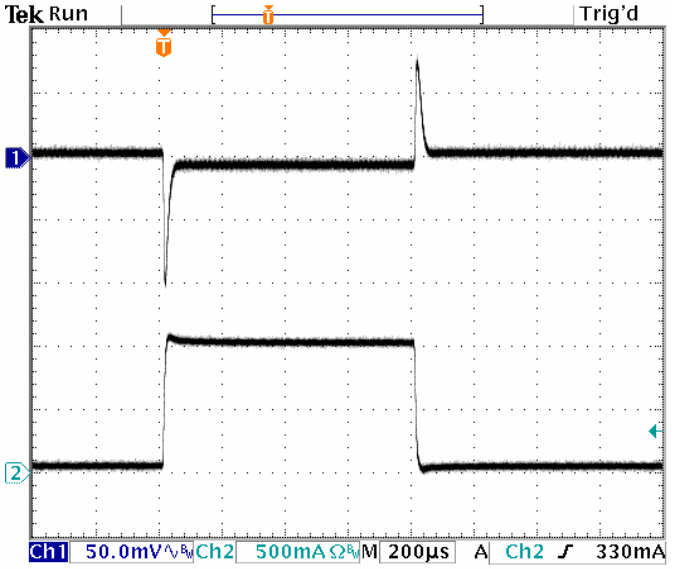
Load stepped from 0mA to 1000mA



Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.2V

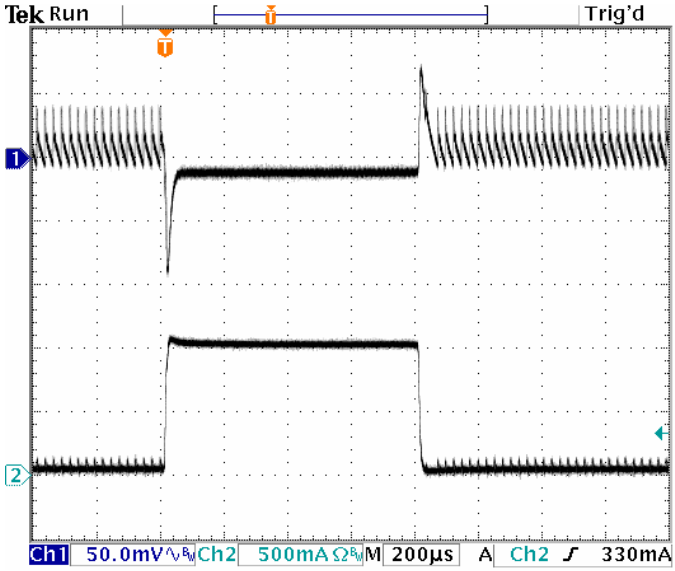
Load stepped from 10mA to 1000mA, LLM enabled

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



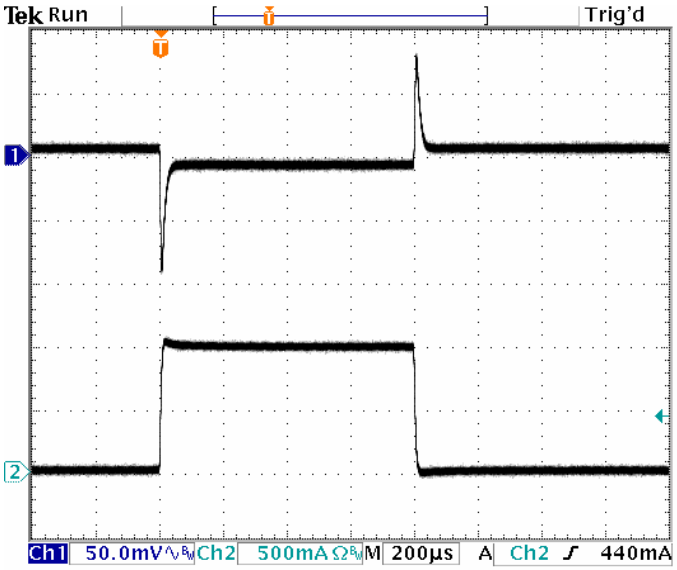
Load Transient: V_{IN} = 3.7V, V_{OUT} = 1.2V

Load stepped from 0mA to 1000mA



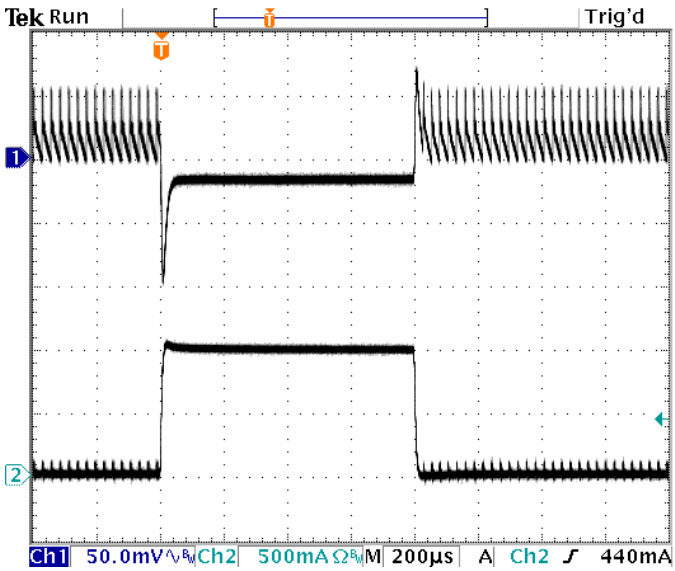
Load Transient: V_{IN} = 3.7V, V_{OUT} = 1.2V

Load stepped from 10mA to 1000mA, LLM enabled



Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.8V

Load stepped from 0mA to 1000mA



Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.8V

Load stepped from 10mA to 1000mA, LLM enabled

FUNCTIONAL BLOCK DIAGRAM

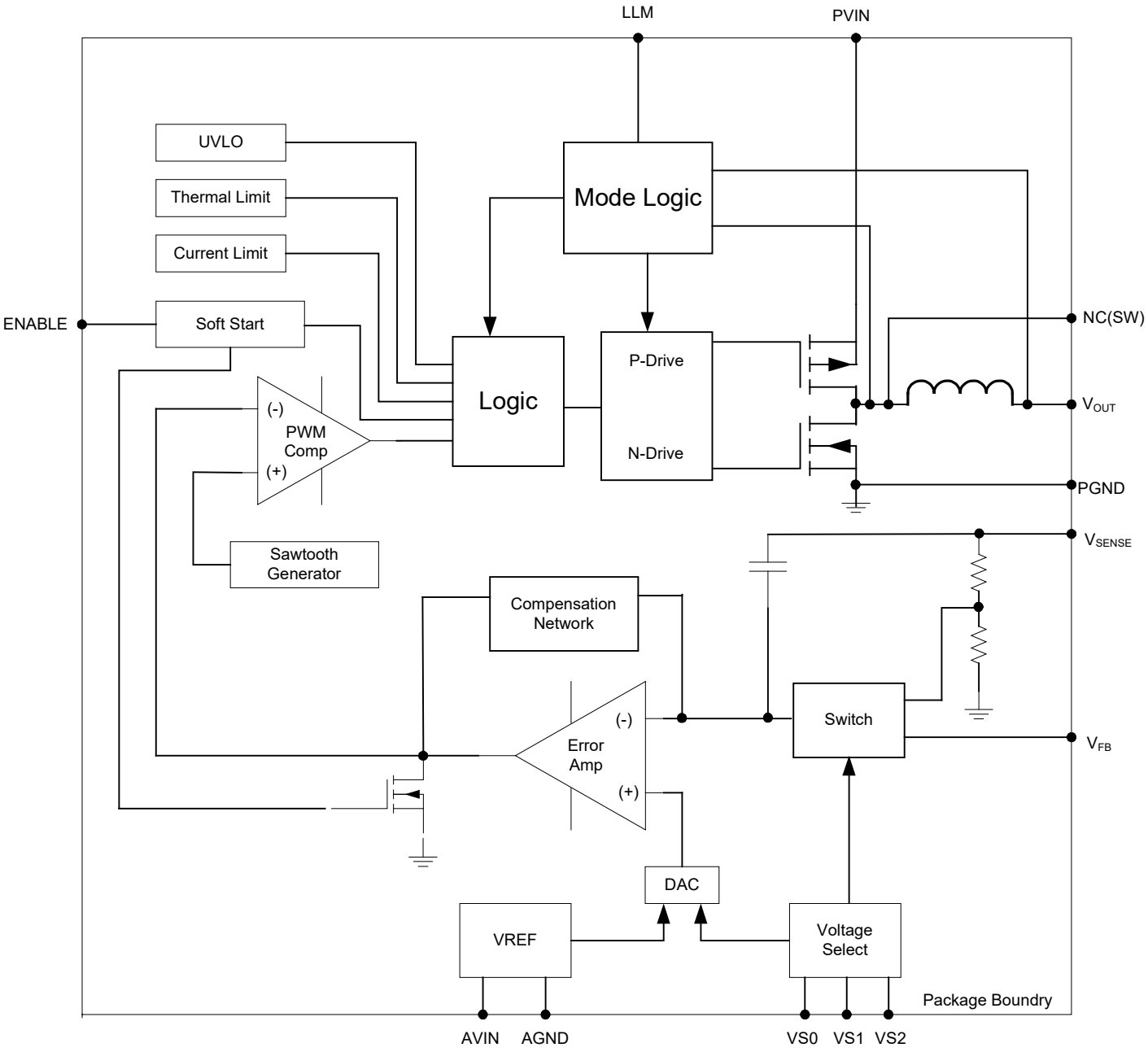


Figure 5: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EP53A7xQI requires only 2 small MLCC capacitors and an 0201 resistor for a complete DC-DC converter solution. The device integrates MOSFET switches, PWM controller, Gate-drive, compensation, and inductor into a tiny 3mm x 3mm x 1.1mm QFN package. Advanced package design, along with the high level of integration, provides very low output ripple and noise. The EP53A7xQI uses voltage mode control for high noise immunity and load matching to advanced ≤90nm loads. A 3-pin VID allows the user to choose from one of 8 output voltage settings. The EP53A7xQI comes with two VID output voltage ranges. The EP53A7HQI provides V_{OUT} settings from 1.8V to 3.3V, the EP53A7LQI provides VID settings from 0.8V to 1.5V, and also has an external resistor divider option to program output setting over the 0.6V to V_{IN}-0.5V range. The EP53A7xQI provides the industry's highest power density of any 1A DCDC converter solution.

The key enabler of this revolutionary integration is Altera Enpirion's proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seamless integration of all switching, control, and compensation circuitry.

The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Altera Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor

The EP53A7xQI utilizes a proprietary low loss integrated inductor. The integration of the inductor greatly simplifies the power supply design process. The integrated inductor provides the optimal solution to the complexity, output ripple, and noise that plague low power DC-DC converter design.

Voltage Mode Control

The EP53A7xQI utilizes an integrated type III compensation network. Voltage mode control is inherently impedance matched to the sub 90nm process technology that is used in today's advanced ICs. Voltage mode control also provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The very high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance.

Light Load Mode (LLM) Operation

The EP53A7xQI uses a proprietary light load mode to provide high efficiency in the low load operating condition. When the LLM pin is high, the device is in automatic LLM/PWM mode. When the LLM pin is low, the device is in PWM mode. In automatic LLM/PWM mode, when a light load condition is detected, the device will (1) step V_{OUT} up by approximately 1.5% above the nominal operating output voltage setting, V_{NOM}, and then (2) shut down unnecessary circuitry, and (3) monitor V_{OUT}. When V_{OUT} falls below V_{NOM}, the device will repeat (1), (2), and (3). The voltage step up, or pre-positioning, improves transient droop when a load transient causes a transition from LLM mode to PWM mode. If a load transient occurs, causing V_{OUT} to fall below the threshold V_{MIN}, the device will exit LLM operation and begin normal PWM operation. Figure 6 demonstrates V_{OUT} behavior during transition into and out of LLM operation.

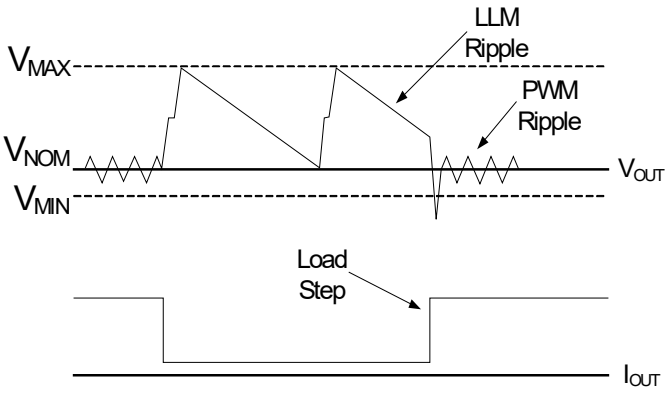


Figure 6: V_{OUT} Behavior in LLM Operation

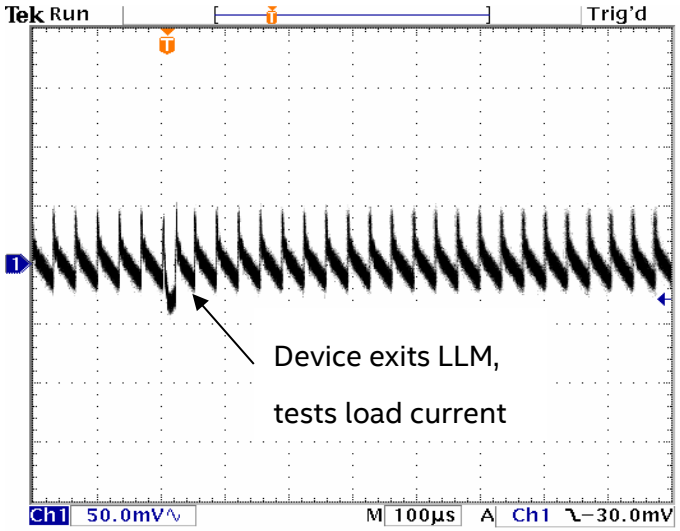


Figure 1: V_{OUT} Droop during Periodic LLM Exit

Many multi-mode DC-DC converters suffer from a condition that occurs when the load current increases only slowly so that there is no load transient driving V_{OUT} below the V_{MIN} threshold (shown in Figure 6). In this condition, the device would never exit LLM operation. This could adversely affect efficiency and cause unwanted ripple. To prevent this from occurring, the EP53A7xQI periodically exits LLM mode into PWM mode and measures the load current. If the load current is above the LLM threshold current, the device will remain in PWM mode. If the load current is below the LLM threshold, the device will re-enter LLM operation. There will be a small droop in V_{OUT} at the point where the device exits and re-enters LLM, as shown in Figure 7. The load current at which the device will enter LLM mode is a function of input and output voltage. Figure 8 shows the typical value at which the device will enter LLM operation. The actual load current at which the device will enter LLM operation can vary by +/-30%. Table 1 shows the minimum load current below which the device is guaranteed to be in LLM operating mode.

To ensure normal LLM operation, LLM mode should be enabled/disabled with specific sequencing. For applications with explicit LLM pin control, enable LLM after VIN ramp up complete; disable LLM before VIN ramp down. For applications with ENABLE control, tie LLM to ENABLE; enable device after VIN ramp up complete and disable device before VIN rampdown begins. For devices with ENABLE and LLM tied to VIN, contact Intel Applications engineering for specific recommendations.

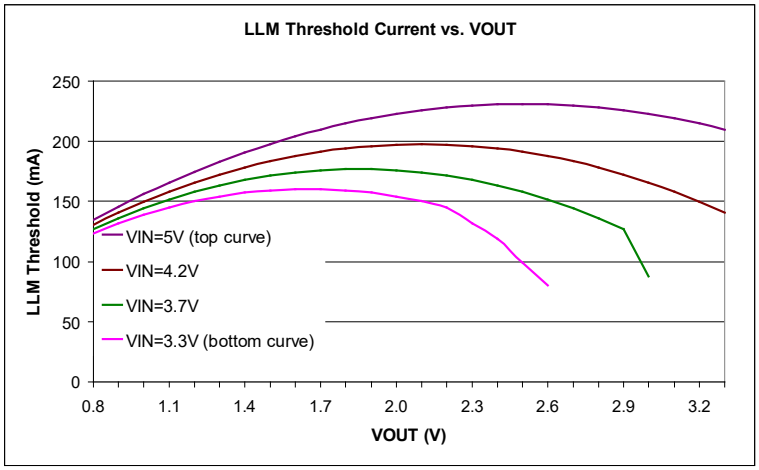


Figure 2: Typical load current for LLM engage and disengage versus V_{OUT} for selected input voltages

Increased output filter capacitance and/or increased bulk capacitance at the load will decrease the magnitude of the LLM ripple. Refer to the section on output filter capacitance for maximum values of output filter capacitance and the Soft-Start section for maximum bulk capacitance at the load.

NOTE: For proper LLM operation the EP53A7xQI requires a minimum difference between V_{IN} and V_{OUT} of 700mV. If this condition is not met, the device cannot be assured proper LLM operation.

NOTE: Automatic LLM/PWM is not available when using the external resistor divider option for V_{OUT} programming.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EP53A7HQI has a soft-start slew rate that is twice that of the EP53A7LQI.

When the EP53A7LUI is configured in external resistor divider mode, the device has a fixed VOUT ramp time. Therefore, the ramp rate will vary with the output voltage setting. Output voltage ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. The maximum total capacitance on the output, including the output filter capacitor and bulk and decoupling capacitance, at the load, is given as:

EP53A7LQI:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 200\mu F$

EP53A7HQI:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 100\mu F$

EP53A7LUI in external divider mode:

$C_{OUT\_TOTAL\_MAX} = 2.25x10^{-4}/V_{OUT}$ Farads

The nominal value for C_{OUT} is 10µF. See the applications section for more details.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for approximately 0.5mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

During initial power up, an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold, the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation.

NOTE: The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature, the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 25C°, the device will go through the normal startup process.

APPLICATION INFORMATION

Output Voltage Programming

The EP53A7xQI utilizes a 3-pin VID to program the output voltage value. The VID is available in two sets of output VID programming ranges. The VID pins should be connected either to an external control signal, AVIN or to AGND to avoid noise coupling into the device. The VID pins must not be left floating.

The "Low" range is optimized for low voltage applications. It comes with preset VID settings ranging from 0.80V and 1.5V. This VID set also has an external divider option.

To specify this VID range, order part number EP53A7LQI.

The "High" VID set provides output voltage settings ranging from 1.8V to 3.3V. This version does not have an external divider option. To specify this VID range, order part number EP53A7HQI.

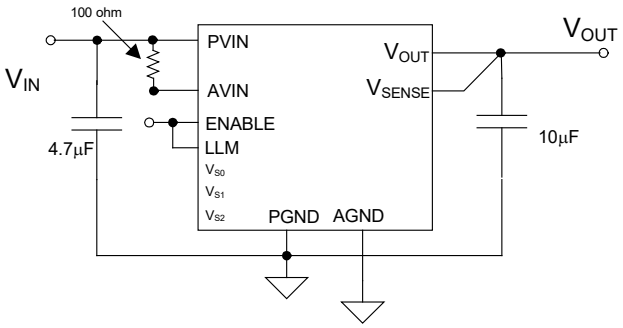


Figure 3: Application Circuit, EP53A7HQI. Note that all control signals should be connected to an external control signal, AVIN or AGND.

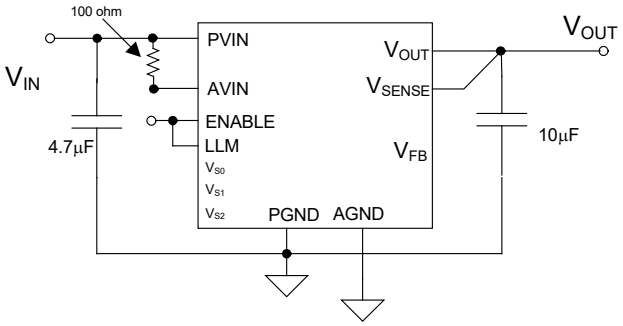


Figure 4: Application Circuit, EP53A7LQI showing the V_{FB} function.

Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

NOTE: The VID pins must not be left floating.

EP53A7L Low VID Range Programming

The EP53A7LQI is designed to provide a high degree of flexibility in powering applications that require low V_{OUT} settings and dynamic voltage scaling (DVS). The device employs a 3-pin VID architecture that allows the user to choose one of seven (7) preset output voltage settings, or the user can select an external voltage divider option. The VID pin settings can be changed on the fly to implement glitch-free voltage scaling.

Table 1: EP53A7LQI VID Voltage Select Settings

VS2	VS1	VS0	VOUT
0	0	0	1.50
0	0	1	1.45
0	1	0	1.20
0	1	1	1.15
1	0	0	1.10
1	0	1	1.05
1	1	0	0.80
1	1	1	EXT

Table 1 shows the VS2-VS0 pin logic states for the EP53A7LQI and the associated output voltage levels. A logic "1" indicates a connection to AVIN or to a "high" logic voltage level. A logic "0" indicates a connection to AGND or to a "low" logic voltage level. These pins can be either hardwired to AVIN or AGND or alternatively can be driven by standard logic levels. Logic levels are defined in the electrical characteristics table. Any level between the logic high and logic low is indeterminate.

EP53A7LQI External Voltage Divider

The external divider option is chosen by connecting VID pins VS2-VS0 to AVIN or a logic "1" or "high". The EP53A7LQI uses a separate feedback pin, V_{FB}, when using the external divider. V_{SENSE} must be connected to V_{OUT} as indicated in Figure 11.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{Ra}{Rb}\right)$$

R_a must be chosen as 237KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{142.2x10^3}{V_{OUT} - 0.6}\Omega$$

V_{OUT} can be programmed over the range of 0.6V to (V_{IN} – 0.5V).

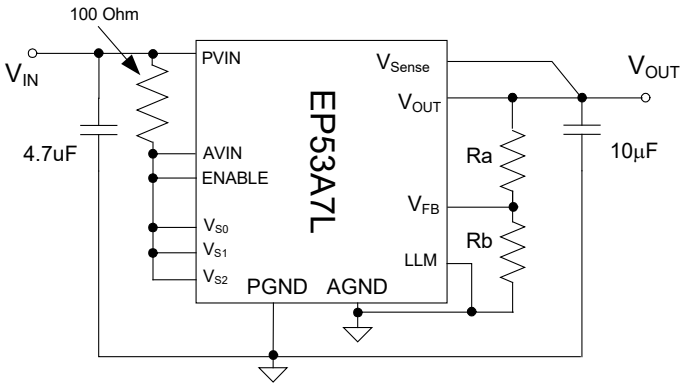


Figure 5: EP53A7LQI using external divider

NOTE: Dynamic Voltage Scaling is not allowed between internal preset voltages and external divider.

NOTE: LLM is not functional when using the external divider option. Tie the LLM pin to AGND when using this option.

EP53A7HQI High VID Range Programming

The EP53A7HQI V_{OUT} settings are optimized for higher nominal voltages such as those required to power IO, RF, or IC memory. The preset voltages range from 1.8V to 3.3V. There are eight (8) preset output voltage settings. The EP53A7HQI does not have an external divider option. As with the EP53A7LQI, the VID pin settings can be changed while the device is enabled.

Table 2 shows the VS0-VS2 pin logic states for the EP53A7HQI and the associated output voltage levels. A logic "1" indicates a connection to AVIN or to a "high" logic voltage level. A logic "0" indicates a connection to AGND or to a "low" logic voltage level. These pins can be either hardwired to AVIN or AGND or alternatively can be driven by standard logic levels. Logic levels are defined in the electrical characteristics table. Any level between the logic high and logic low is indeterminate. These pins must not be left floating.

Table 2: EP53A7HQI VID Voltage Select Settings

VS2	VS1	VS0	VOUT (V)
0	0	0	3.3
0	0	1	3.0
0	1	0	2.9
0	1	1	2.6
1	0	1	2.5
1	0	1	2.2
1	1	0	2.1
1	1	1	1.8

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EP53A7xQI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EP53A7xQI is not pre-biased when the EP53A7xQI is first enabled.

Input Filter Capacitor

The input filter capacitor requirement is a 4.7µF 0402 or 0603 low ESR MLCC capacitor.

Output Filter Capacitor

The output filter capacitor requirement is a minimum of 10µF 0805 MLCC. Ripple performance can be improved by using 2x10µF 0603 or 2x10µF 0805 MLCC capacitors.

The maximum output filter capacitance next to the output pins of the device is 60µF low ESR MLCC capacitance. V_{OUT} has to be sensed at the last output filter capacitor next to the EP53A7xQI.

Additional bulk capacitance for decoupling and bypass can be placed at the load as long as there is sufficient separation between the V_{OUT} Sense point and the bulk capacitance. The separation provides an inductance that isolates the control loop from the bulk capacitance.

NOTE: Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Refer to the section on Soft-Start for the maximum total capacitance on the output.

NOTE: The Input and Output capacitors must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter filter applications.

LAYOUT RECOMMENDATIONS

Figure 12 shows critical components and layer 1 traces of a recommended minimum footprint EP53A7LQI/EP53A7HQI layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Altera website www.intel.com/enpirion for exact dimensions and other layers. Please refer to Figure 12 while reading the layout recommendations in this section.

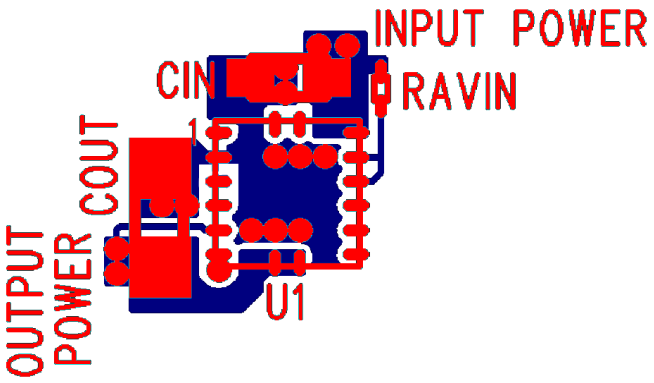


Figure 12: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EP53A7QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EP53A7QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Input and output grounds are separated until they connect at the PGND pins. The separation shown on Figure 12 between the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Altera website www.intel.com/enpirion.

Recommendation 4: Multiple small vias should be used to connect the ground traces under the device to the system ground plane on another layer for heat dissipation. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 12. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 5: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 12 this connection is made with RAVIN at the input capacitor close to the V_{IN} connection.

RECOMMENDED PCB FOOTPRIN

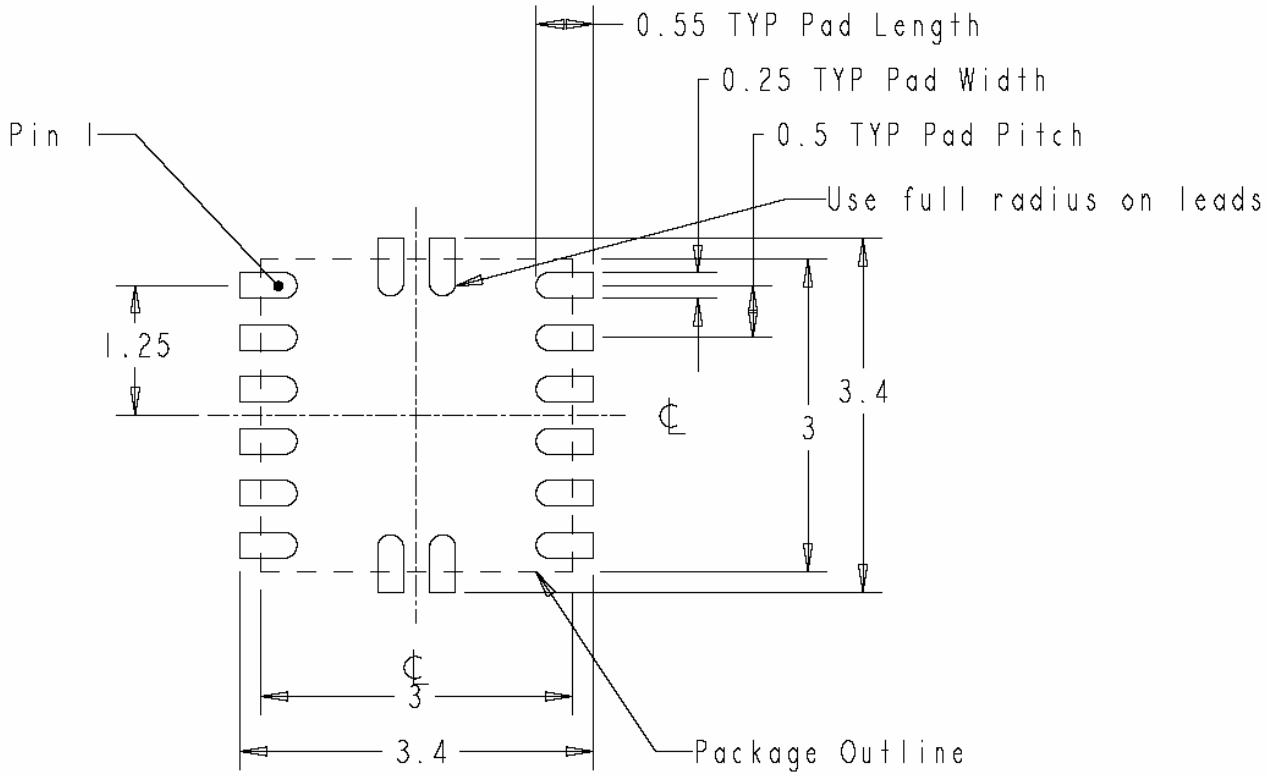


Figure 13: EP53A7xQI PCB Footprint (Top View)

PACKAGE DIMENSIONS

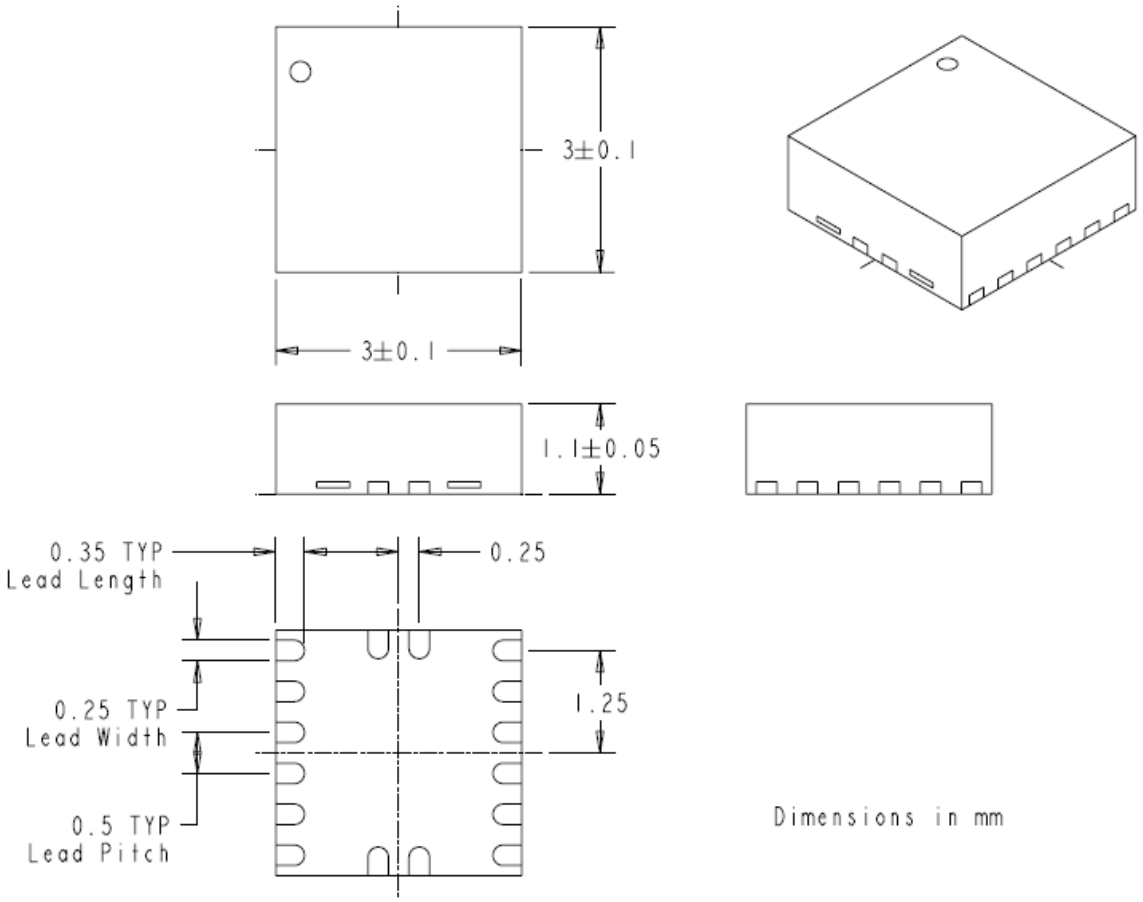


Figure 14: EP53A7xQI Package Dimensions

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
F	Jan 2019	Changed datasheet into Intel format.

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.altera.com/enpirion