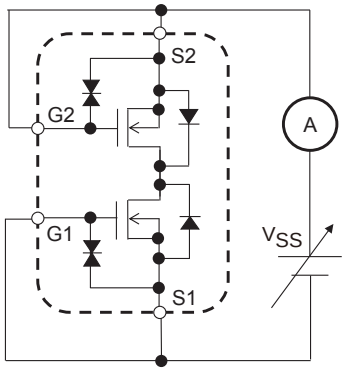
ELECTRICAL CHARACTERISTICS at Ta = 25°C (Note 2)

Parameter	Symbol	Conditions		Value			Unit
				min	typ	max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S=1mA, V_{GS}=0V	Test Circuit 1	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=10V, V_{GS}=0V	Test Circuit 1			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{SS}=0V	Test Circuit 2			±1	μA
Gate Threshold Voltage	V_{GS}(th)	V_{SS}=6V, I_S=1mA	Test Circuit 3	0.5		1.3	V
Forward Transconductance	g_{FS}	V_{SS}=6V, I_S=3A	Test Circuit 4		19		S
Static Source to Source On-State Resistance	R_{SS}(on)1	I_S=5A, V_{GS}=4.5V	Test Circuit 5	1.8	2.3	3.2	mΩ
	R_{SS}(on)2	I_S=5A, V_{GS}=4.0V	Test Circuit 5	1.9	2.4	3.2	mΩ
	R_{SS}(on)3	I_S=5A, V_{GS}=3.8V	Test Circuit 5	2.0	2.6	3.2	mΩ
	R_{SS}(on)4	I_S=5A, V_{GS}=3.1V	Test Circuit 5	2.1	3.3	4.4	mΩ
	R_{SS}(on)5	I_S=5A, V_{GS}=2.5V	Test Circuit 5	2.7	4.0	6.3	mΩ
Turn-ON Delay Time	t_d(on)	V_{SS}=6V, V_{GS}=4.5V, I_S=3A	Test Circuit 6		80		ns
Rise Time	t_r				570		ns
Turn-OFF Delay Time	t_d(off)				38,000		ns
Fall Time	t_f				17,700		ns
Total Gate Charge	Qg	V_{SS}=6V, V_{GS}=4.5V, I_S=27A	Test Circuit 7		100		nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S=3A, V_{GS}=0V	Test Circuit 8		0.75	1.2	V

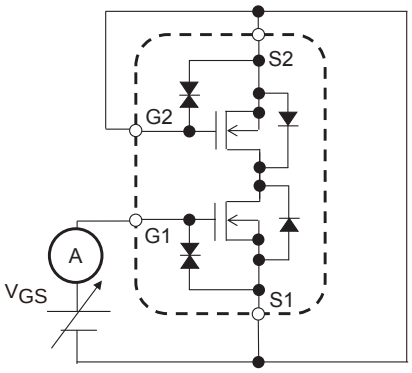
Note 2 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test circuits are example of measuring FET1 side

Test Circuit 1
V_{SSS} / I_{SSS}

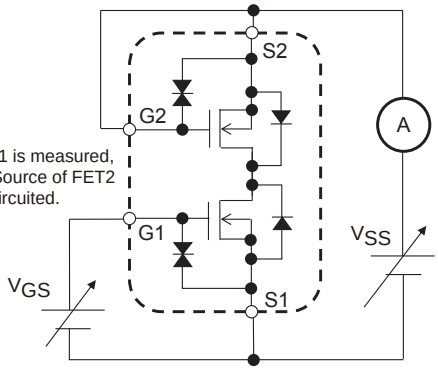


Test Circuit 2
I_{GSS}



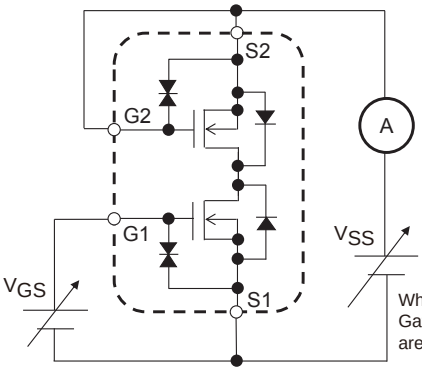
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS(th)}$



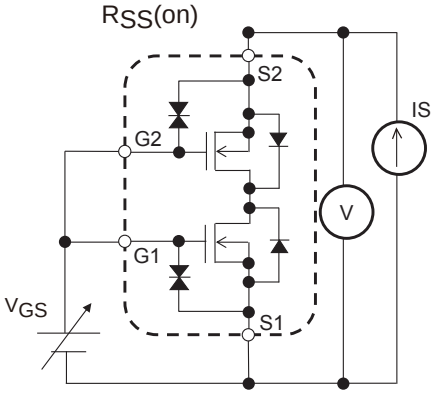
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
g_{FS}

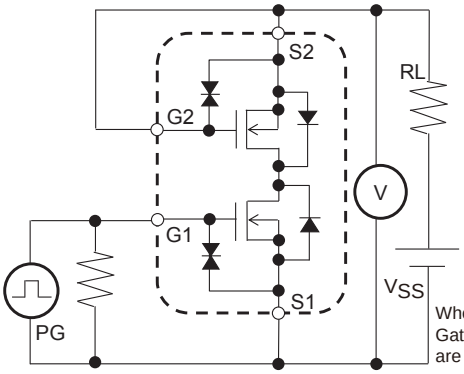


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
$R_{SS(on)}$

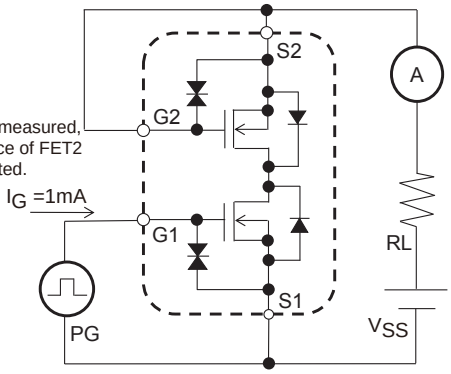


Test Circuit 6
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f



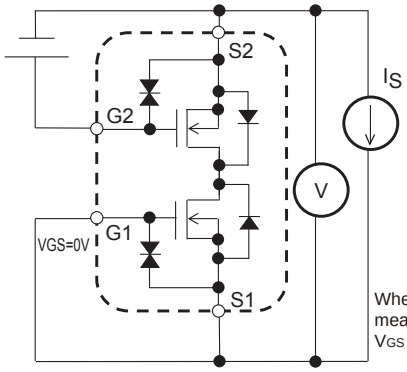
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 7
Qg



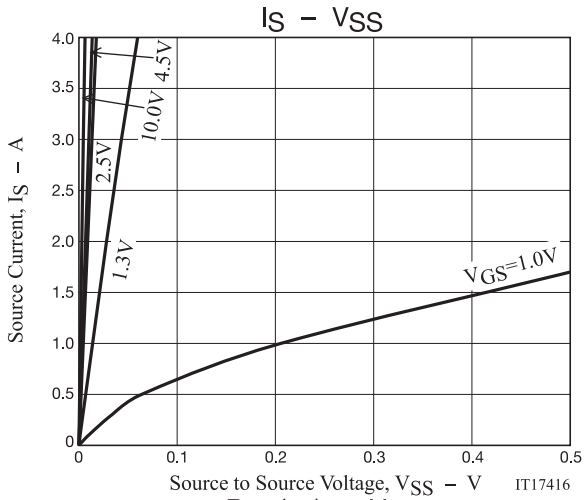
When FET1 is measured, Gate and Source of FET2 are short-circuited.

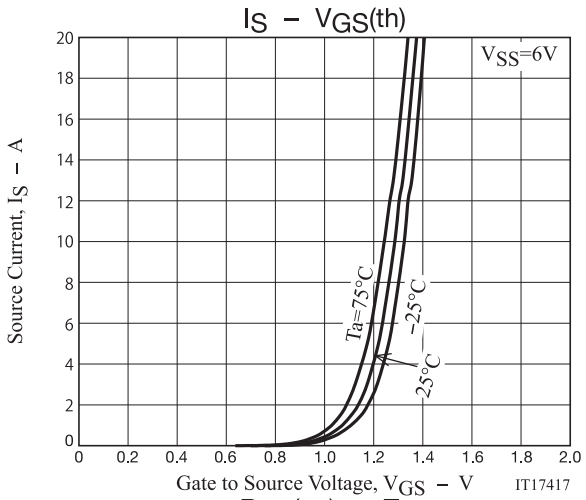
Test Circuit 8
$V_{F(S-S)}$

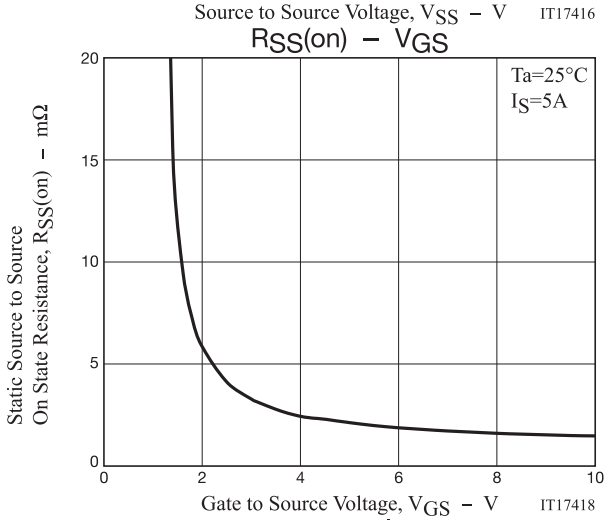


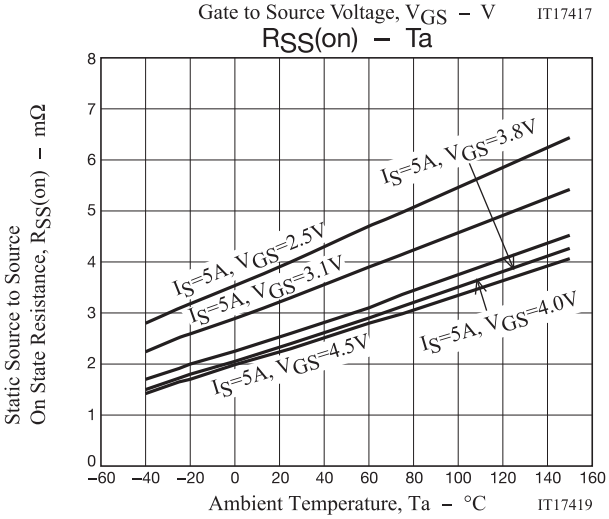
When FET1 is measured,+4.5V is added to V_{GS} of FET2.

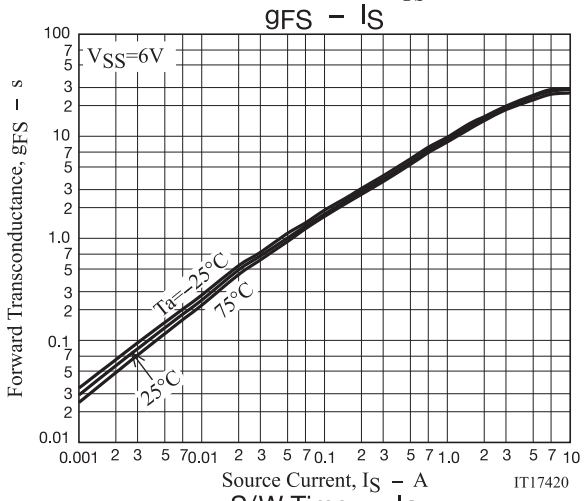
When FET2 is measured, the position of FET1 and FET2 is switched.

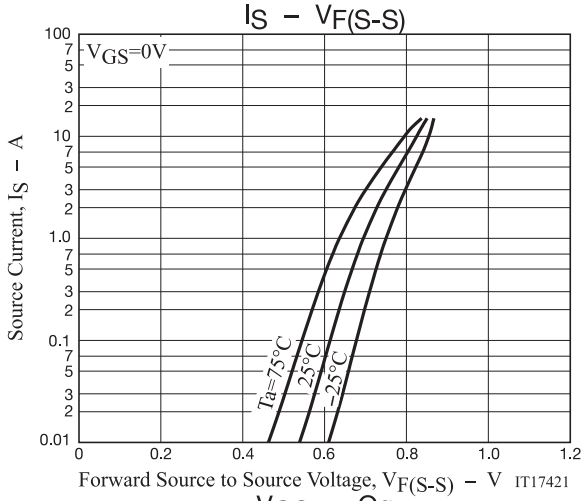


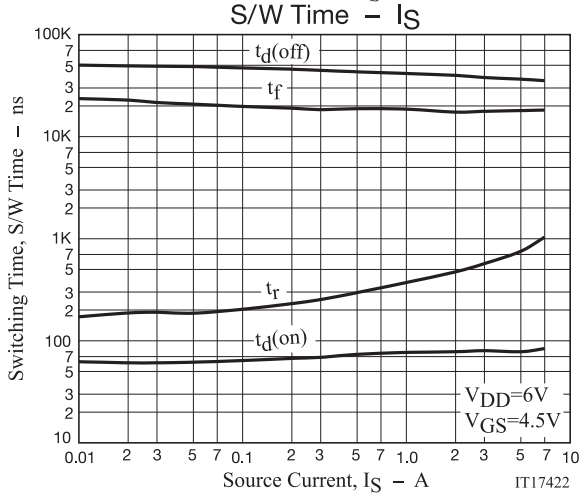


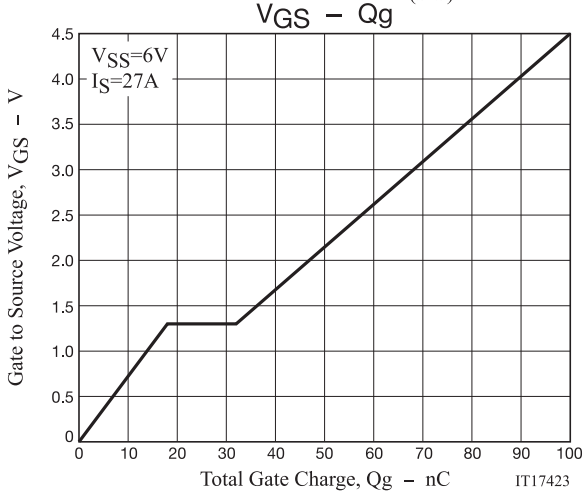


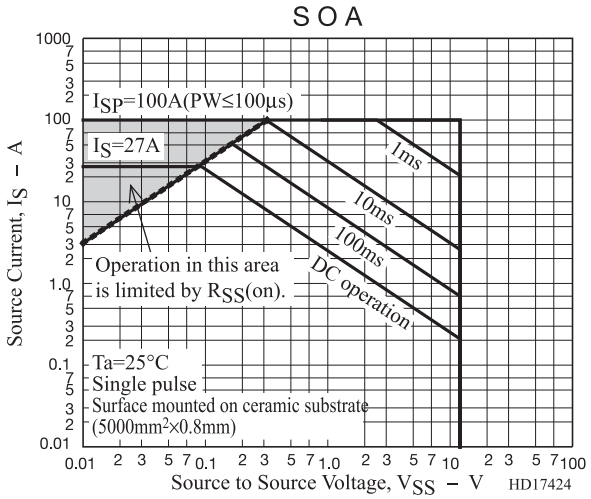


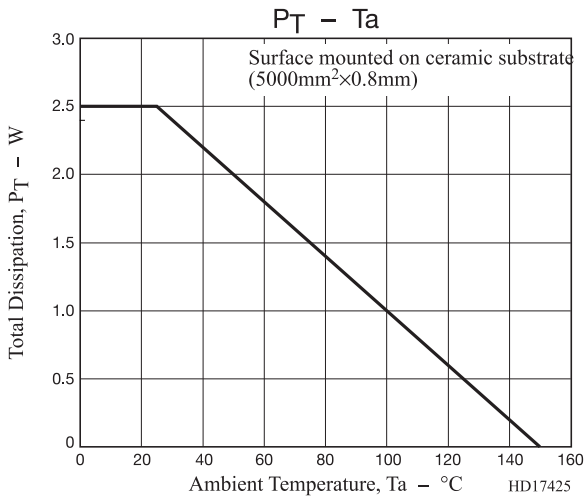


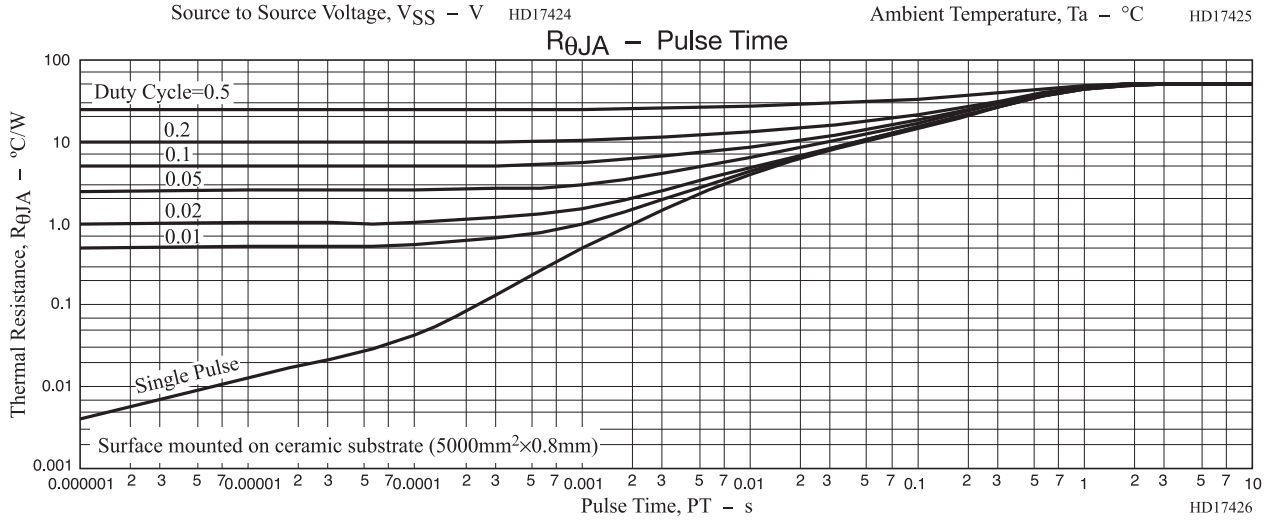










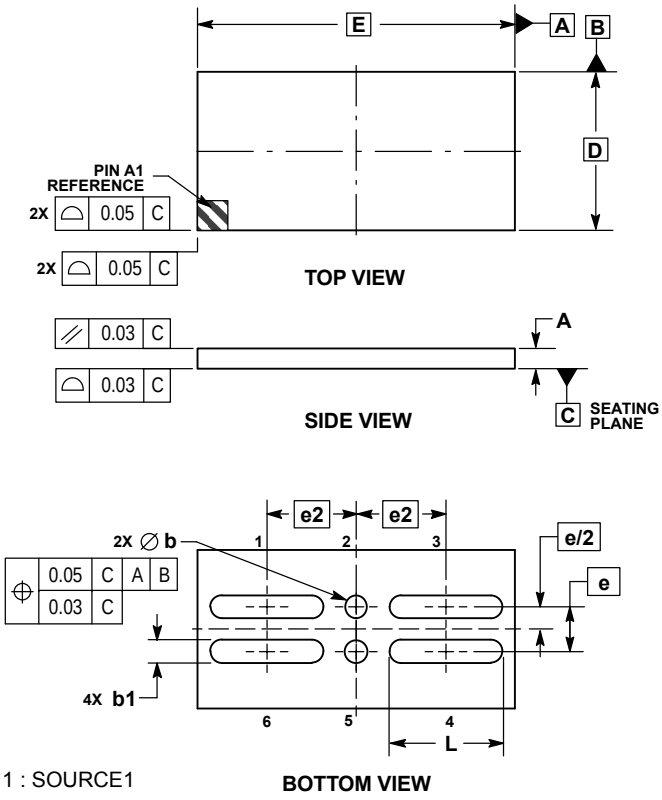


PACKAGE DIMENSIONS

unit : mm

CSP6, 1.77x3.54 / EFCP3517-6DGH-020

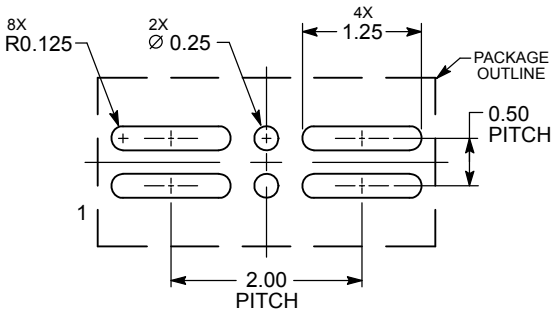
CASE 568AL
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS MIN	MAX
A	----	0.22
b	0.22	0.28
b1	0.22	0.28
D	1.77 BSC	
E	3.54 BSC	
e	0.50 BSC	
e2	1.00 BSC	
L	1.22	1.28

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

1 : SOURCE1
2 : GATE1
3 : SOURCE 1
4 : SOURCE 2
5 : GATE2
6 : SOURCE 2

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)
EFC6611R-TF	ML	CSP6, 1.77x3.54 / EFCP3517-6DGH-020 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the EFC6611R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.