

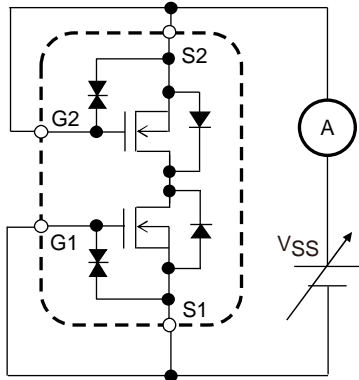
EFC4619R

Electrical Characteristics at Ta = 25°C

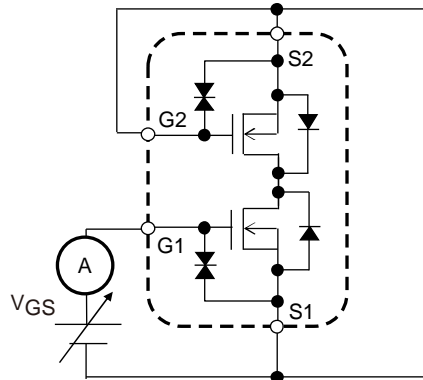
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Source to Source Breakdown Voltage	V(BR) _{SSS}	I _S =1mA, V _{GS} =0V Test Circuit 1	24			V
Zero-Gate Voltage Source Current	I _{SSS}	V _{SS} =20V, V _{GS} =0V Test Circuit 1			1	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{SS} =0V Test Circuit 2			±1	μA
Cutoff Voltage	V _{GS(off)}	V _{SS} =10V, I _S =1mA Test Circuit 3	0.5		1.3	V
Forward Transfer Admittance	y _{fs}	V _{SS} =10V, I _S =3A Test Circuit 4		5.8		S
Static Source to Source On-State Resistance	R _{SS(on)1}	I _S =3A, V _{GS} =4.5V Test Circuit 5	13.5	19.8	23	mΩ
	R _{SS(on)2}	I _S =3A, V _{GS} =4.0V Test Circuit 5	14	20.5	24	mΩ
	R _{SS(on)3}	I _S =3A, V _{GS} =3.7V Test Circuit 5	14.5	21	25.5	mΩ
	R _{SS(on)4}	I _S =3A, V _{GS} =3.1V Test Circuit 5	14.9	23	30	mΩ
	R _{SS(on)5}	I _S =3A, V _{GS} =2.5V Test Circuit 5	18.5	27	35	mΩ
Turn-ON Delay Time	t _{d(on)}	V _{SS} =10V, V _{GS} =4.5V, I _S =3A Test Circuit 7		340		ns
Rise Time	t _r			440		ns
Turn-OFF Delay Time	t _{d(off)}			24400		ns
Fall Time	t _f			22400		ns
Total Gate Charge	Q _g		V _{SS} =10V, V _{GS} =4.5V, I _S =6A Test Circuit 8		21.7	
Forward Source to Source Voltage	V _{F(S-S)}	I _S =3A, V _{GS} =0V Test Circuit 6		0.8	1.2	V

Test circuits are example of measuring FET1 side

Test Circuit 1
I_{SSS}

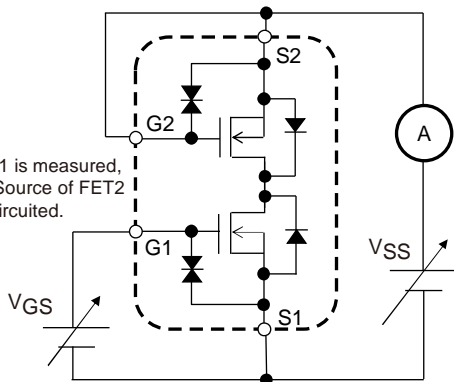


Test Circuit 2
I_{GSS}



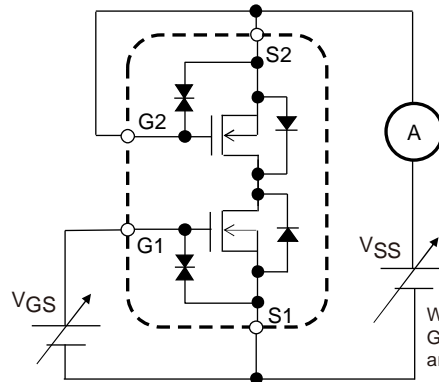
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
V_{GS(off)}



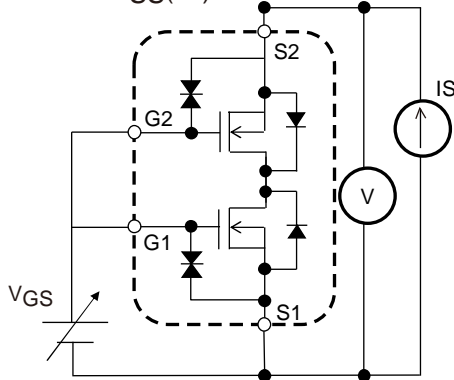
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
|y_{fs}|

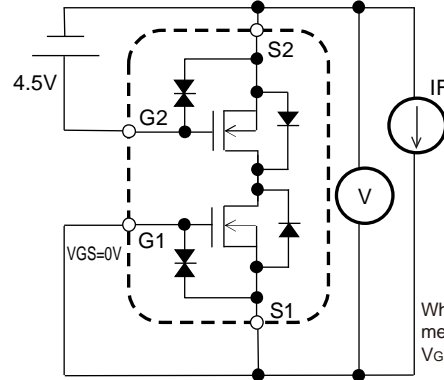


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
R_{SS(on)}

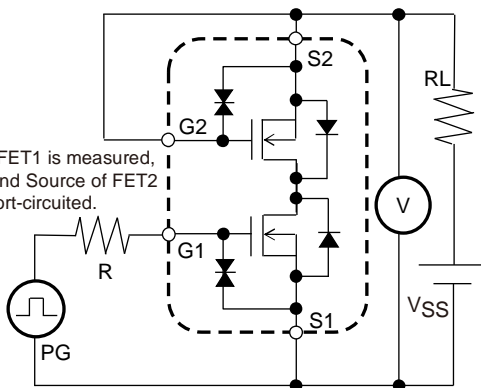


Test Circuit 6
V_{F(S-S)}



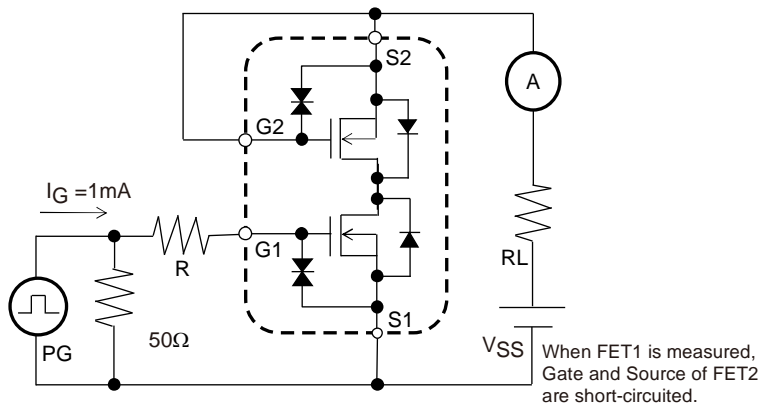
When FET1 is measured, +4.5V is added to V_{GS} of FET2.

Test Circuit 7
t_{d(on)}, t_r, t_{d(off)}, t_f



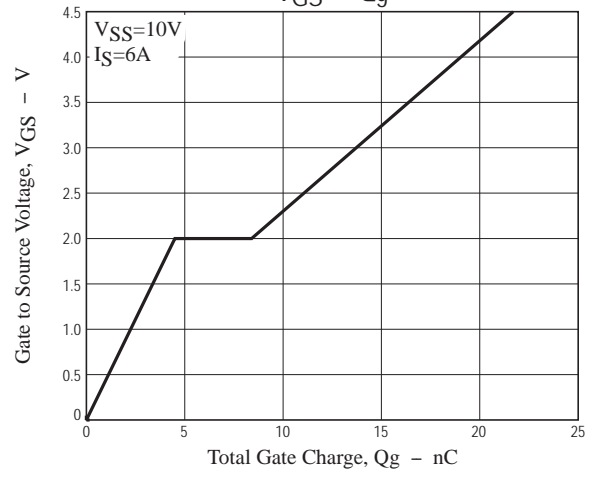
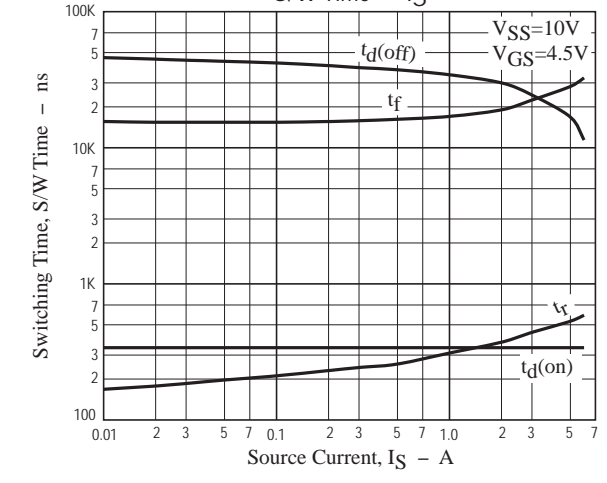
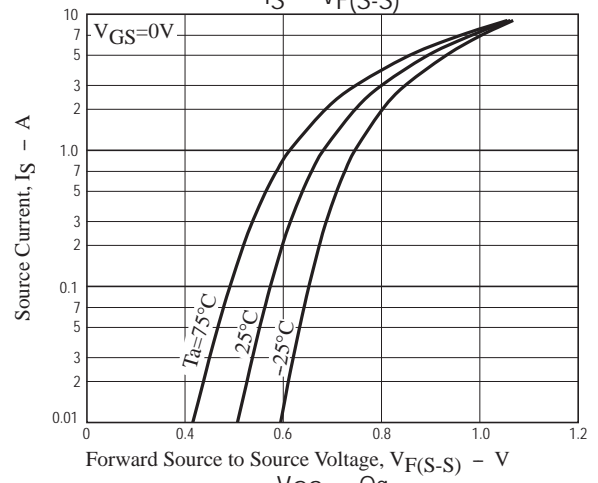
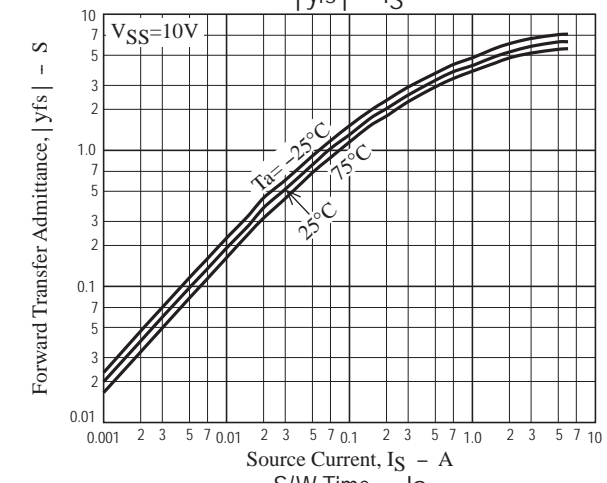
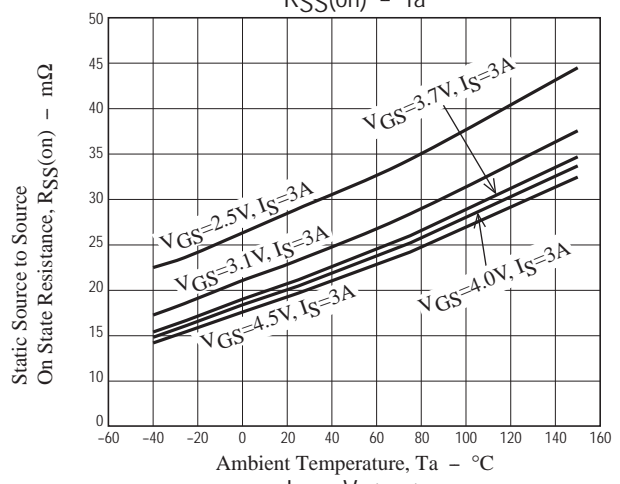
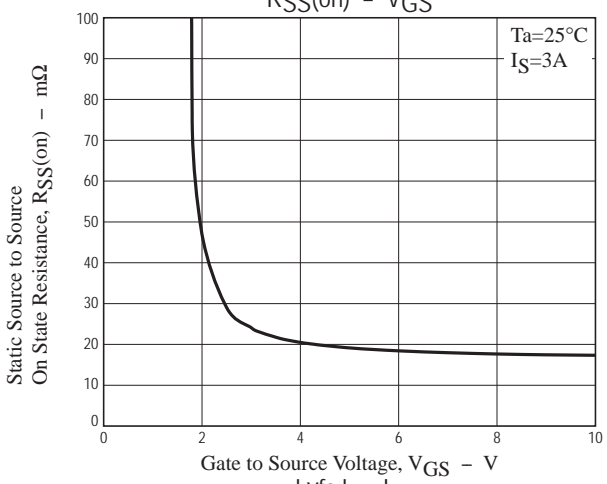
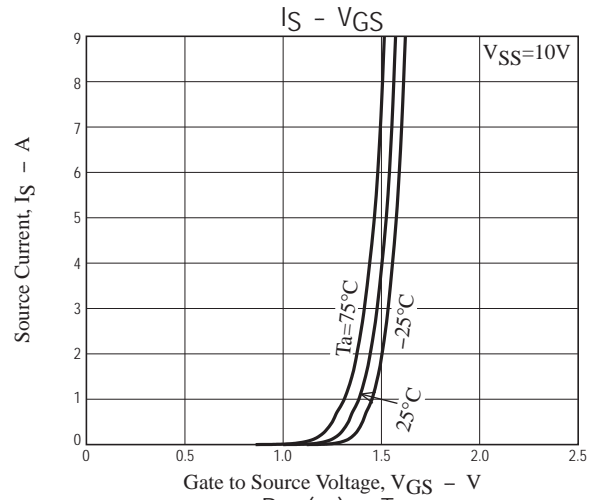
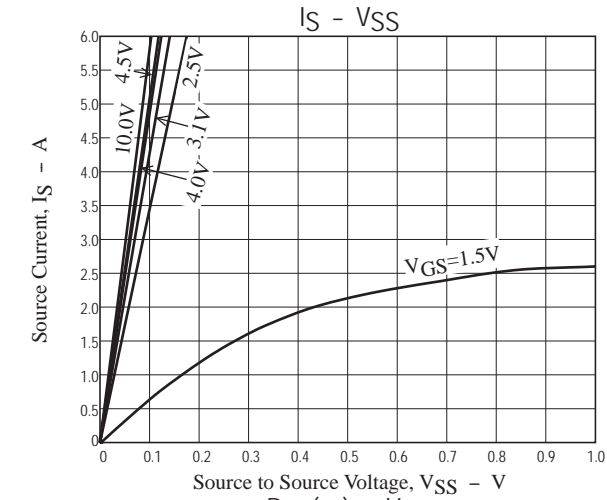
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 8
Q_g

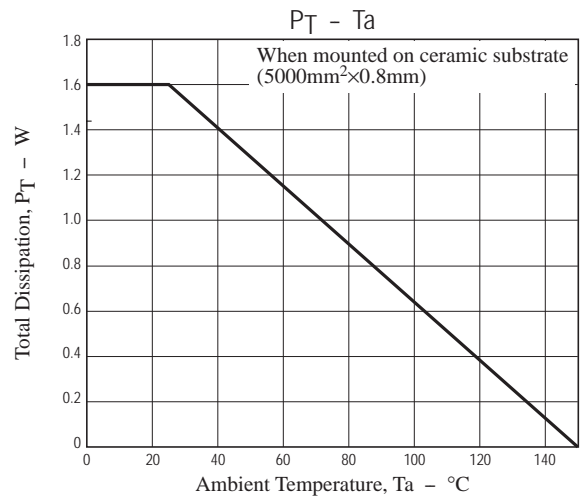
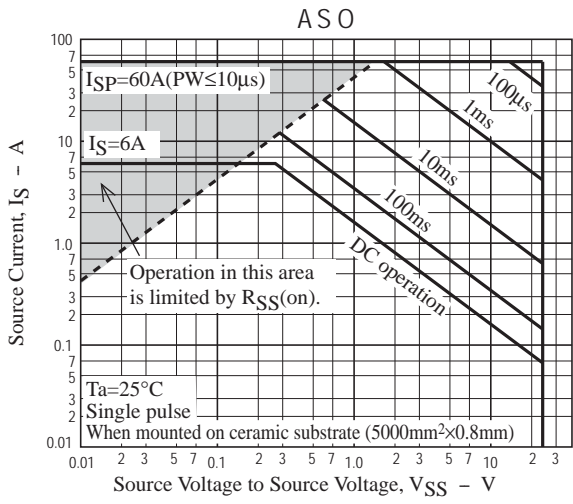


When FET1 is measured, Gate and Source of FET2 are short-circuited.

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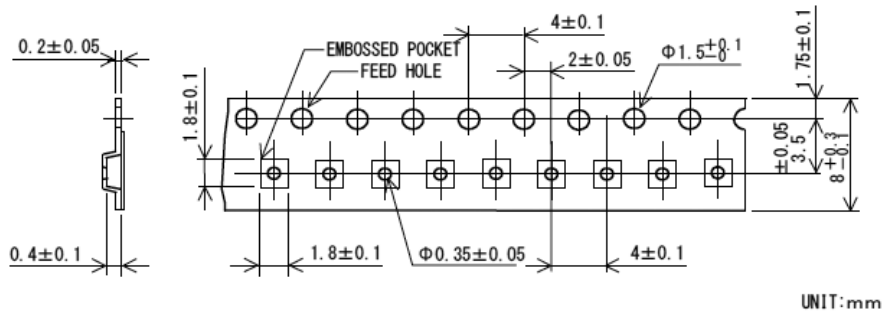
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Taping Specification

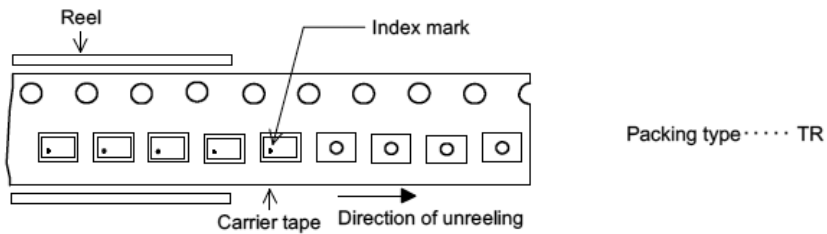
EFC4619R-TR

1. Taping Configuration

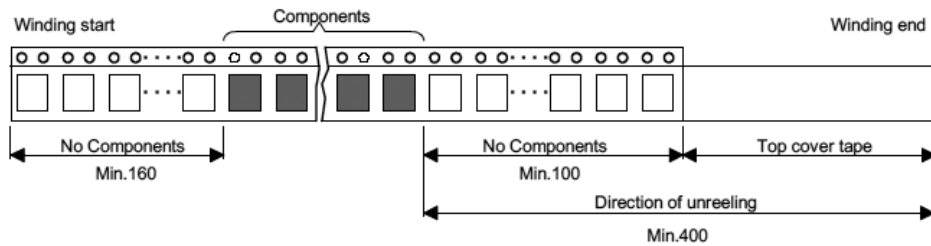
1-1. Carrier Tape Size (unit:mm)



1-2. Device Placement Direction



1-3. Leader portion and Trailer portion (unit:mm)



EFC4619R

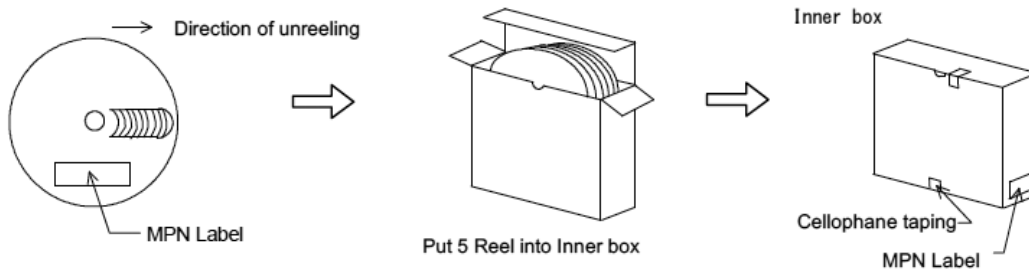
Packing Format

Carrier Tape code	Package code	Maximum Number of devices contained. (pcs.)			Packing Format	
		Reel	Inner box		Inner box BOX(C-1)	
1818X04	EFCP1616-4CE-022	5,000	25,000		5reels contained. Dimensions:mm 183×72×185	

MPN Label



Packing Method

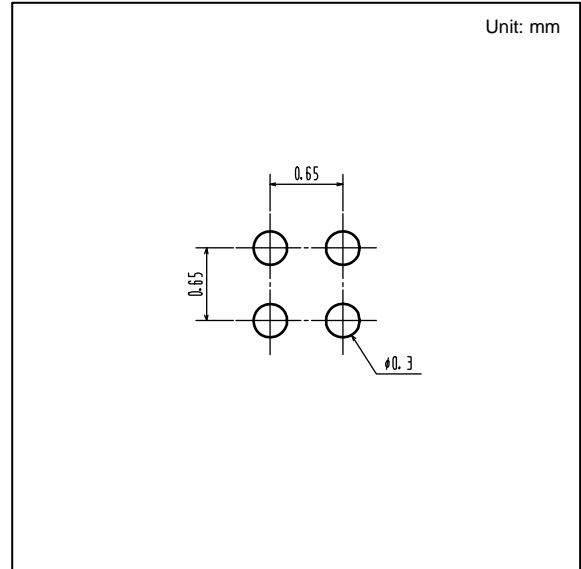
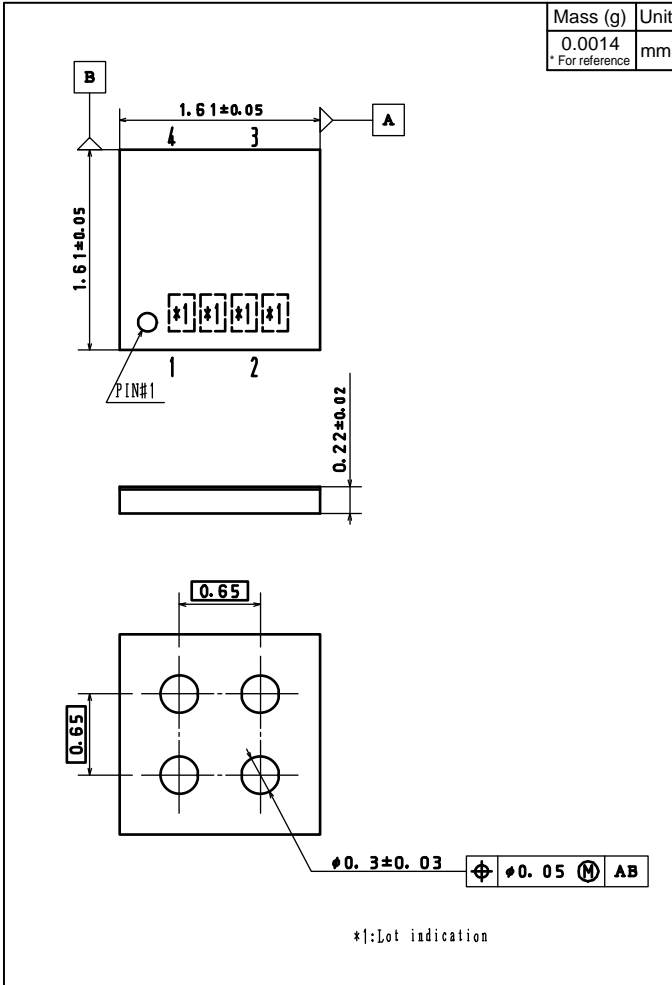


EFC4619R

Outline Drawing

EFC4619R-TR

Land Pattern Example



Note on usage : Since the EFC4619R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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