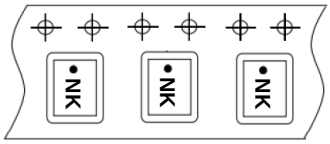
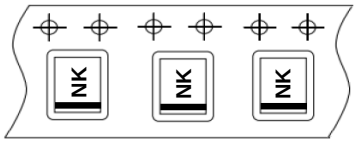
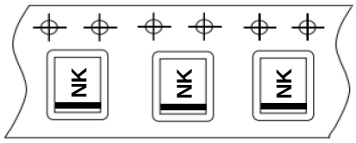
Marking Information

DMN62D0LFB-7	 Top View Dot Denotes Drain Side From date code 1527 (YYWW), this changes to:  Top View Bar Denotes Gate and Source Side  
DMN62D0LFB-7B	 Top View Bar Denotes Gate and Source Side NK = Part Marking Code 

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = 4.0V	Steady State	T_A = +25°C T_A = +70°C	I_D	320 75	mA
Pulsed Drain Current (Note 6)			I_{DM}	1	A

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 5)	P_D	0.5	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 5)	$R_{\theta JA}$	258	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
6. Repetitive rating, pulse width limited by junction temperature.

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Electrical Characteristics (@ T_A = +25°C, unless otherwise stated.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	μA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±5V, V_{DS} = 0V
		—	—	±500	nA	V_{GS} = ±10V, V_{DS} = 0V
		—	—	±2.0	μA	V_{GS} = ±15V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.6	—	1.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	1.3	2	Ω	V_{GS} = 4V, I_D = 100mA
		—	1.5	2.5		V_{GS} = 2.5V, I_D = 50mA
		—	1.9	3		V_{GS} = 1.8V, I_D = 50mA
		—	2.6	—		V_{GS} = 1.5V, I_D = 10mA
Forward Transfer Admittance	$\|Y_{fs}\|$	—	0.8	—	S	V_{DS} = 10V, I_D = 200mA
Diode Forward Voltage	V_{SD}	—	0.9	1.3	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	32	64	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	4.4	9		
Reverse Transfer Capacitance	C_{rss}	—	2.9	6		
Gate Resistance	R_g	—	126	250	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	0.45	0.9	nC	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 250mA
Gate-Source Charge	Q_{gs}	—	0.08	0.2		
Gate-Drain Charge	Q_{gd}	—	0.08	0.2		
Turn-On Delay Time	$t_{D(ON)}$	—	3.4	10	ns	V_{GS} = 10V, V_{DS} = 30V, R_L = 150Ω, R_g = 25Ω, I_D = 200mA
Turn-On Rise Time	t_R	—	3.4	10	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	26.4	45	ns	
Turn-Off Fall Time	t_F	—	16.3	30	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

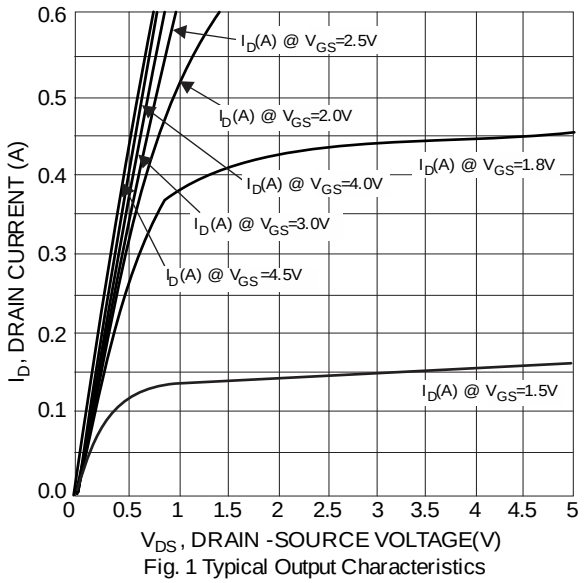

Fig. 1 Typical Output Characteristics

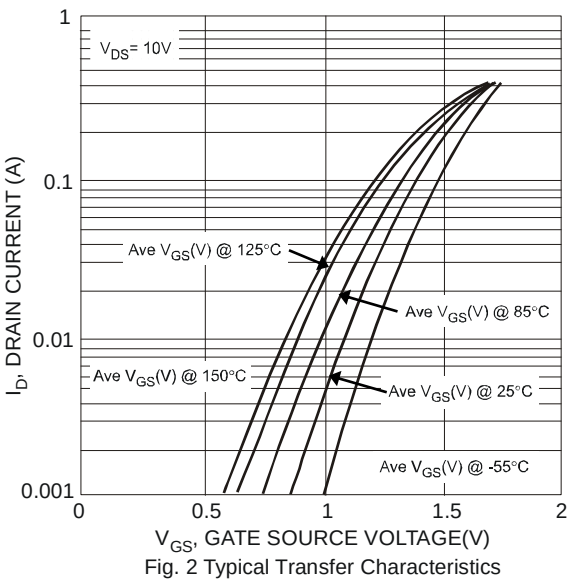

Fig. 2 Typical Transfer Characteristics

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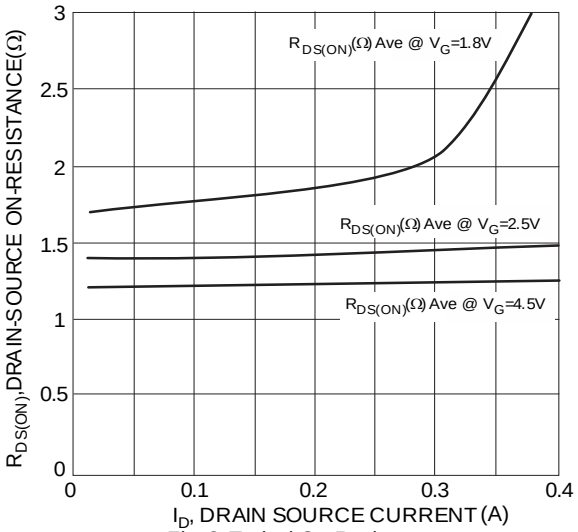

Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

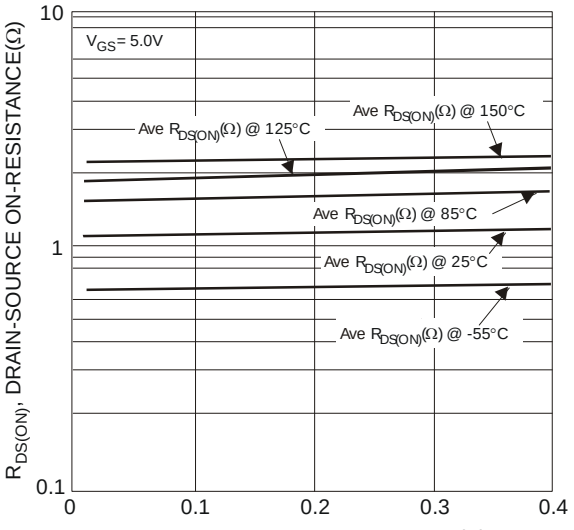

Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

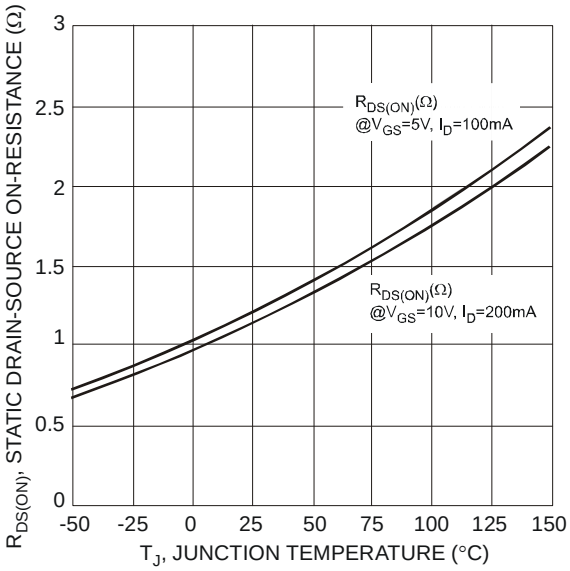

Fig. 5 On-Resistance Variation with Temperature

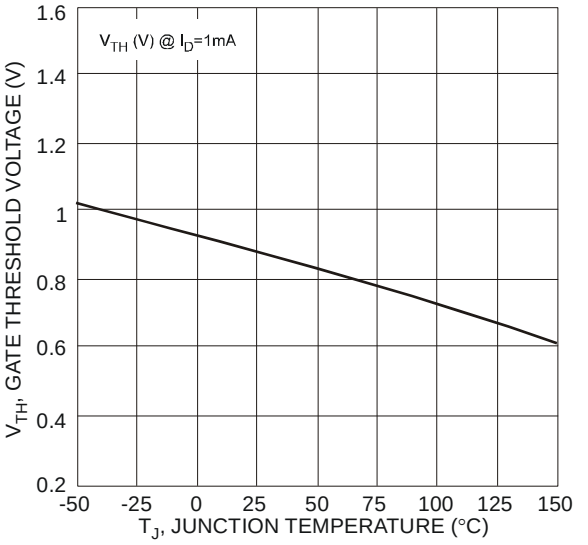

Fig. 6 Gate Threshold Variation vs. Junction Temperature

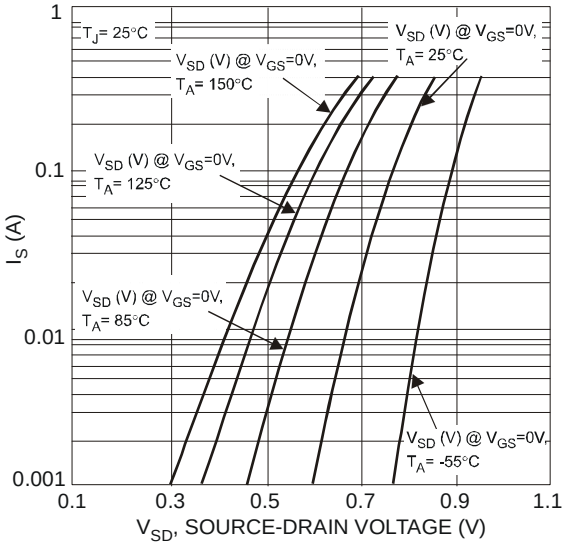

Fig. 7 Diodes Forward Voltage vs. Current

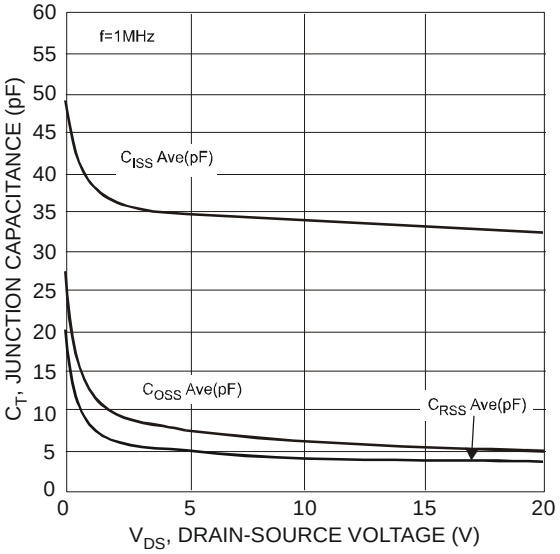

Fig. 8 Typical Junction Capacitance

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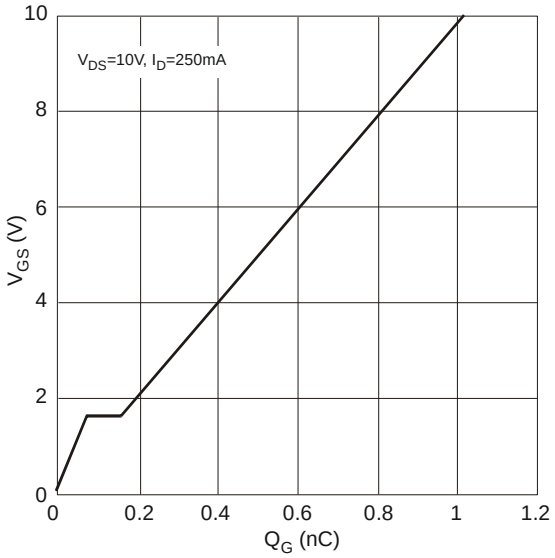

Fig. 9 Gate Charge Characteristics

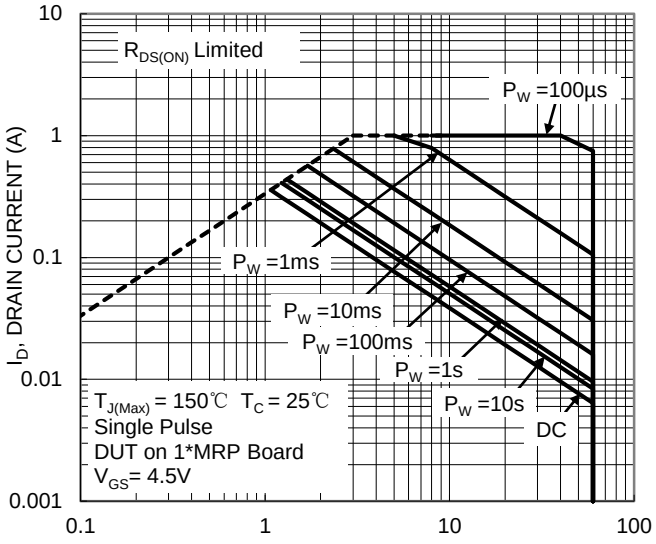

Fig.10 SOA, Safe Operation Area

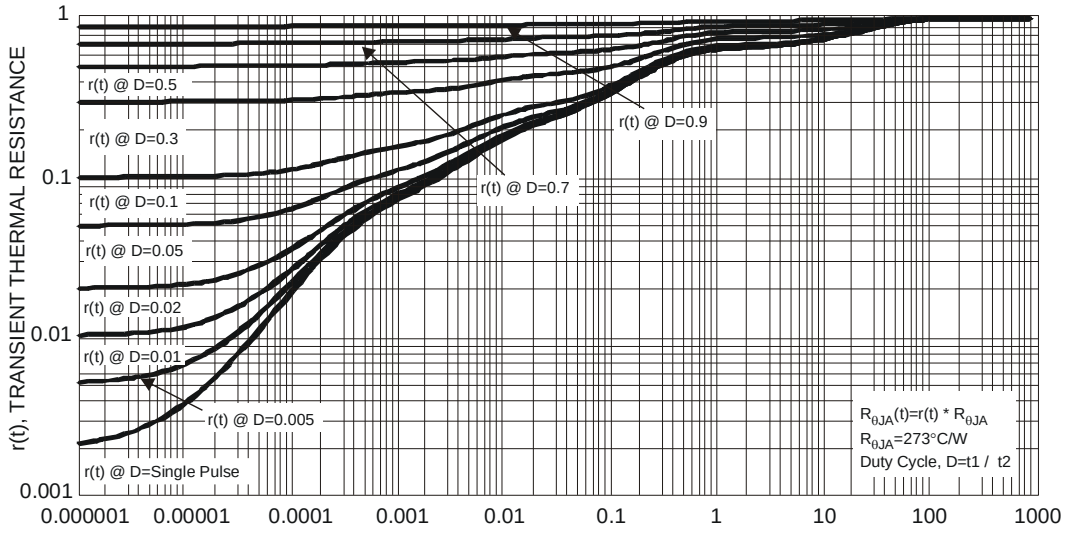

Fig. 11 Transient Thermal Resistance

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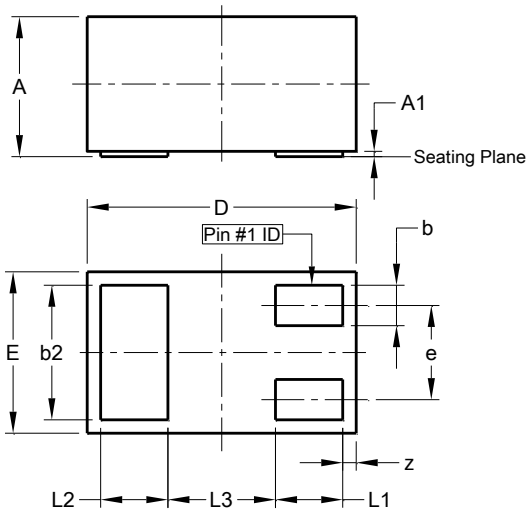
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1006-3

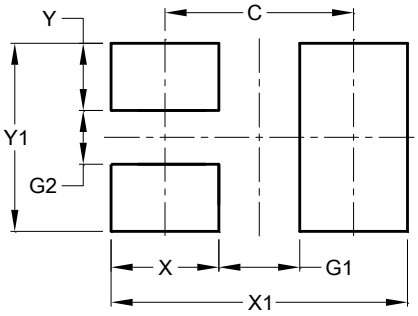


X1-DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1006-3



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

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