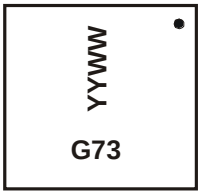
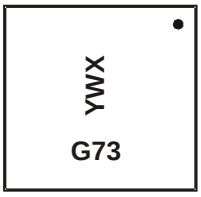
Marking Information

Site1



G73 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 21 = 2021)
WW = Week Code (01 to 53)

Site 2



G73 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 1 = 2021)
W = Week (ex: A = Week 27; Z Represents Week 52 And 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2011	…	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	1	…	1	2	3	4	5	6	7	8	9	0

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	10.5 8.5	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	14 11	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	90	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	3.0	A
Avalanche Current (Note 7) L = 0.1mH			I_{AR}	22	A
Repetitive Avalanche Energy (Note 7) L = 0.1mH			E_{AR}	24	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	Steady State	P_D	0.9	W
	t<10s		1.5	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	142	°C/W
	t<10s		78	
Total Power Dissipation (Note 6)	Steady State	P_D	2.2	W
	t<10s		3.5	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	59	°C/W
	t<10s		33	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	11	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. I_{AR} and E_{AR} ratings are based on low frequency and duty cycles to keep T_J = +25°C.

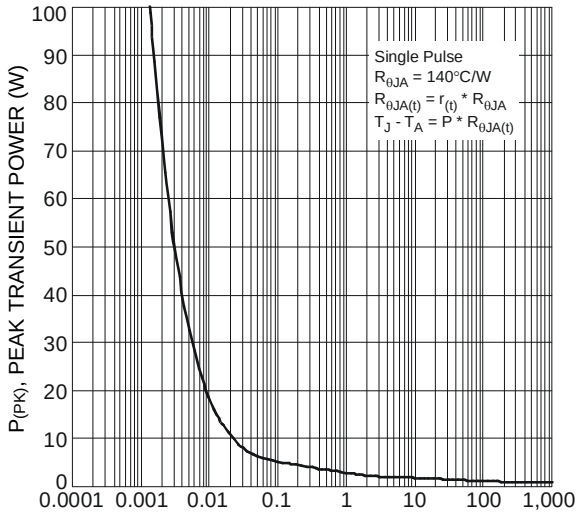


Fig. 1 Single Pulse Maximum Power Dissipation

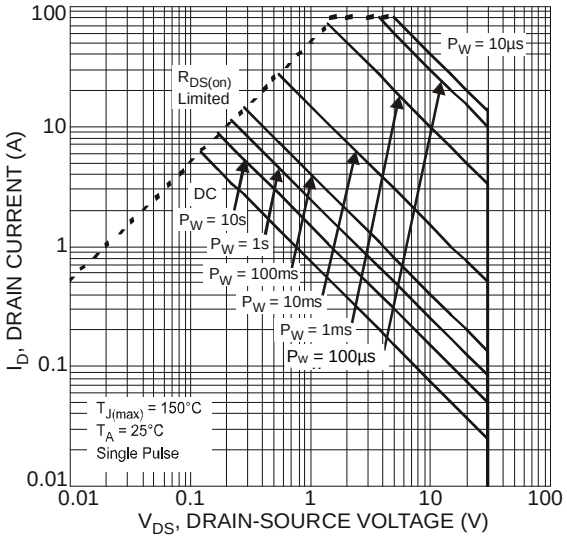


Fig. 2 SOA, Safe Operation Area

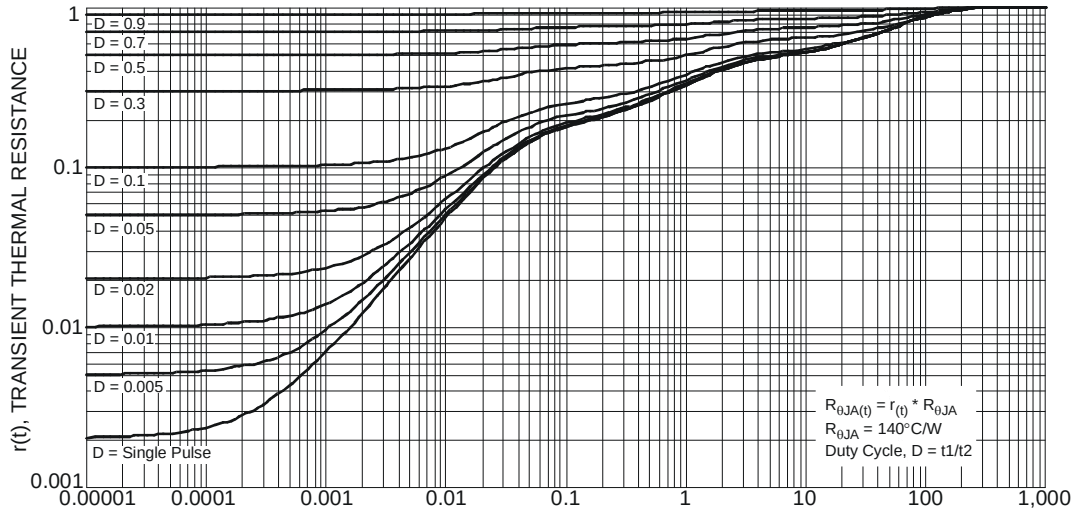


Fig. 3 Transient Thermal Resistance

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.4	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	7	11	mΩ	V_{GS} = 10V, I_D = 20A
		—	11	15		V_{GS} = 4.5V, I_D = 20A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	74	—	S	V_{DS} = 5V, I_D = 20A
Diode Forward Voltage	V_{SD}	—	0.75	1.0	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1281	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	145	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	125	—	pF	
Gate Resistance	R_g	—	1.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	12.5	—	nC	V_{DS} = 15V, I_D = 12A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	26.7	—	nC	
Gate-Source Charge	Q_{gs}	—	3.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	4.4	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.2	—	ns	V_{DD} = 15V, V_{GS} = 10V, R_L = 1.25Ω, R_G = 3Ω
Turn-On Rise Time	t_R	—	21.2	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	22.3	—	ns	
Turn-Off Fall Time	t_F	—	5.1	—	ns	
Reverse Recovery Time	t_{RR}	—	8.5	—	ns	I_F = 12A, di/dt = 500A/μs
Reverse Recovery Charge	Q_{RR}	—	7.0	—	nC	I_F = 12A, di/dt = 500A/μs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

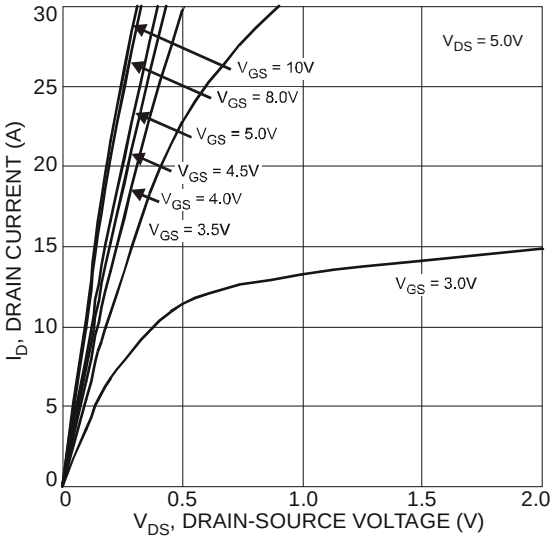


Fig.4 Typical Output Characteristic

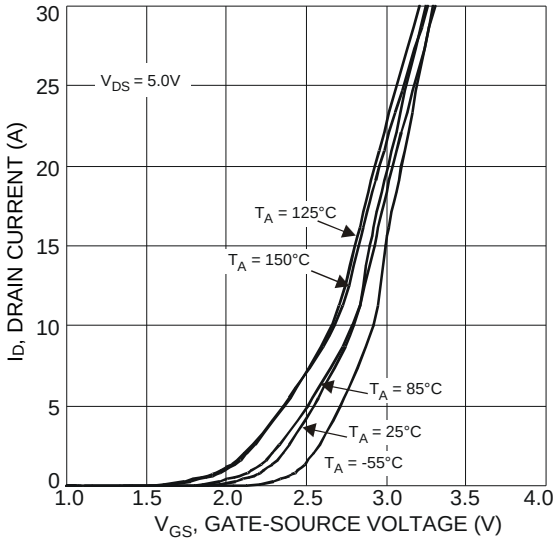


Fig. 5 Typical Transfer Characteristics

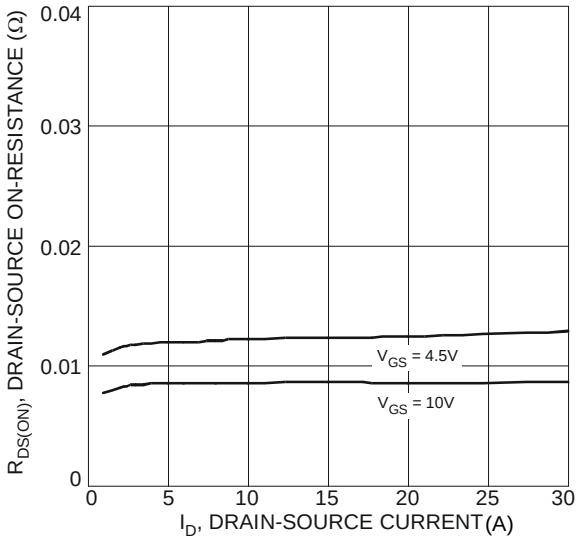


Fig. 6 Typical On-Resistance vs. Drain Current and Gate Voltage

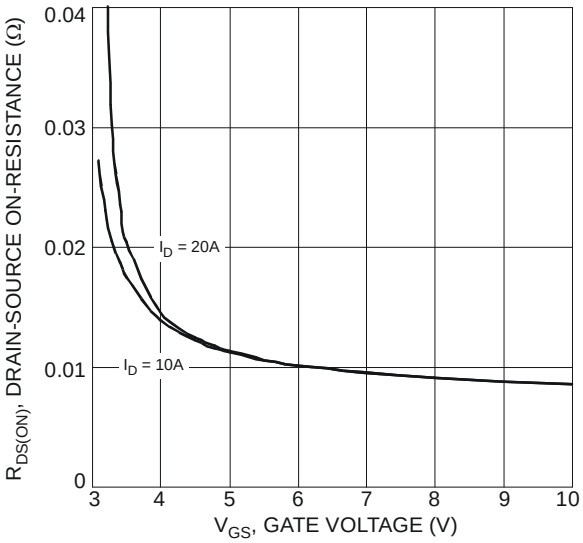


Fig. 7 Typical On-Resistance vs. Gate Voltage

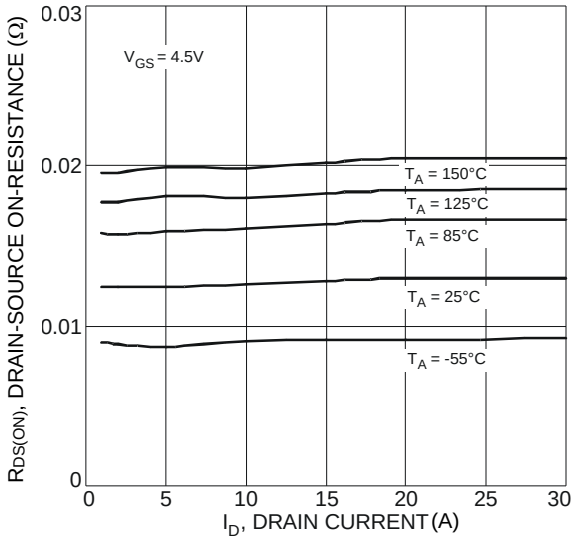


Fig. 8 Typical On-Resistance vs. Drain Current and Temperature

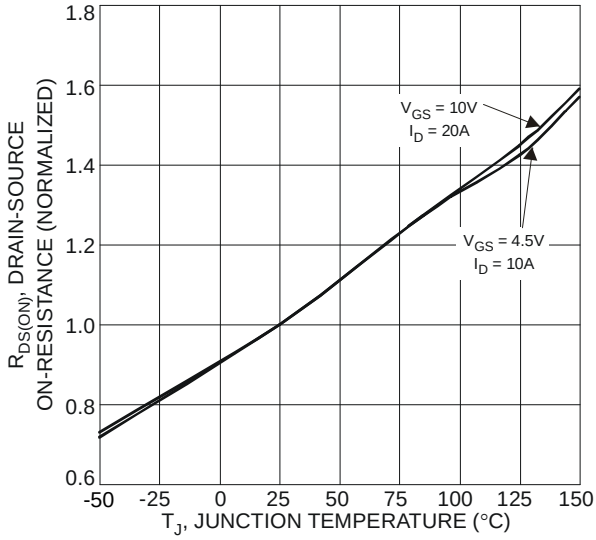


Fig. 9 On-Resistance Variation with Temperature

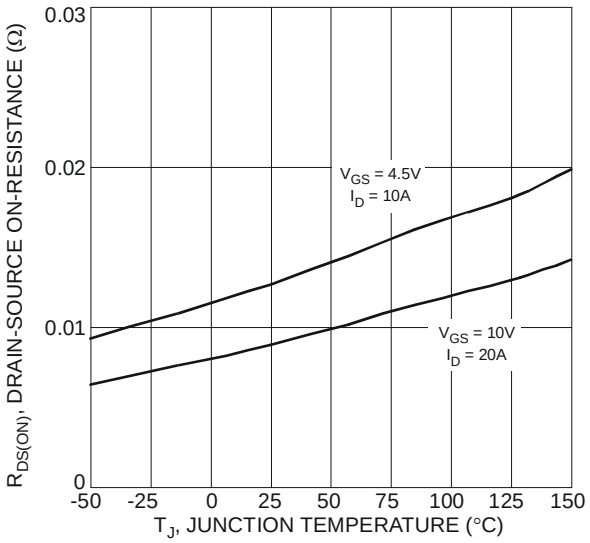


Fig. 10 On-Resistance Variation with Temperature

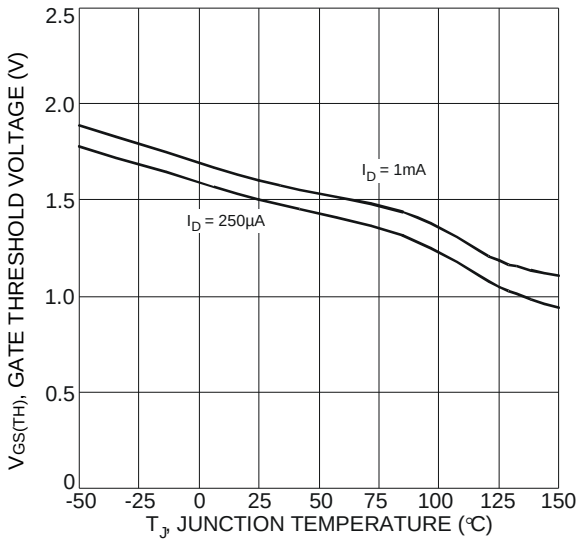


Fig. 11 Gate Threshold Variation vs. Junction Temperature

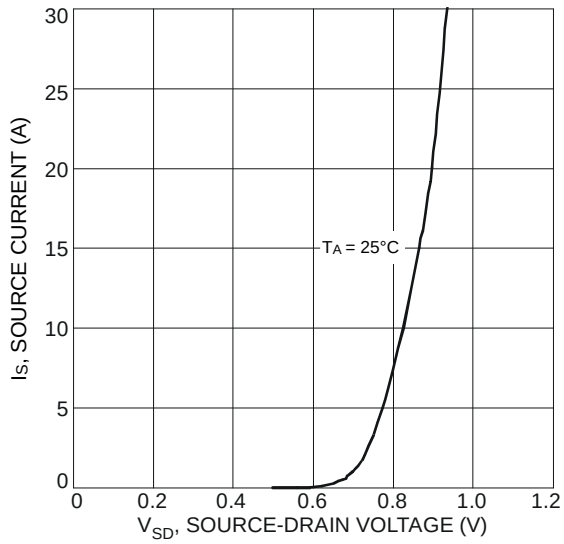


Fig.12 Diode Forward Voltage vs. Current

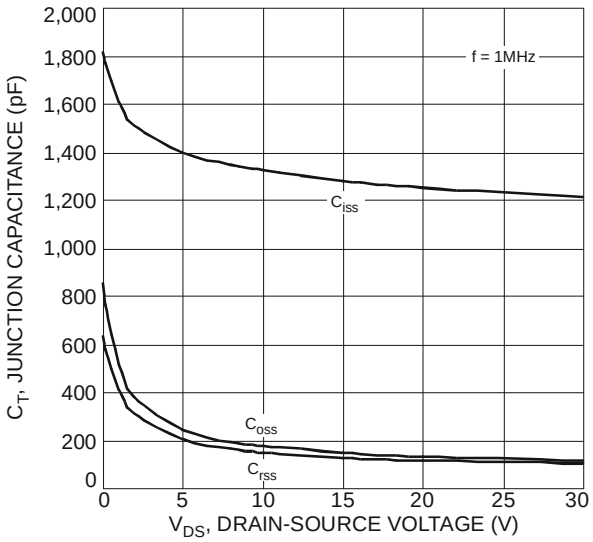


Fig. 13 Typical Junction Capacitance

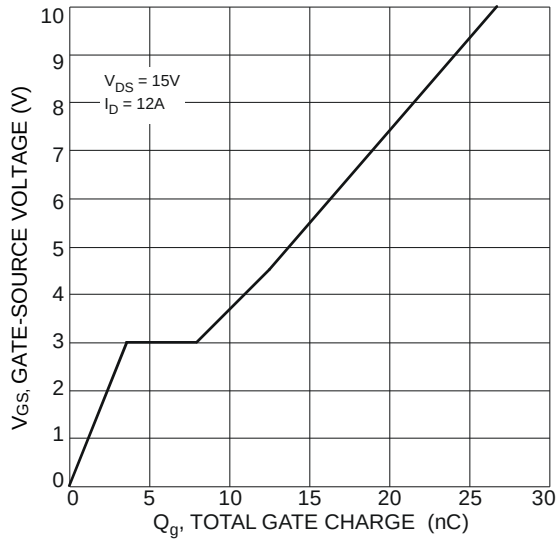
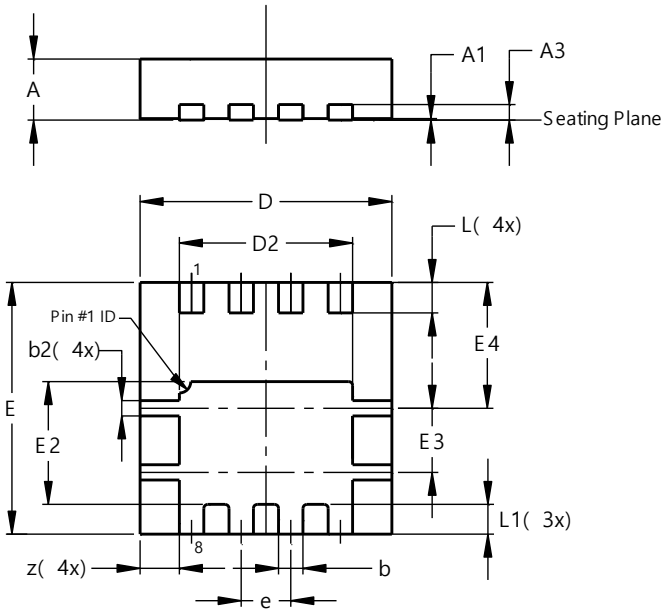


Fig. 14 Gate Charge

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8

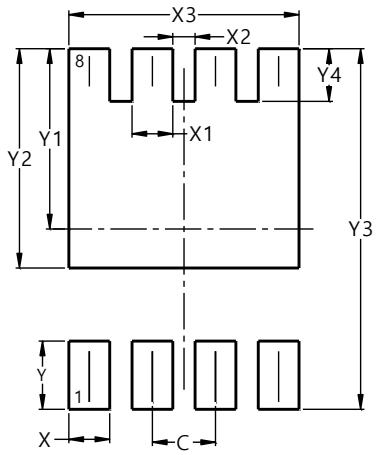


PowerDI3333-8			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	–	–	0.203
b	0.27	0.37	0.32
b2	0.15	0.25	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
E4	1.60	1.70	1.65
e	–	–	0.65
L	0.35	0.45	0.40
L1	–	–	0.39
z	–	–	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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