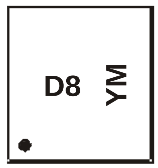
Marking Information

Site 1



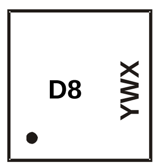
D8 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

Date Code Key

Year	2014	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	B	…	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2



D8 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 0 = 2020)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2014	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	4	…	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1 N-CHANNEL	Q2 P-CHANNEL	Unit
Drain-Source Voltage			V_{DSS}	12	-20	V
Gate-Source Voltage			V_{GSS}	±8	±8	V
Continuous Drain Current (Note 5) N-Channel: V_{GS} = 4.5V P-Channel: V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	6.0 4.8	-3.4 -2.7	A
	t < 5s	T_A = +25°C T_A = +70°C	I_D	7.1 5.7	-4.0 -3.2	A
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	1.4	-1.4	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	40	-20	A
Avalanche Current L = 0.1mH			I_{AS}	12	-12	A
Avalanche Energy L = 0.1mH			E_{AS}	8.4	7.5	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	Steady State	P_D	1.36	W
	t < 5s		1.89	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	92	°C/W
	t < 5s		66	
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	19	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Note: 5. Device mounted on 1” × 1” FR-4 PCB with high coverage 2oz. Copper, single sided.

Electrical Characteristics Q1 N-CHANNEL (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	12	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	µA	V_{DS} = 12V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	—	1	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	17	25	mΩ	V_{GS} = 4.5V, I_D = 5.2A
		—	19	30		V_{GS} = 3.3V, I_D = 5.0A
		—	21	32		V_{GS} = 2.5V, I_D = 4.8A
		—	30	40		V_{GS} = 1.8V, I_D = 2.5A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	787	—	pF	V_{DS} = 6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	203	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	177	—	pF	
Gate Resistance	R_g	—	4.8	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 3.3V)	Q_g	—	7.9	—	nC	V_{DS} = 6V, I_D = 6.8A
Total Gate Charge (V_{GS} = 4.5V)		—	10.5	—	nC	
Total Gate Charge (V_{GS} = 8V)		—	18.5	—	nC	
Gate-Source Charge	Q_{gs}	—	1.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.9	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.6	—	ns	V_{DD} = 6V, V_{GS} = 4.5V, R_L = 1.1Ω, R_G = 1Ω
Turn-On Rise Time	t_R	—	9.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	15.7	—	ns	
Turn-Off Fall Time	t_F	—	3.7	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	12.0	—	ns	I_S = 5.4A, dI/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	1.8	—	nC	I_S = 5.4A, dI/dt = 100A/µs

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to product testing.

Electrical Characteristics Q2 P-CHANNEL (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1.0	μA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.4	—	-1	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	55	80	mΩ	V_{GS} = -4.5V, I_D = -3.8A
		—	63	90		V_{GS} = -3.3V, I_D = -3.5A
		—	70	100		V_{GS} = -2.5V, I_D = -3.3A
		—	88	140		V_{GS} = -1.8V, I_D = -1.0A
		—	110	210		V_{GS} = -1.5V, I_D = -0.5A
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	576	—	pF	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	87	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	71	—	pF	
Gate Resistance	R_g	—	15	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -3.3V)	Q_g	—	5.2	—	nC	V_{DS} = -10V, I_D = -4.9A
Total Gate Charge (V_{GS} = -4.5V)		—	6.7	—	nC	
Total Gate Charge (V_{GS} = -8V)		—	11.5	—	nC	
Gate-Source Charge	Q_{gs}	—	1.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.0	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.5	—	ns	V_{DD} = -10V, V_{GS} = -4.5V, R_L = 2.6Ω, R_G = 1Ω
Turn-On Rise Time	t_R	—	3.6	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	20.8	—	ns	
Turn-Off Fall Time	t_F	—	12.7	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	13.1	—	ns	I_S = -3.9A, dI/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q_{RR}	—	3.9	—	nC	I_S = -3.9A, dI/dt = 100A/μs

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to product testing.

Typical Characteristics - N-CHANNEL

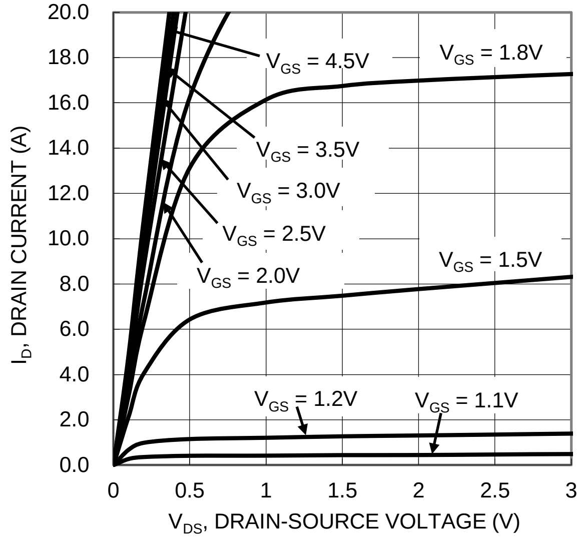


Figure 1 Typical Output Characteristic

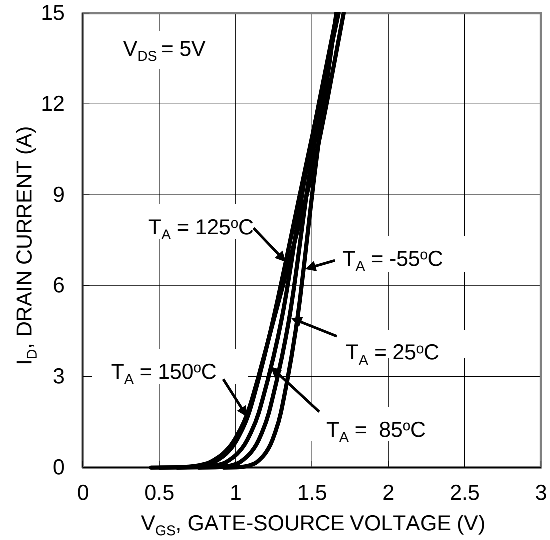


Figure 2 Typical Transfer Characteristic

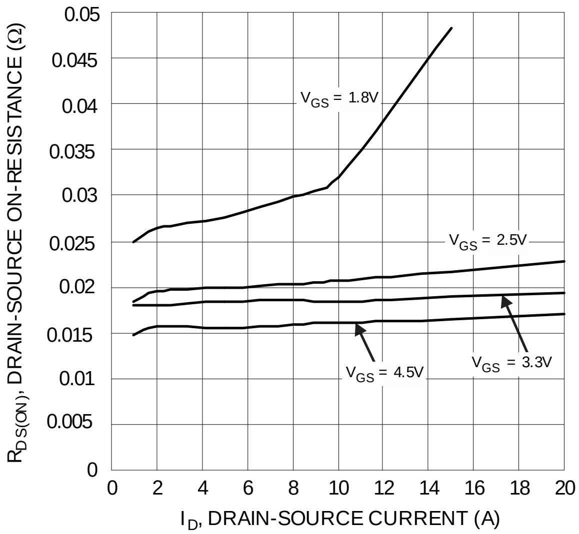


Figure 3 Typical On-Resistance vs.
Drain Current and Gate Voltage

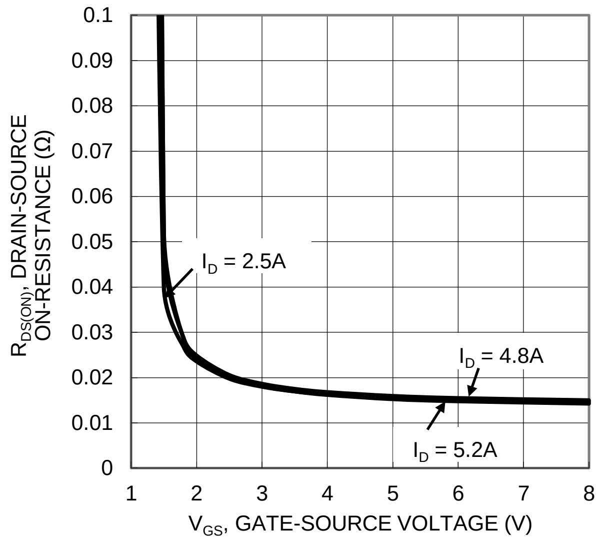


Figure 4 Typical Transfer Characteristic

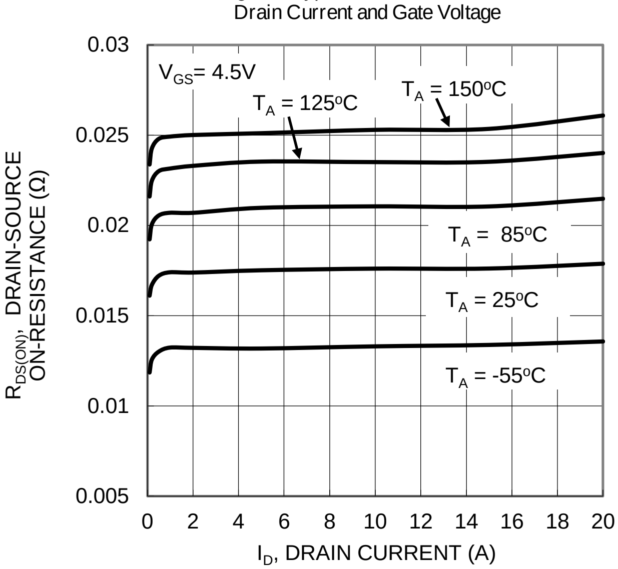


Figure 5 Typical On-Resistance vs. Drain Current
and Temperature

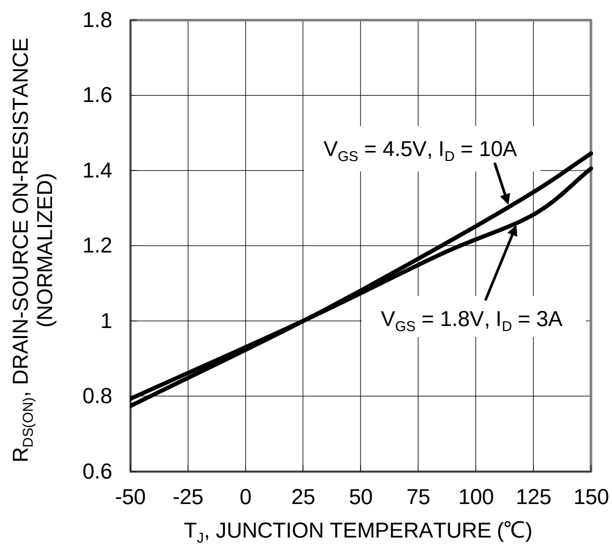


Figure 6 On-Resistance Variation with
Temperature

Typical Characteristics - N-CHANNEL (continued)

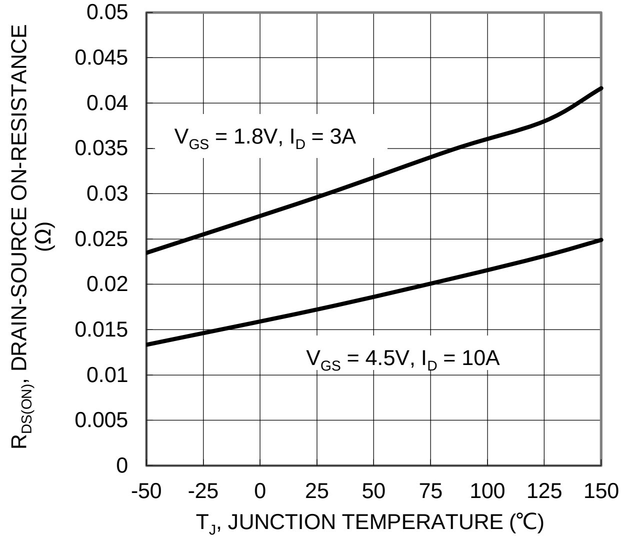


Figure 7 On-Resistance Variation with Temperature

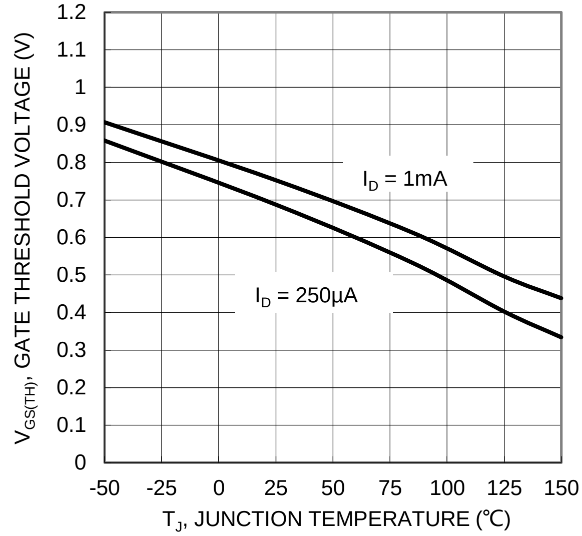


Figure 8 Gate Threshold Variation vs. Junction Temperature

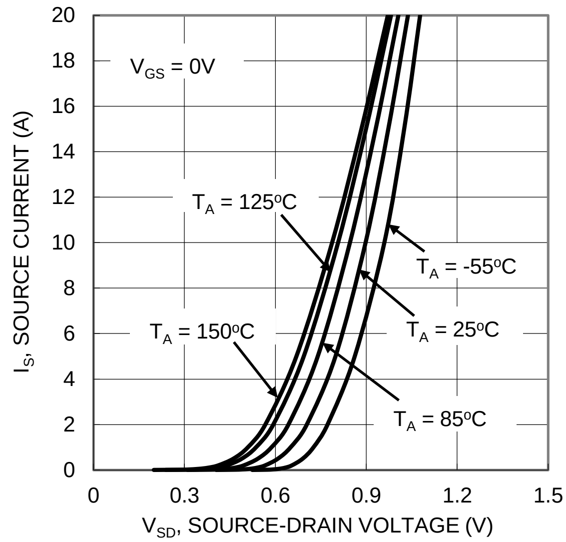


Figure 9 Diode Forward Voltage vs. Current

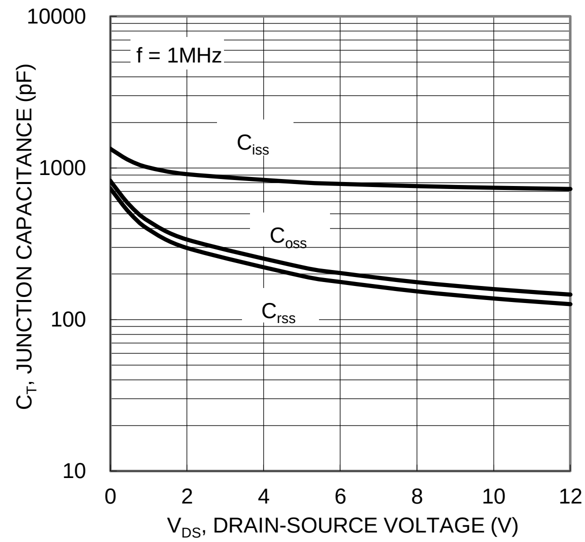
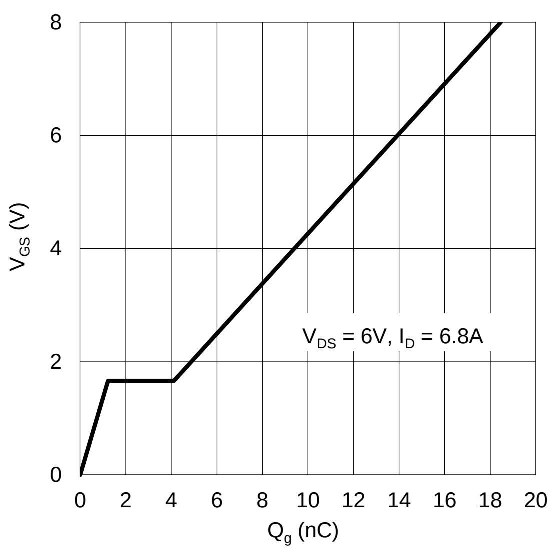


Figure 10 Typical Junction Capacitance



Fiure 11 Gate Charge

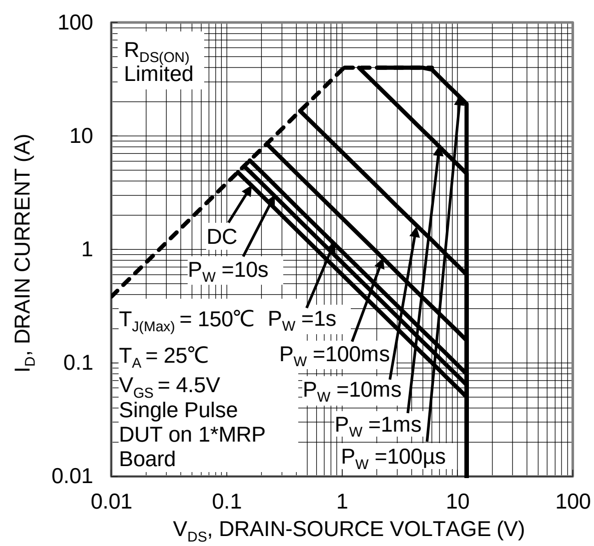


Figure 12 SOA, Safe Operation Area

Typical Characteristics - P-CHANNEL

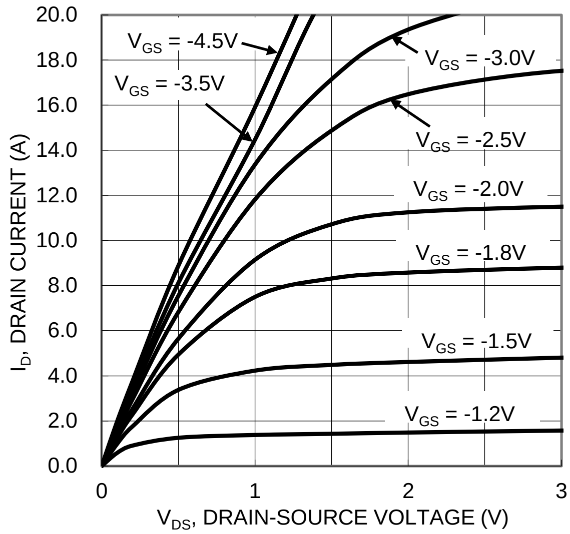


Figure 13 Typical Output Characteristic

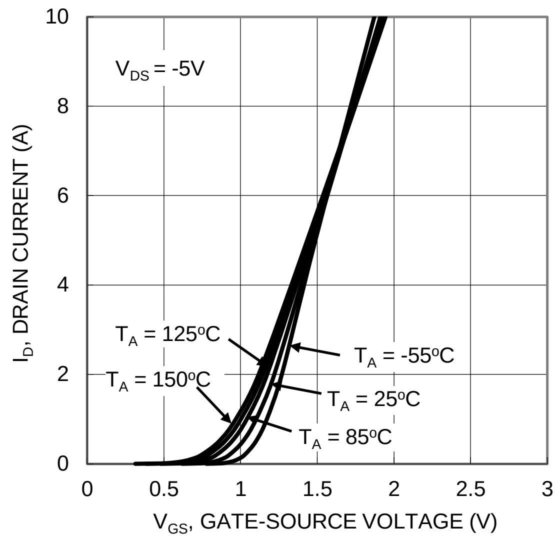


Figure 14 Typical Transfer Characteristic

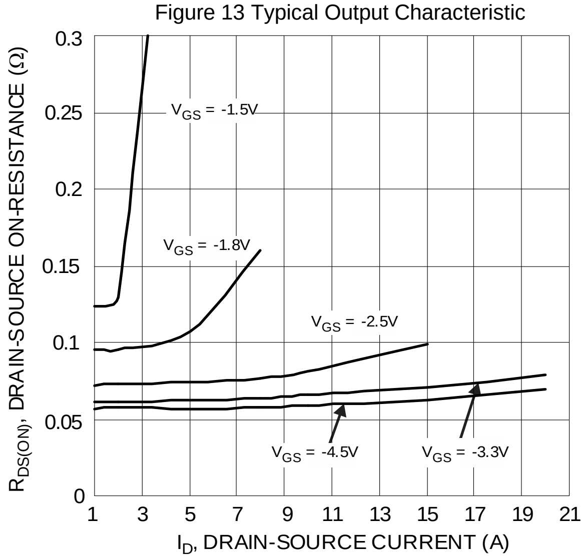


Figure 15 Typical On-Resistance vs. Drain Current and Gate Voltage

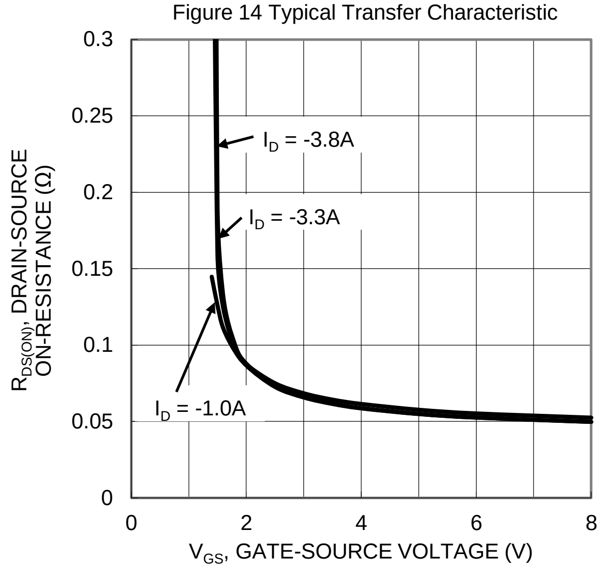


Figure 16 Typical Transfer Characteristic

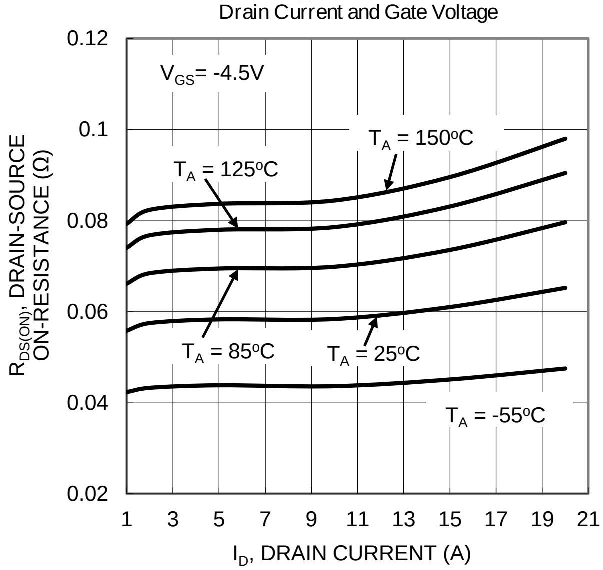


Figure 17 Typical On-Resistance vs. Drain Current and Temperature

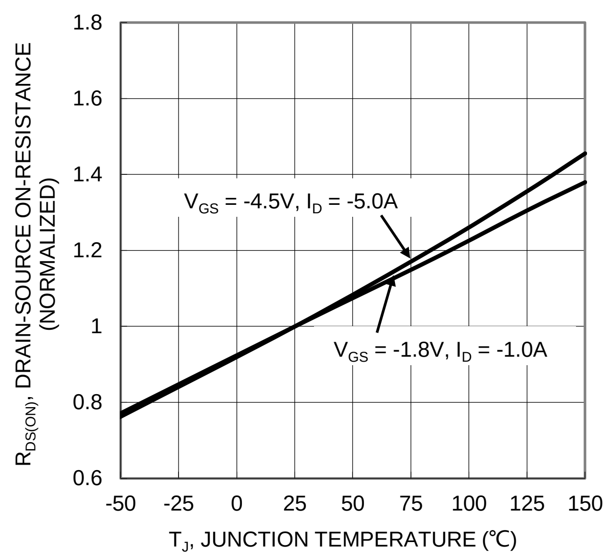


Figure 18 On-Resistance Variation with Temperature

Typical Characteristics - P-CHANNEL (continued)

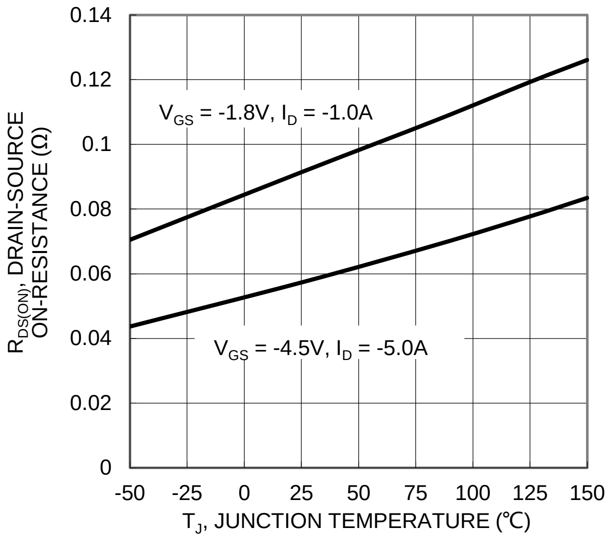


Figure 19 On-Resistance Variation with Temperature

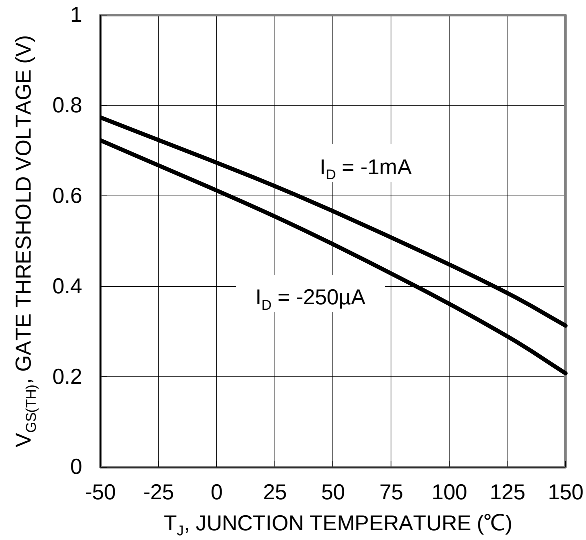


Figure 20 Gate Threshold Variation vs. Junction Temperature

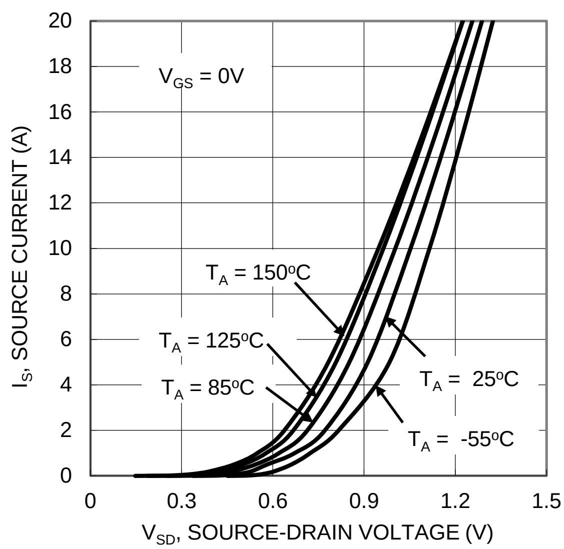


Figure 21 Diode Forward Voltage vs. Current

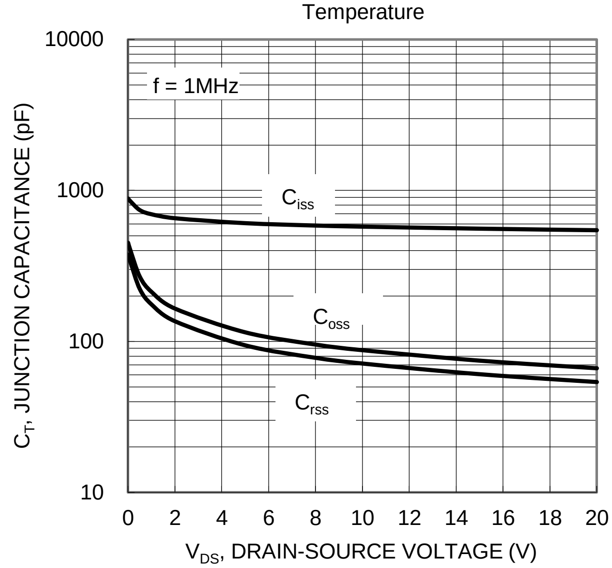


Figure 22 Typical Junction Capacitance

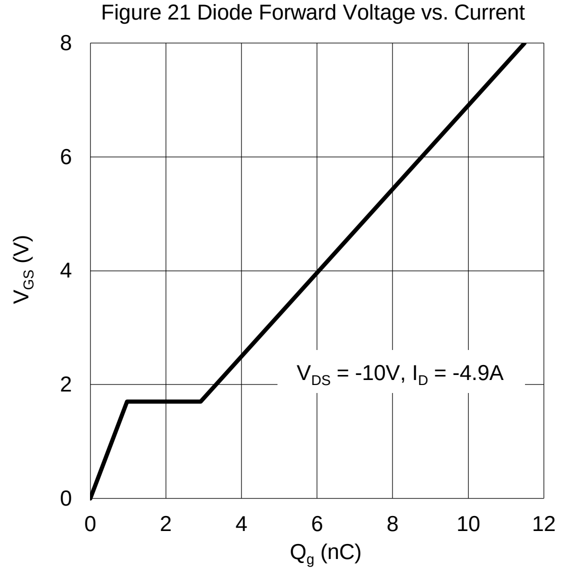


Figure 23 Gate Charge

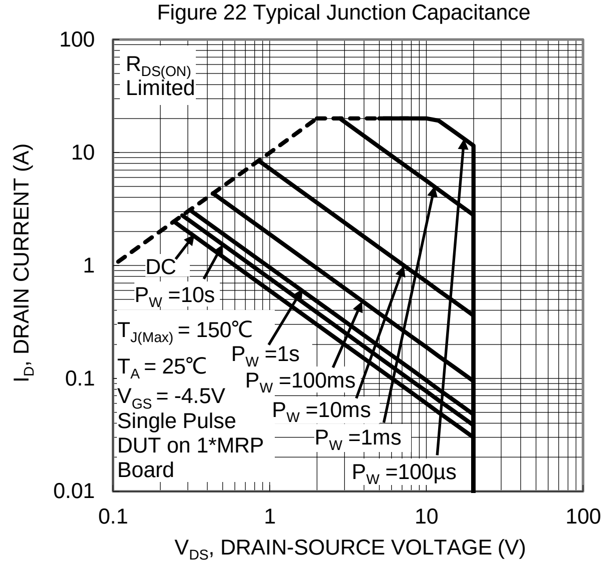


Figure 24 SOA, Safe Operation Area

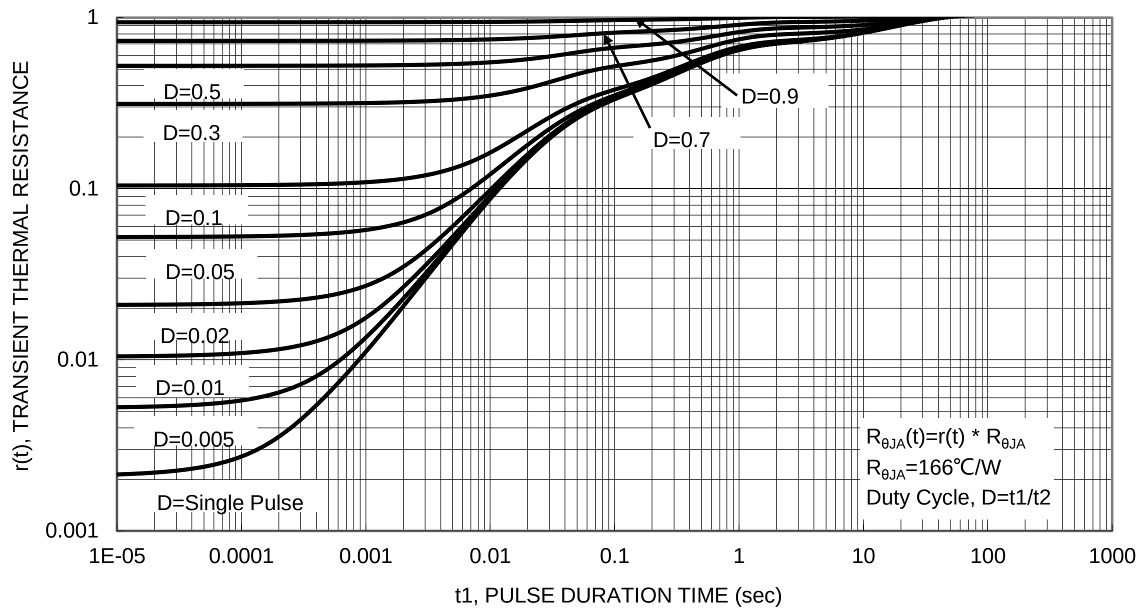
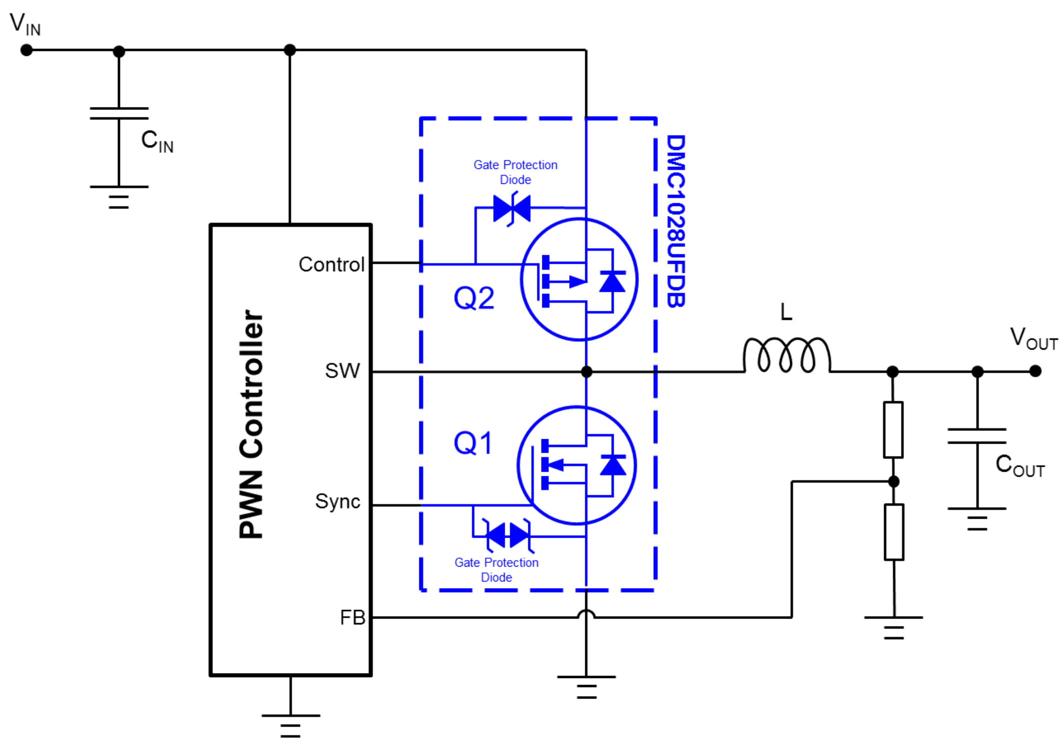


Figure 25 Transient Thermal Resistance

Typical Application Circuit



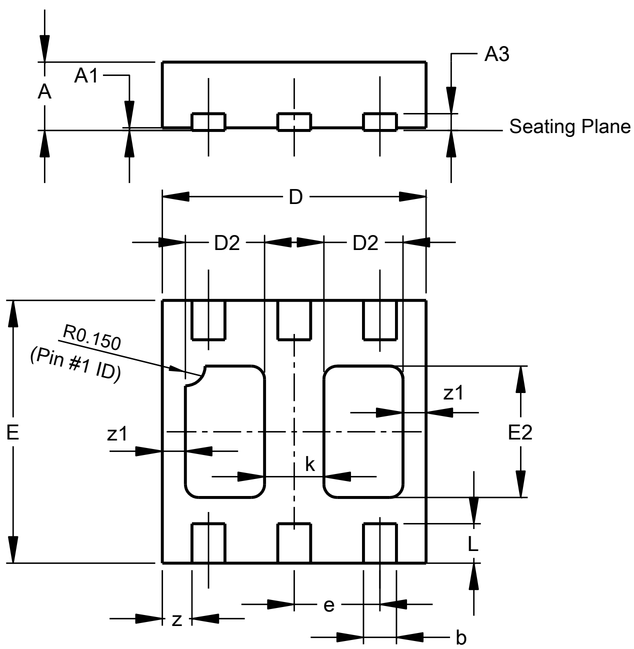
Example of a 3.3V to 1V POL Buck Converter using the DMC1028UFDB

DMC1028UFDB is designed for Point-of-Load (POL) converter that is stepping down from a nominal 3.3V to 1V with a load current up to 3A. This is implemented with a separate ASIC that is PWM signaling the complementary MOSFETs to act as a synchronous buck converter. The control switch (Q2) is implemented with P-channel MOSFETs to avoid needing a charge pump and with the 3.3V to 1V step down, which has a duty cycle of 33%. This means that for 67% of the cycle, the synchronous switch (Q1) is on and efficiency is dominated by the conduction losses; hence, the need for low $R_{DS(ON)}$ N-channel MOSFETs. Whereas for the control switch (Q2), the gate charge needs to be minimized as the switching losses become significant.

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type B)

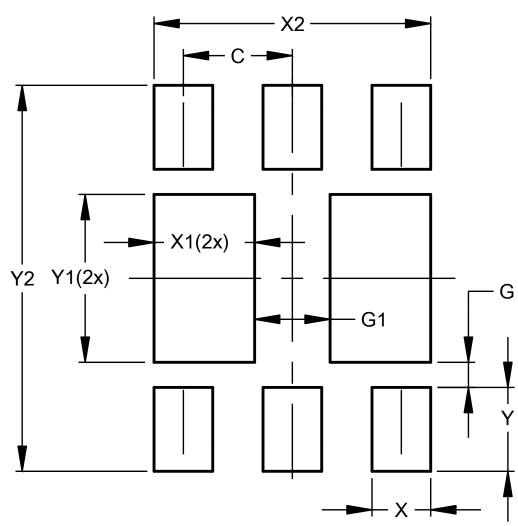


U-DFN2020-6 Type B			
Dim	**Min**	**Max**	**Typ**
A	0.545	0.605	0.575
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	0.50	0.70	0.60
e	-	-	0.65
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
k	-	-	0.45
L	0.25	0.35	0.30
z	-	-	0.225
z1	-	-	0.175
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type B)



Dimensions	Value (in mm)
C	0.650
G	0.150
G1	0.450
X	0.350
X1	0.600
X2	1.650
Y	0.500
Y1	1.000
Y2	2.300

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    1. are intended to implant into the body, or

    2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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