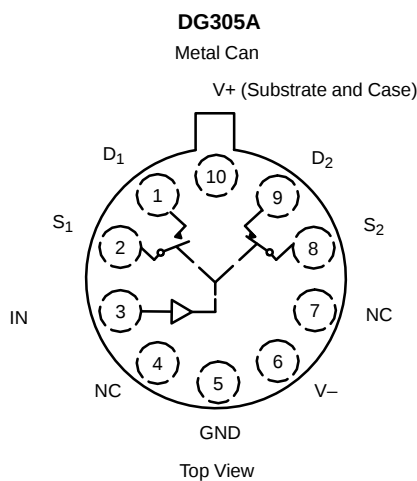
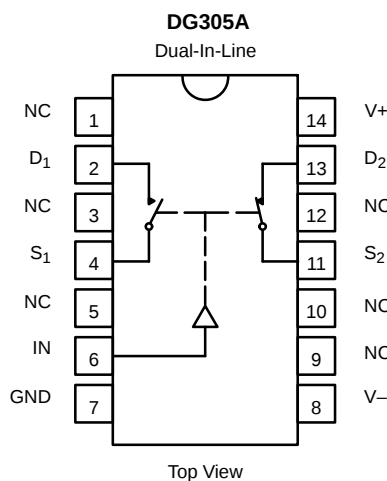
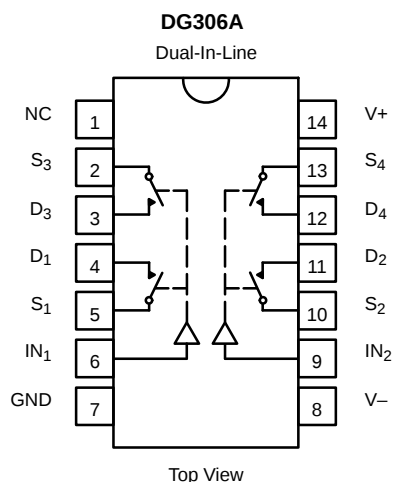


FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



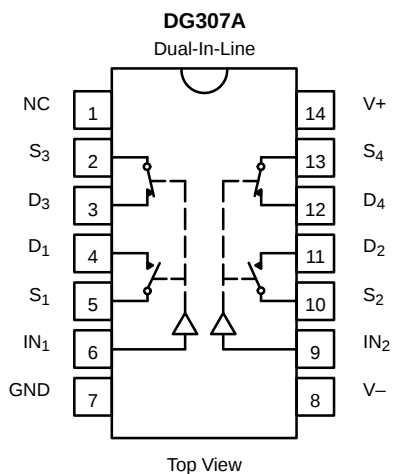
TRUTH TABLE		
Logic	SW ₁	SW ₂
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V



TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V



Four SPST Switches per Package

TRUTH TABLE		
Logic	SW ₁ , SW ₂	SW ₃ , SW ₄
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V



ORDERING INFORMATION		
Temp Range	Package	Part Number
DG304A		
–0 to 70°C	14-Pin Plastic DIP	DG304ACJ
–55 to 125°C	14-Pin CerDIP	DG304AAK/883
		JM38510/11605BCA
	10-Pin Can	JM38510/11605BIA
	14-Pin Sidebrazed	JM38510/11605BCC
DG305A		
–55 to 125°C	14-Pin CerDIP	JM38510/11605BCA
	10-Pin Can	JM38510/11606BIC
	14-Pin Sidebrazed	JM38510/11606BCA
DG306A		
–0 to 70°C	14-Pin Plastic DIP	DG306ACJ
–55 to 125°C	14-Pin CerDIP	DG306AAK/883
		JM38510/11607BCA
	14-Pin Sidebrazed	JM38510/11607BCC
DG307A		
0 to 70°C	14-Pin Plastic DIP	DG307ACJ
–25 to 85°C	14-Pin CerDIP	DG307ABK
–55 to 125°C		DG307AAK
		DG307AAK/883
		JM38510/11608BCA
		14-Pin Sidebrazed

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ 44 V

GND 25 V

Digital Inputs^a, V_S, V_D (V–) –2 V to (V+) +2V or
30 mA, whichever occurs first

Current, Any Terminal 30 mA

Continuous Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature (AAA, AAK, ABK Suffix) –65 to 150°C
(ACJ Suffix) –65 to 125°C

Power Dissipation^b

14-Pin Plastic DIP^c 470 mW

14-Pin CerDIP^d 825 mW

10-Pin Metal Can^e 450 mW

Notes:

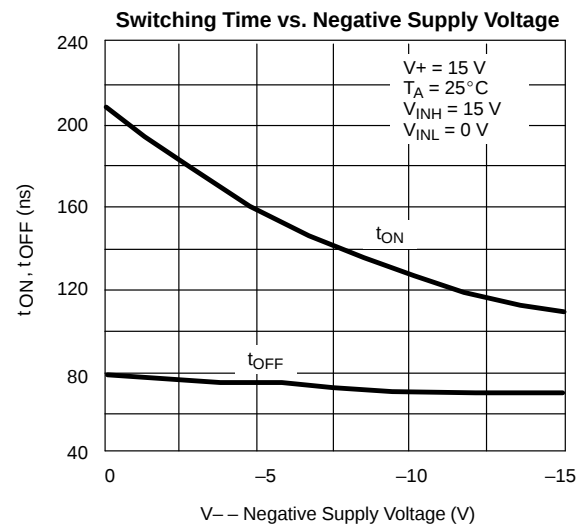
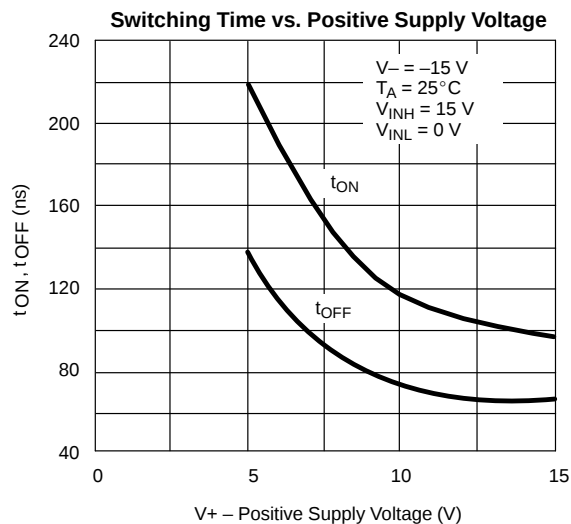
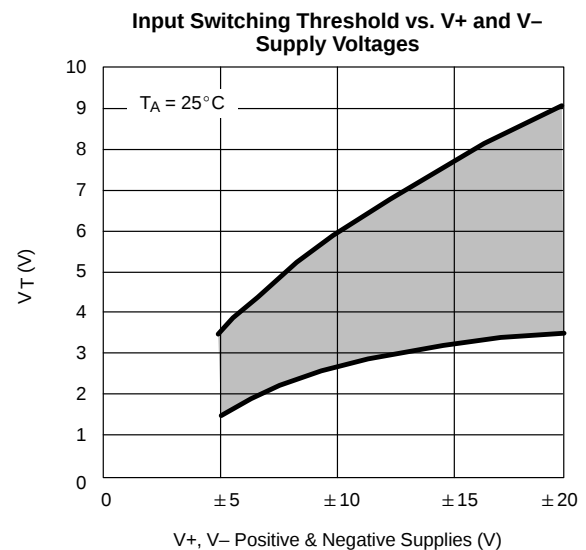
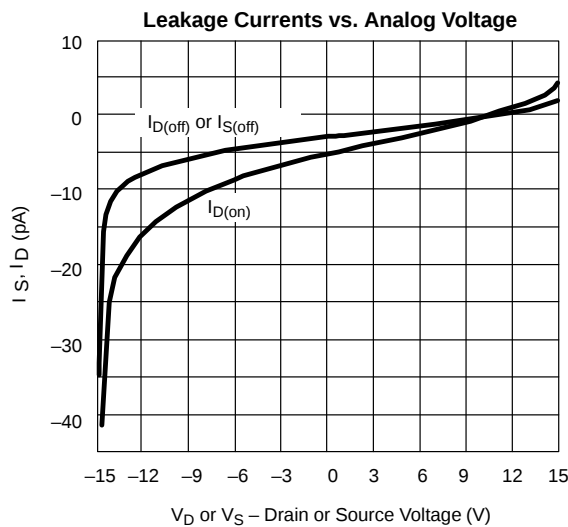
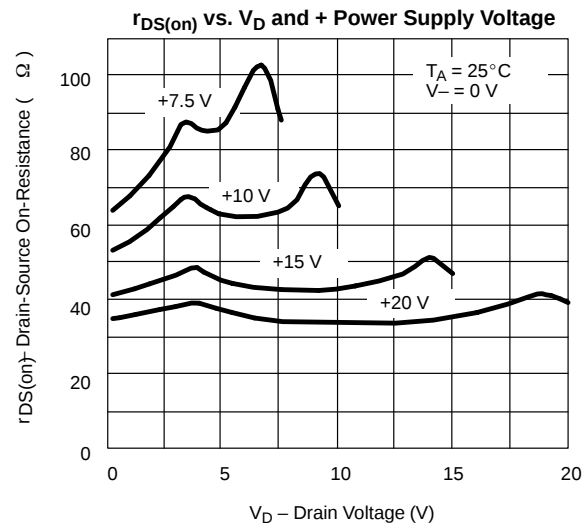
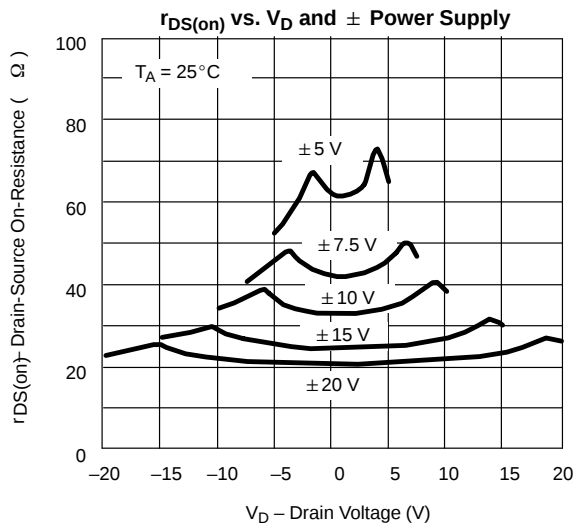
- Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 11 mW/°C above 75°C
- Derate 6.5 mW/°C above 25°C
- Derate 6 mW/°C above 75°C

**SPECIFICATIONS^a**

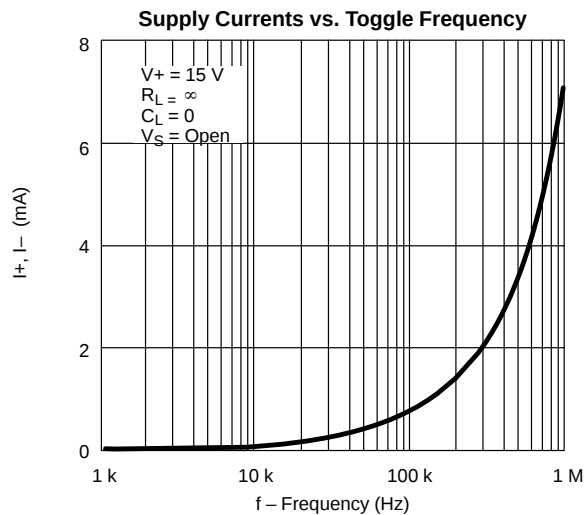
Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V− = −15 V VIN = 3.5 V or 11 V ^f	Temp ^b	Typ ^c	A Suffix −55 to 125°C		B, C Suffix −25 to 85°C 0 to 70°C		Unit	
					Min ^d	Max ^d	Min ^d	Max ^d		
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}		Full		−15	15	−15	15	V	
Drain-Source On-Resistance	r _{DS(on)}	V _D = ± 10 V, I _S = 10 mA	Room Full	30		50 75		50 75	Ω	
Source Off Leakage Current	I _{S(off)}	V _S = ± 14 V V _D = ∓ 14 V	Room Full	± 0.1	−1 −100	1 100	−5 −100	5 100	nA	
Drain Off Leakage Current	I _{D(off)}	V _S = ± 14 V V _D = ∓ 14 V	Room Full	± 0.1	−1 −100	1 100	−5 −100	5 100		
Drain On Leakage Current	I _{D(on)}	V _D = V _S = ± 14 V	Room Full	± 0.1	−2 −200	2 200	−5 −200	5 200		
Digital Control										
Input Current with Input Voltage High	I _{INH}	V _{IN} = 5 V	Room Full	−0.001	−1 −1		−1		μA	
		V _{IN} = 15 V	Room Full	0.001		1 1		1		
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0 V	Room Full	−0.001	−1 −1		−1			
Dynamic Characteristics										
Turn-On Time	t _{ON}	See Figure 2		Room	110		250		ns	
Turn-Off Time	t _{OFF}			Room	70		150			
Break-Before-Make Time	t _{OPEN}	DG305A/307A ONLY See Figure 3		Room	50					
Charge Injection	Q	C _L = 1 nF, R _{gen} = 0 V _{gen} = 0 V, See Figure 4		Room	30				pC	
Source-Off Capacitance	C _{S(off)}	f = 1 MHz, V _S = 0 V V _S , V _D = 0 V		Room	14				pF	
Drain-Off Capacitance	C _{D(off)}			Room	14					
Channel-On Capacitance	C _{D(on)}			Room	40					
Input Capacitance	C _{IN}	f = 1 MHz	V _{IN} = 0 V	Room	6					
			V _{IN} = 15 V	Room	7					
Off-Isolation	OIRR	V _{IN} = 0 V, R _L = 1 kΩ V _S = 1 V _{rms} , f = 500 kHz		Room	62				dB	
Crosstalk (Channel-to-Channel)	X _{TALK}			Room	74					
Power Supplies										
Positive Supply Current	I+	V _{IN} = 15 V or 0 V (All Inputs)		Room Full	0.001		10 100		100	μA
Negative Supply Current	I−			Room Full	−0.001	−10 −100		−100		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

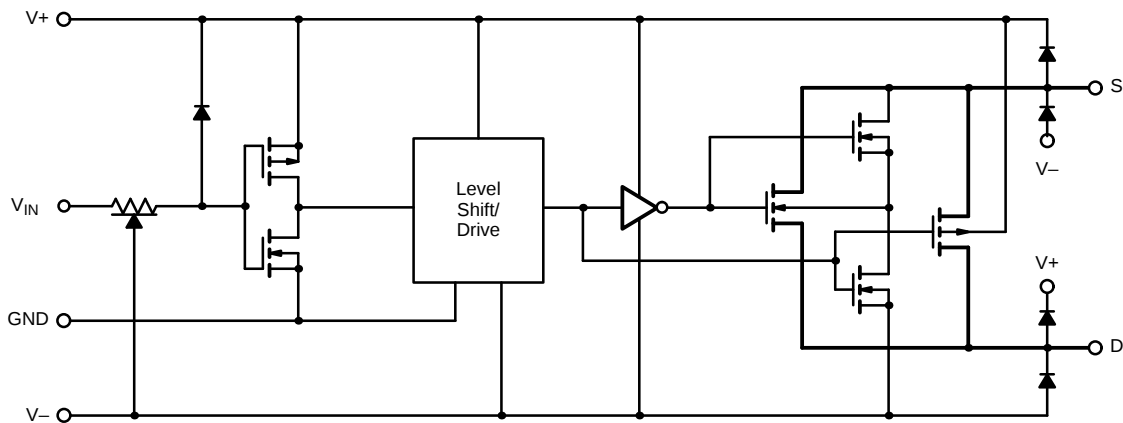


FIGURE 1.

TEST CIRCUITS

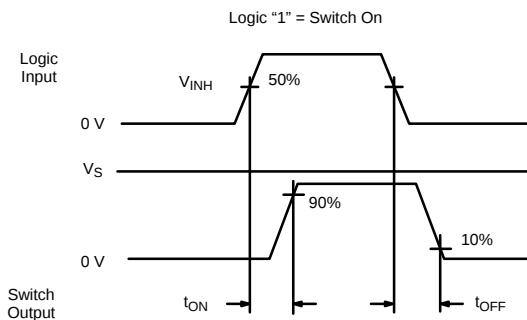
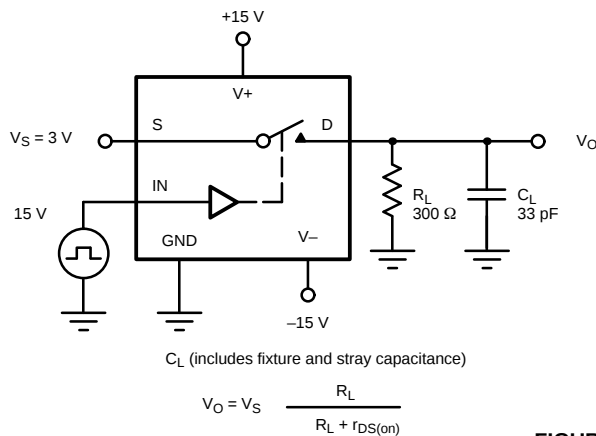


FIGURE 2. Switching Time

TEST CIRCUITS

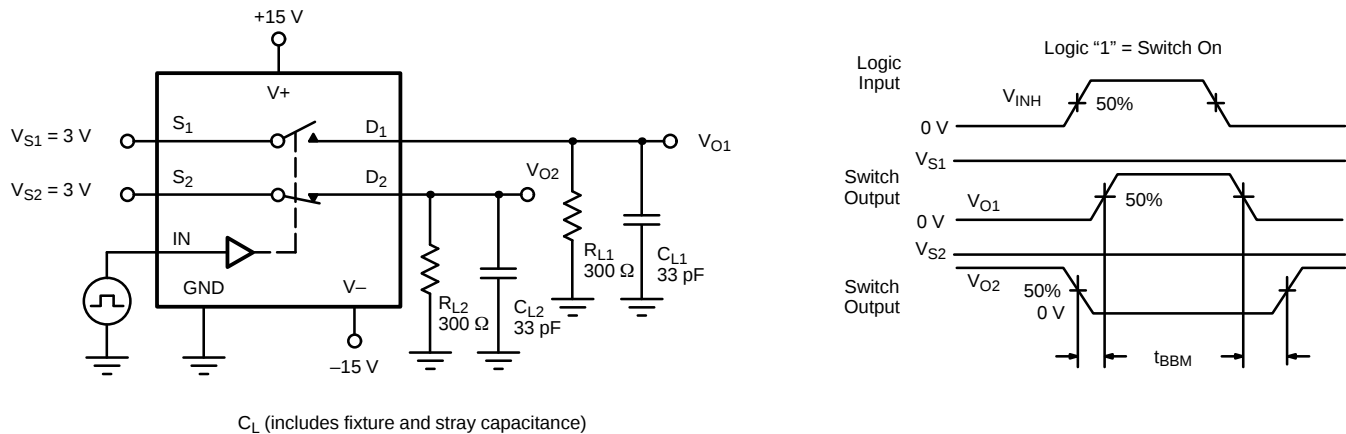


FIGURE 3. Break-Before-Make SPDT (DG305A, DG307A)

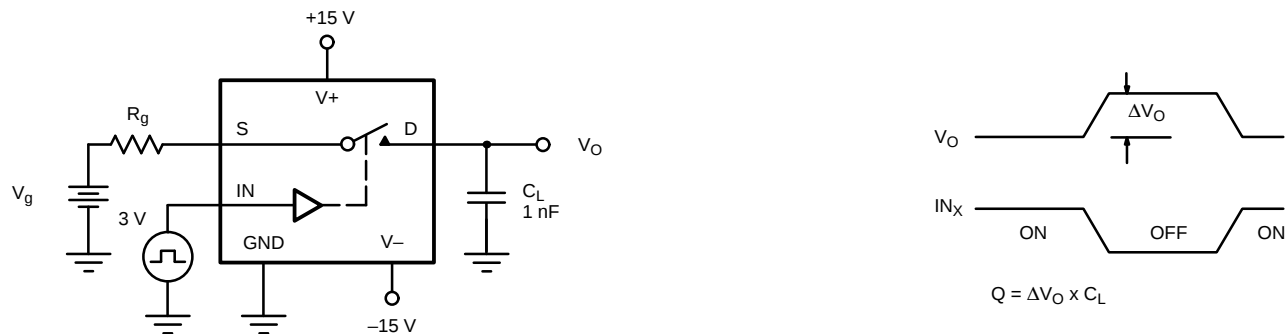


FIGURE 4. Charge Injection

APPLICATION HINTS^a

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Voltage (V)	V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V)	V _S or V _D Analog Voltage Range (V)
15	-15	0	11/3.5	-15 to 15
20	-20	0	11/3.5	-20 to 20
15	0	0	11/3.5	0 to 15

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

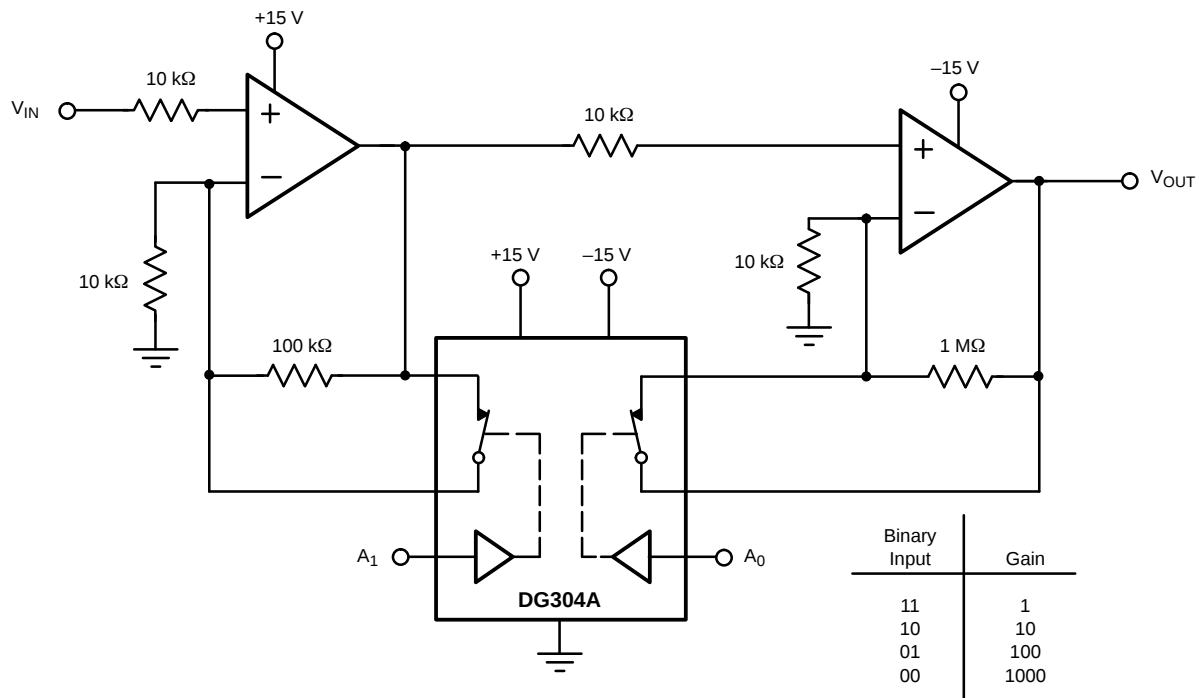


FIGURE 5. Low Power Binary to 10^n Gain Low Frequency Amplifier

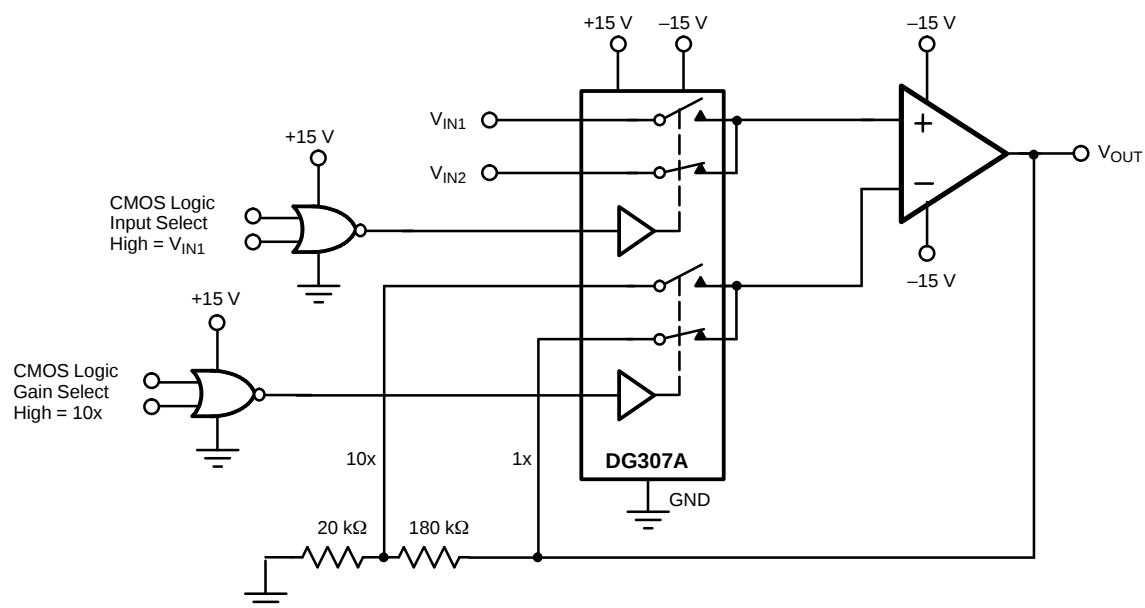


FIGURE 6. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain



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